DATA HANDBOOK

Small- signal Field-effect Transistors

BOOK SC07 1991

Philips Semiconductors

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SMALL-SIGNAL FIELD-EFFECT TRANSISTORS

SELECTION GUIDE

Small-signal field-effect transistors

Selection guide

INTRODUCTION

The following tables represent our complete range of small-signal field-effect transistors, grouped according to main application area.

N-channel junction field-effect transistors, general purpose

TYPE NUMBER	ENVELOPE	$\pm V_{DS}$ (V)	CHARACTERISTICS					REMARKS	PAGE
			I_G (mA)	I_{DSS} min. - max. (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. f = 1 kHz (mS)	C_{rs} (pF)		
BC264A	TO-92 var.	30	10	2 - 4.5	> 0.5	2.5	1.2	hi-fi amplifiers and AF equipment	45
BC264B				3.5 - 6.5		3			
BC264C				5 - 8		3.5			
BC264D				7 - 12		4			
BF245A	TO-92 var.	30	10	2 - 6.5	> 8	3 - 6.5	1.1	DC, LF and HF amplifiers	51
BF245B				6 - 15					
BF245C				12 - 25					
BF246A	TO-92 var.	25	10	30 - 80	0.6 - 14.5	8	3.5	VHF and UHF amplifiers; general purpose switching	63
BF246B				60 - 140					
BF246C				110 - 250					
BF247A	TO-92 var.	25	10	30 - 80	0.6 - 14.5	8	3.5	VHF and UHF amplifiers; general purpose switching	63
BF247B				60 - 140					
BF247C				110 - 250					
BF256A	TO-92 var.	30	10	3 - 70	7.5	4.5	0.7	VHF and UHF applications	65
BF256B				6 - 13					
BF256C				11 - 18					
BF410A	TO-92 var.	20 (note 1)	10	0.7 - 3	typ. 0.8	2.5	0.3	RF stages FM portables	77
BF410B				2.5 - 7	typ. 1.5	4		RF stages car radios	
BF410C				6 - 12	typ. 2.2	6		RF stages mains radios	
BF410D				10 - 18	typ. 3	7		mixer stages	
BF510	SOT23	20	10	0.7 - 3	typ. 0.8	2.5	0.3	RF stages FM portables	81
BF511				2.5 - 7	typ. 1.5	4		RF stages car radios	
BF512				6 - 12	typ. 2.2	6		RF stages mains radios	
BF513				10 - 18	typ. 3	7		mixer stages	
BFR30	SOT23	25	5	4 - 10	5	1 - 4	0.85	low-level, general purpose amplifiers	95
BFR31				1 - 5	2.5	1.5 - 4.5			
BFR101A	SOT143	30	10	0.2 - 1.5	1	1.2	–	source follower	105
BFR101B				1 - 5	2.5	2.5	–		
BFR200	SOT143	30	10	0.2 - 3.5	2	1.3	–	source follower	107

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TYPE NUMBER	ENVELOPE	$\pm V_{DS}$ (V)	CHARACTERISTICS					REMARKS	PAGE
			I_G (mA)	I_{DSS} min. - max. (mA)	$-V_{(P)GS}$ (V)	$\lvert y_{fs} \rvert$ min. f = 1 kHz (mS)	C_{rs} (pF)		
BFT46	SOT23	25	5	0.2 - 1.5	1.2	1	0.85	general purpose amplifier	117
BFW10	TO-72	30	10	8 - 20	8	3.5 - 6.5	0.6	broad band up to 300 MHz and differential ampl.	125
BFW11				4 - 10	6	3 - 6.5			
BFW12	TO-72	30	5	1 - 5	2.5	2	0.6	low current, low voltage applications	137
BFW13				0.2 - 1.5	1.2	1			
BFW61	TO-72	25	10	2 - 20	8	2 - 6.5	< 2	general purpose amplifier	147
2N3822	TO-72	50	10	2 - 10	6	3 - 6.5	< 3	general purpose HF amplifier	213
2N3823	TO-72	30	10	4 - 20	8	3.5 - 6.5	< 2	industrial IF/RF amplifier	215

Note

1. Asymmetrical.

N-channel junction field-effect transistors for differential amplifiers, ($\pm V_{DS}$ = 30 V)
Envelope for BFQ types: TO-71; for BFS types: SOT52.

TYPE NUMBER	RATINGS		CHARACTERISTICS									PAGE
	individual transistor	total device	individual transistor				total device					
	I_G (mA)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$\lvert \Delta V_{GS} \rvert$ max. (mV)	$\lvert \frac{d\Delta V_{GS}}{dT} \rvert$ max. (μV/K)	$\lvert \Delta \frac{1}{g_{fs}} \rvert$ max. (Ω)	$\lvert \Delta \frac{g_{os}}{g_{fs}} \rvert$ max. (μV/V)	CMRR min. (dB)	
			min.	max.	min.	max.						
BFQ10	–	10	0.5	10	0.5	3.5	5	5	6	18	95	87
BFQ11							10	5	6	30	90	
BFQ12							10	10	12	30	85	
BFQ13							10	20	12	30	85	
BFQ14							15	20	12	30	80	
BFQ15							20	40	20	30	80	
BFQ16							50	50	30	100	80	
BFS21	10	0.5	1	–	–	6	20	75	15	1000	60	111
BFS21A							10	40	7.5	500	66	

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N-channel junction field-effect transistors for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
BSR56	SOT23	40	50	50	–	4	10	25	–	9	25	149
BSR57				20	100	2	6	40	5	10	50	
BSR58				8	80	0.8	4	60	–	20	100	
BSV78	TO-18	40	50	50	–	3.75	11	25	–	10	10	153
BSV79				20	–	2	7	40	5	18	16	
BSV80				10	–	1	5	60	–	30	32	
J108	SOT54	25	50	80	–	3	10	8	15	–	–	161
J109				40	–	2	6	12		–	–	
J110				10	–	0.5	4	18		–	–	
J111	TO-92	40	50	20	–	3	10	30	–	–	–	167
J112				5	–	1	5	50	–	–	–	
J113				2	–	0.5	3	100	–	–	–	
PMBF4391	SOT23	40	50	50	150	4	10	30	–	15	20	175
PMBF4392				25	75	2	5	60	3.5		35	
PMBF4393				5	30	0.5	3	100	–		50	
PMBFJ108	SOT54	25	50	80	–	3	10	8	15	–	–	179
PMBFJ109				40	–	2	6	12		–	–	
PMBFJ110				10	–	0.5	4	18		–	–	
PMBFJ111	SOT23	40	50	20	–	3	10	30	–	–	–	185
PMBFJ112				5	–	1	5	50	–	–	–	
PMBFJ113				2	–	0.5	3	100	–	–	–	
PN4391	TO-92	40	50	50	150	4	10	30	5	15	20	195
PN4392				25	100	2	5	60			35	
PN4393				5	60	0.5	3	100			50	
PZFJ108	SOT54	25	50	80	–	3	10	8	15	–	–	199
PZFJ109				40	–	2	6	12		–	–	
PZFJ110				10	–	0.5	4	18		–	–	
2N3966	TO-72	30	10	2	–	4	6	220	1.5	120	100	217
2N4091	TO-18	40	10	30	–	5	10	30	5	25	40	221
2N4092				15	–	2	7	50		35	60	
2N4093				8	–	1	5	80		60	80	
2N4391	TO-18	50	50	50	150	4	10	30	3.5	15	20	233
2N4392				25	75	2	5	60			35	
2N4393				5	30	0.5	3	100			50	

Small-signal field-effect transistors

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TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
2N4856	TO-18	40	50	50	–	4	10	25	8	9	25	241
2N4857		40		20	100	2	6	40		10	50	
2N4858		40		8	80	0.8	4	60		20	100	
2N4859		30		50	–	4	10	25		9	25	
2N4860		30		20	100	2	6	40		10	50	
2N4861		30		8	80	0.8	4	60		20	100	

P-channel junction field-effect transistors for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_G (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V)		$R_{DS(on)}$ max. (Ω)	C_{rs} max. (pF)	t_{on} max. (ns)	t_{off} max. (ns)	
				min.	max.	min.	max.					
J174	TO-92	30	50	20	135	5	10	85	4	7	15	171
J175				7	70	3	6	125		15	30	
J176				2	35	1	4	250		35	35	
J177				1.5	20	0.8	2.25	300		45	40	
PMBFJ174	SOT23	30	50	20	135	5	10	85	4	7	15	191
PMBFJ175				7	70	3	6	125		15	30	
PMBFJ176				2	35	1	4	250		35	35	
PMBFJ177				1.5	20	0.8	2.25	300		45	40	

N-channel, single gate MOS-FETs for switching

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS								PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} (mA)		$-V_{(P)GS}$ (V) (note 1)		mode	$R_{DS(on)}$ max. (Ω)	C_{rs} typ. (pF)	t_{on}/t_{off} typ. (ns)	
				min.	max.	min.	max.					
BFR29	TO-72	30 (note 2)	20	10	40	0.5	3.5	depl.	–	0.4	–	259
BSD12	TO-72	20	50	–	–	–	2	depl.	30	0.6	1/5	267
BSD22	SOT143	20	50	–	–	–	2	depl.	30	0.6	1/5	271
BSD212	TO-72	10	50	–	–	0.1	2	enh.	70	0.6	1/5	275
BSD213		10										
BSD214		20										
BSD215		20										
BSS83	SOT143	10	50	–	–	0.1	2	enh.	45	0.6	1/5	279
BSV81	TO-72	30 (note 2)	25	–	–	–	–	depl.	100	0.5	–	283

Notes

1. Enhancement types $V_{GS(th)}$.
2. V_{DB}/V_{SB}.

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N-channel, dual gate MOS-FETs

All types protected against excessive input voltage surges, except BF980A and BF994S.

TYPE NUMBER	ENVELOPE	RATINGS		CHARACTERISTICS							REMARKS	PAGE
		V_{DS} (V)	I_D (mA)	I_{DSS} (mA) min.	I_{DSS} (mA) max.	$-V_{(P)G1-S}$ max. (V)	$\|y_{fs}\|$ f = 1 kHz min. (mS)	C_{is} typ. (pF)	C_{os} typ. (pF)	F typ. (dB)		
BF960	SOT103	20	20	2	20	2.7	9.5	1.8	0.9	2.8	UHF	291
BF964S	SOT103	20	30	4	20	2.5	15	2.5	1	1	VHF	295
BF965	SOT103	20	30	2	20	2.5	15	2.5	1	1	VHF	301
BF966S	SOT103	20	30	4	20	2.5	15	2.3	0.8	1.8	UHF	305
BF980A	SOT103	18	30	–	–	1.3	18	2.6	1.1	2	UHF	311
BF981	SOT103	20	20	4	25	2.5	10	2.1	1.1	1	VHF	317
BF982	SOT103	20	40	–	–	1.3	20	4	2	1.2	VHF	325
BF988	SOT103	12	30	2	18	2.5	21	2.1	1.05	1	VHF & UHF	329
BF989	SOT143	20	20	2	20	2.7	9.5	1.8	0.9	2.8	UHF	341
BF990A	SOT143	18	30	–	–	1.3	18	2.6	1.2	2.8	UHF	345
BF990AR	SOT143R	18	30	–	–	1.3	18	–	1.2	2	UHF	349
BF991	SOT143	20	20	4	25	2.5	10	2.1	1.1	0.7	VHF	351
BF992	SOT143	20	40	–	–	1.3	20	4	2	1.2	VHF	355
BF992R	SOT143R	20	40	–	–	1.3	20	–	2	1.2	VHF	361
BF994S	SOT143	20	30	4	20	2.5	15	2.5	1	1	VHF	363
BF996S	SOT143	20	30	4	20	2.5	15	2.3	0.8	1.8	UHF	367
BF997	SOT143	20	30	2	20	2.5	15	2.5	1	1	VHF	371
BF998	SOT143	12	30	2	18	2.5	21	2.1	1.05	1	VHF & UHF	375
BF998R	SOT143R	12	30	2	18	2.5	21	2.1	1.05	1	VHF & UHF	385
BFR84	TO-72	20	50	20	55	3.8	12	5.5	3.5	2.3	general purpose	395

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N-channel vertical D-MOS-FETs for switching

TYPE NUMBER	ENVELOPE	RATINGS				CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	at T_{amb} (°C)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS107	TO-92 var.	200	120	500	25	1.8 (typ.)	15	28	20	2.6	10/10	403
BS107A	TO-92 var.	200	250	600	25	1 - 3	4.5	6.4	250	10	5/15	411
BS170	TO-92 var.	60	500	830	25	0.8 - 3	2.5	5	200	10	10/10	415
BSN204	SOT54	200	250	1000	25	0.4 - 1.8	5	8	100	2.8	10/30	429
BSN204A	SOT54	200	250	1000	25	0.4 - 1.8	5	8	100	2.8	10/30	429
BSN205	TO-92 var.	200	300	1000	25	0.8 - 2.8	3.5	6	400	10	10/20	435
BSN205A	TO-92 var.	200	300	1000	25	0.8 - 2.8	3.5	6	400	10	10/20	435
BSN254	TO-92 var.	250	300	1000	25	0.8 - 2.2	4.5	10	20	2.4	–	439
BSN254A	TO-92 var.	250	300	1000	25	0.8 - 2.2	4.5	10	20	2.4	–	439
BSN274	TO-92 var.	270	250	1000	25	0.8 - 2	6.5	14	20	2.4	10/30	443
BSN274A	TO-92 var.	270	250	1000	25	0.8 - 2	6.5	14	20	2.4	10/30	443
BSP103		35	700	1500	25	0.8 - 2	1.5	5			10/15	
BSP105	SOT223	60	500	1500	25	0.8 - 2	1.8	5	300	5	10/15	449
BSP109		90	450	1500	25	0.8 - 2	2.5	5.3			10/15	
BSP106	SOT223	60	425	1500	25	0.8 - 3	2.5	4	200	10	5/15	455
BSP107	SOT223	200	200	1500	25	0.8 - 2.4	20	28	20	2.6	10/20	463
BSP108	SOT223	80	500	1500	25	1.5 - 3.5	2	3	500	10	8/15	471
BSP110	SOT223	80	325	1500	25	0.8 - 2.8	7	10	150	5	5/10	475
BSP120	SOT223	200	250	1500	25	0.8 - 2.8	7	12	250	10	6/20	479
BSP121	SOT223	200	350	1500	25	0.8 - 2.8	4.5	6	400	10	10/20	483
BSP126	SOT223	250	350	1500	25	0.8 - 2	5	10	20	2.4	10/30	489
BSS87	SOT89	200	280	1000	25	0.8 - 2.8	4.5	6	400	10	10/25	537
BSS89	TO-92 var.	200	300	1000	25	0.8 - 2.8	4.5	6	400	10	–	541
BSS91	TO-18	200	350	1500	25 (note 1)	0.8 - 2.8	4.5	6	400	10	15/25	545
BST70A	TO-92 var.	80	500	1000	25	1.5 - 3.5	2	4	500	10	10/15	581
BST72A	TO-92 var.	80	300	830	25	1.5 - 3.5	7	10	150	5	10/10	585
BST74A	TO-92 var.	200	300	1000	25	0.8 - 2.8	6	12	250	10	10/25	589
BST76A	TO-92 var.	180	300	1000	25	0.7 - 2.7	7	10	15	3	10/15	593
BST78	TO-126	450	750	15000	75 (note 2)	2 - 4	10	14	100	10	10/100	597
BST80	SOT89	80	500	1000	25	1.5 - 3.5	2	4	500	10	10/15	601
BST82	SOT23	80	175	300	25	1.5 - 3.5	7	10	150	5	10/10	605
BST84	SOT89	200	250	1000	25	0.8 - 2.8	6	12	250	10	10/25	609
BST86	SOT89	180	300	1000	25	0.7 - 2.7	7	10	15	3	10/15	613

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TYPE NUMBER	ENVELOPE	RATINGS				CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	at T_{amb} (°C)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
PH6659		35	750				1.5	5				
PH6660	TO-92 var.	60	500	1000	25	0.8 - 2	1.8	5	300	5	10/10	633
PH6661		90	500				2.4	5.3				
PMBF107	SOT23	200	100	250	25	0.8 - 2.4	20	28	20	2.6	10/20	637
PMBF170	SOT23	60	250	300	25	0.8 - 3	2.5	5	200	10	10/15	645
VN2406L	TO-92 var.	240	210	1000	25	0.8 - 2	–	6	500	10	10/30	649
VN2410L	TO-92 var.	240	150	1000	25	0.8 - 2	–	10	100	2.5	10/30	657
2N6659		35	1400				1.5	5				
2N6660	TO-39	60	1100	6250	25 (note 2)	0.8 - 2	1.8	5	300	5	10/20	665
2N6661		90	900				2.4	5.3				
2N7000	TO-92 var.	60	280	830	25	0.8 - 3	2.5	5.3	75	4.5	10/10	669
2N7002	SOT23	60	180	300	25	0.8 - 3	2.5	5.3	75	4.5	10/15	677

Notes

1. T_{case}.
2. T_{mb}.

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P-channel vertical D-MOS-FETs for switching

TYPE NUMBER	ENVELOPE	RATINGS				CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	at T_{amb} (°C)	$V_{GS(th)}$ (V)	$R_{DS(on)}$ (Ω) typ.	$R_{DS(on)}$ (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS208	TO-92 var.	200	200	830	25	0.8 - 2.8	10	14	200	10	10/30	419
BS250	TO-92 var.	45	250	830	25	1.3 - 5	9	14	200	10	4/10	425
BSP204	TO-92 var.	200	250	1000	25	0.8 - 2.8	10	15	200	10	–	495
BSP204A	TO-92 var.	200	250	1000	25	0.8 - 2.8	10	15	200	10	–	495
BSP205	SOT223	60	275	1500	25	1.5 - 3.5	7.5	10	200	10	6/15	503
BSP206	SOT223	60	350	1500	25	1.5 - 3.5	4.5	6	200	10	8/25	507
BSP220	SOT223	200	225	1500	25	0.8 - 2.8	10	12	200	10	20/30	511
BSP225	SOT223	250	225	1500	25	0.8 - 2.8	10	15	200	10	10/30	519
BSP254	TO-92 var.	250	200	1000	25	0.8 - 2.8	10	15	200	10	10/30	527
BSP254A	TO-92 var.	250	200	1000	25	0.8 - 2.8	10	15	200	10	10/30	527
BSS92	TO-92 var.	200	250	1000	25	0.8 - 2.8	10	20	100	10	–	549
BSS192	SOT89	200	150	1000	25	0.8 - 2.8	10	20	100	10	10/30	573
BST100	TO-92 var.	60	300	1000	25	1.5 - 3.5	4.5	6	200	10	4/20	617
BST110	TO-92 var.	50	300	830	25	1.5 - 3.5	7.5	10	200	10	4/20	621
BST120	SOT89	60	300	1000	25	1.5 - 3.5	4.5	6	200	10	4/20	625
BST122	SOT89	50	250	1000	25	1.5 - 3.5	7.5	10	200	10	4/20	629

TYPE NUMBER SURVEY

Small-signal field-effect transistors — Type number survey

In this alphanumeric list we present all small-signal transistors mentioned in this handbook.

Small-signal field-effect transistors — Type number survey

TYPE NUMBER	PAGE	TYPE NUMBER	PAGE	TYPE NUMBER	PAGE	TYPE NUMBER	PAGE
2N4220	225	2N4392	233	2N4860	241	2N5486	253
2N4220A	225	2N4393	233	2N4861	241	2N6659	665
2N4221	225	2N4416	237	2N5116	245	2N6660	665
2N4221A	225	2N4416A	237	2N5460	249	2N6661	665
2N4222	225	2N4856	241	2N5461	249	2N7000	669
2N4222A	225	2N4857	241	2N5462	249	2N7002	677
2N4340	229	2N4858	241	2N5484	253		
2N4391	233	2N4859	241	2N5485	253		

GENERAL

PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

"Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do."

A basic type number consists of:
TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
B. SILICON or other material with band gap of 1,0 to 1,3 eV.
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\ j\text{-}mb} > 15$ K/W)
D. TRANSISTOR; power, audio frequency ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\ j\text{-}mb} > 15$ K/W)
G. MULTIPLE OF DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\ j\text{-}mb} > 15$ K/W)
S. TRANSISTOR; low power, switching ($R_{th\ j\text{-}mb} > 15$ K/W)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
U. TRANSISTOR; power, switching ($R_{th\ j\text{-}mb} \leqslant 15$ K/W)
X. DIODE: multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.*
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.*
This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*
   The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage
   A. 1% (according to IEC 63: series E96)
   B. 2% (according to IEC 63: series E48)
   C. 5% (according to IEC 63: series E24)
   D. 10% (according to IEC 63: series E12)
   E. 20% (according to IEC 63: series E6)
   The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.
   The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*
   The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R. The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*
   The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER,* preceded by a hyphen (–)
   The NUMBER indicates the depletion layer in μm. The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER,* preceded by a stroke (/).
   The NUMBER indicates how many basic devices are assembled into the array.

* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

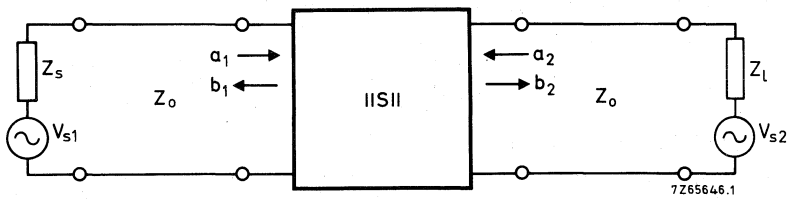
Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}} \qquad 1)$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \frac{b_1}{a_1}\bigg|_{a_2 = 0}$$
$$s_r = s_{12} = \frac{b_1}{a_2}\bigg|_{a_1 = 0}$$
$$s_f = s_{21} = \frac{b_2}{a_1}\bigg|_{a_2 = 0}$$
$$s_o = s_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o = 50\ \Omega$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o = 50\ \Omega$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o = 50\ \Omega$ and $V_{s2} = 0$.

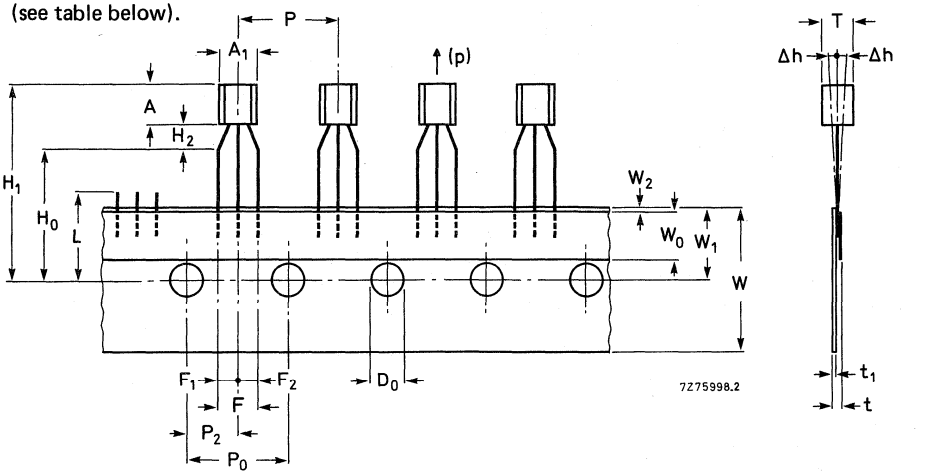
$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o = 50\ \Omega$ and $V_{s1} = 0$.

TO-92 VARIANT TRANSISTORS ON TAPE

MECHANICAL DATA

Dimensions in mm

Fig. 1 (see table below).



Item	Symbol	Specifications				Remarks
		min.	nom.	max.	tol.	
Body width	A_1	4,0		4,8		
Body height	A	4,8		5,2		
Body thickness	T	3,9		4,2		
Pitch of component	P		12,7		± 1	
Feed hole pitch	P_o		12,7		± 0,3	Cumulative pitch error 1,0 mm/20 pitch
Feed hole centre to component centre	P_2		6,35		± 0,4	To be measured at bottom of clinch
Distance between outer leads	F		5,08		+ 0,6 −0,2	
Component alignment	Δh		0	1		At top of body
Tape width	W		18		± 0,5	
Hold-down tape width	W_o		6		± 0,2	
Hole position	W_1		9		+ 0,7 −0,5	
Hold-down tape position	W_2		0,5		± 0,2	
Lead wire clinch height	H_o		16		± 0,5	
Component height	H_1			32,25		
Length of snipped leads	L			11,0		
Feed hole diameter	D_o		4		± 0,2	
Total tape thickness	t			1,2		t_1 0,3-0,6
Lead-to-lead distance	F_1, F_2		2,54		+ 0,4 −0,1	
Clinch height	H_2			3		
Pull-out force	(p)	6N				

PACKING

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel is 1600 and per ammobox 2000*.

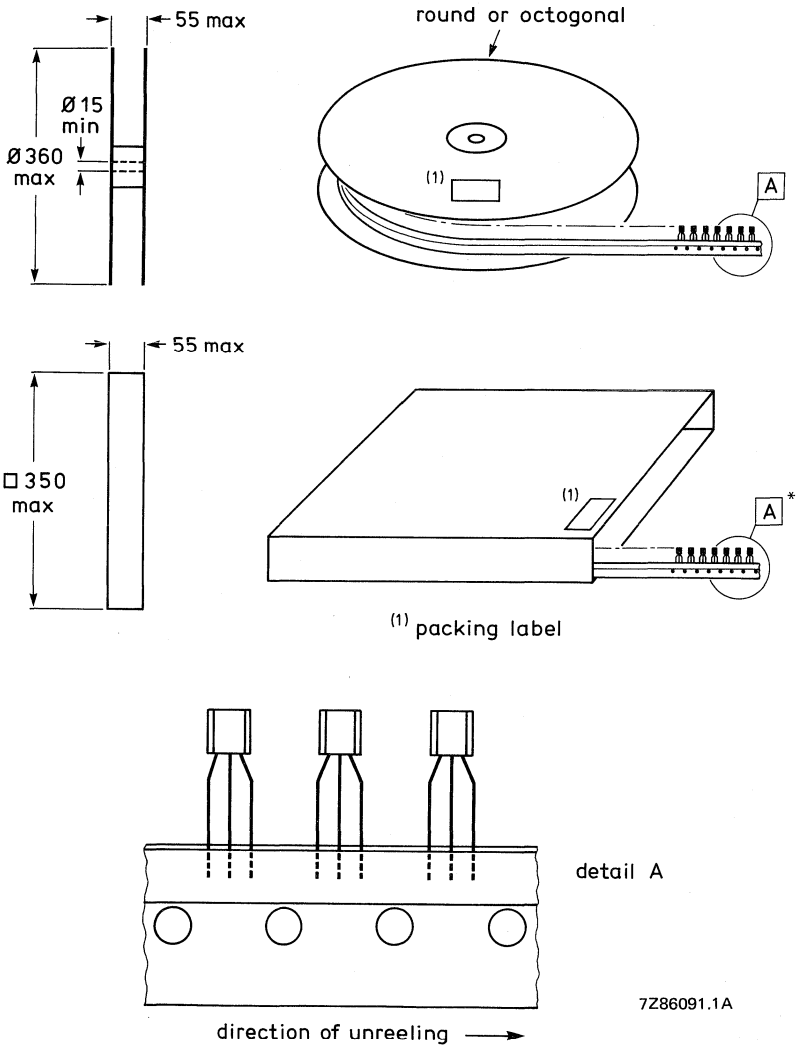


Fig. 2 Dimensions (in mm) of reel and box.

DROPOUTS

A maximum of 0,5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Slice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Fig. 3).

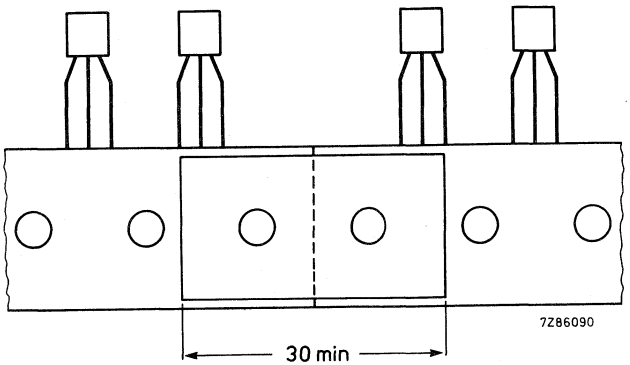


Fig. 3 Jointing tape with splicing patch.

* The ammobox has 80 layers of 25 transistors each.
Each layer contains 25 transistors plus one empty position in order to fold the layer correctly.

The ammobox is accessible from both sides enabling the user to choose between "normal" (see Fig. 2) and "reverse" tape.

TAPE AND REEL SPECIFICATION

Semiconductors in SOT-23, SOT-143 and SOT-89 encapsulations can be delivered in reel packing for aotomatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.

A separate reel packing for SOT-89 encapsulation is given in Fig. 3.

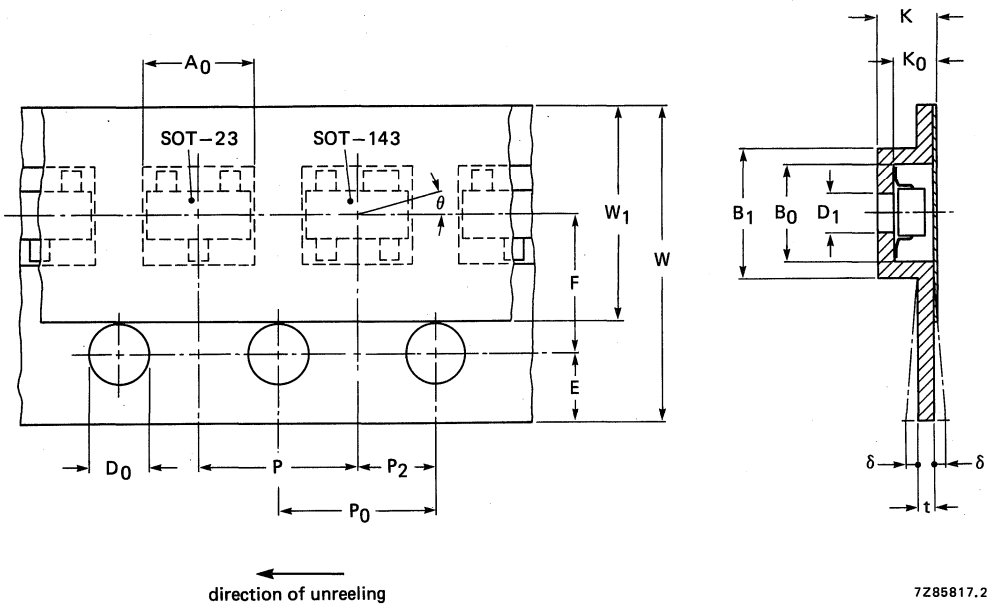


Fig. 1 Configuration of bandolier. Dimensions in mm.

Compartment			tol.
length	A_0	component length	+0,2
width	B_0	component width	+0,2
depth	K_0	0,95	+0,2
width outside	B_1	3,3	max.
pitch	P	4,0	±0,1
deviation	Θ	15°	max.
hole diameter	D_1	1	min.
Sprocket hole			
diameter	D_0	1,5	+0,1
pitch	P_0	4,0	±0,1
distance	E	1,75	±0,1
cumulative (10) pitch error		±0,1	

Centre line dimensions			tol.
length direction	P_2	2,0	±0,05
width direction	F	3,5	±0,05
Fixing tape			
width	W_1	5,5	±0,25
thickness	—	0,1	max.
Carrier tape			
width	W	8,0	±0,2
bending	δ	0,3	max.
thickness	t	0,4	max.
Overall thickness	K	1,5	max.

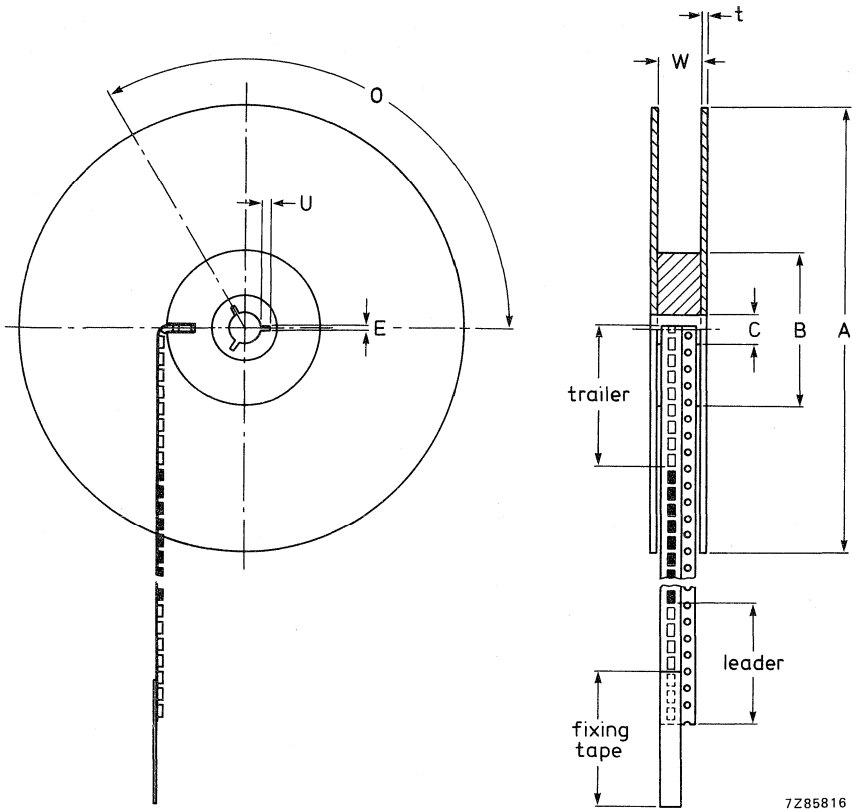


Fig. 2 Configuration of reel and flange (dimensions in mm).

Flange			tol.
diameter	A	180	$^{+0}_{-2}$
thickness	t	1,5	$^{+0,5}_{-0,1}$
space between flanges	W	9,5	± 0,5

Hub			tol.
diameter	B	62	± 1,5
spindle hole	C	12,75	$^{+0,15}_{-0}$
key slit			
width	E	2	± 0,5
depth	U	4	± 0,5
location	O	120	degrees

Amount of devices per reel

The bandolier of a 180 mm reel contains at least 3000 devices with no more than 15 empty compartments (0,5%). Three consecutive empty places might be found provided this gap is followed by 6 consecutive devices.

The carrier tape (leader) starts with at least 75 empty positions (equivalent to 300 mm); the covering foil is at least 300 mm. In order to fix the carrier tape a self-adhesive tape of 20 to 50 mm is applied.

At the end of the bandolier (trailer) at least 75 empty positions (equivalent to a length of 300 mm) and 300 mm foil. For fixing onto the reel a self-adhesive tape of 20 to 50 mm is applied.

Semiconductors in SOT-89 encapsulations can also be delivered in reel packing for automatic placement on hybrid circuits and printed circuit boards. The devices are placed with the mounting side downwards in compartments.Total number of devices per reel is 1000.

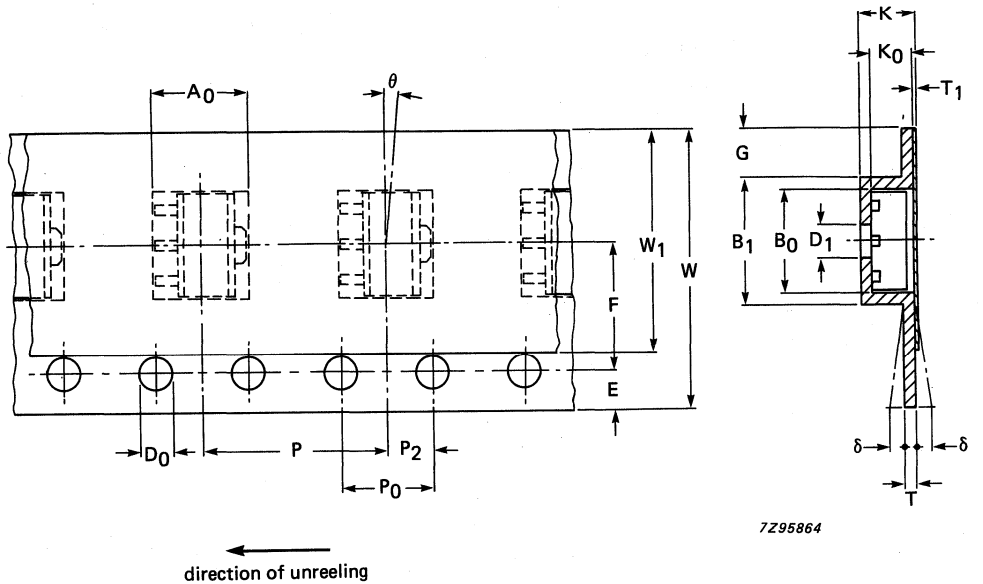


Fig. 3 Configuration of bandolier. Dimensions in mm.

			tol.
Compartment			
length	A_0	component length	
width	B_0	component width	
depth	K_0	component depth	
width outside	B_1	5,7	max.
pitch	P	8,0	± 0,1
deviation	Θ	± 5°	max.
hole diam.	D_1	1,5	min.
Sprocket hole			
diameter	D_0	1,5	+ 0,1
pitch	P_0	4,0	± 0,1
distance	E	1,75	± 0,1
cumulative (10) pitch error		± 0,1	

			tol.
Centre line dimensions			
length direction	P_2	2,0	± 0,05
width direction	F	5,5	± 0,1
Fixing tape			
width	W_1	9,5	max.
thickness	T_1	0,1	max.
Carrier tape			
width	W	12	± 0,2
bending	δ	0,3	max.
thickness	T	0,4	max.
Overall thickness	K	2,4	max.
distance	G	1,8	min.

SOLDERING RECOMMENDATIONS
SOT-23, SOT-143 AND SOT-89 ENVELOPES

SOT-23, SOT-143 and SOT-89 devices are ideally suited for placement onto thick and thin film substrates and printed circuit boards.

To assure reliable and consistent connections particular attention should be paid to:

1. **Flux**

   A non-active flux is recommended. Where active fluxes are employed, great care in subsequent substrate cleaning must be exercised.

2. **Metal-alloy solder or solder paste**

   Correct choice of solder alloy or solder paste to be employed e.g. 62% Sn, 36% Pb, 2% Ag or 60% Sn/40% Pb. Any paste used should contain at least 85% metal dry weight.

3. **Soldering temperature**

   This will vary according to the actual method employed.

REFLOW SOLDERING

The preferred technique for mounting microminiature components on hybrid thick and thin-film is the method of reflow soldering.

The tags of SOT-23, SOT-143 and SOT-89 envelopes are pre-tinned and the best results are obtained if a similar solder is applied to the corresponding soldering areas on the substrate. This can be done by either dipping the substrate in a solder bath or by screen printing a solder paste.
The maximum temperature of the leads or tab during the soldering cycle should not exceed 285 °C.
The most economic method of soldering is a process in which all different components are soldered simultaneously for example SOT-23, SOT-143 or SOT-89 devices, capacitors and resistors.

Having first been fluxed, all components are positioned on the substrate. The slight adhesive force of the flux is sufficient to keep the components in place. Solder paste contains a flux and has therefore good inherent adhesive properties which eases positioning of the components.

With the components in position the substrate is heated to a point where the solder begins to flow. This can be done on a heating plate or on a conveyor belt running through an infrared tunnel. The maximum allowed temperature of the plastic body of a device must be kept below 280 °C during the soldering cycle. For further temperature behaviour during the soldering process see Figs 2 and 3.

The surface tension of the liquid solder tends to draw the tags of the device towards the centre of the soldering area and has thus a correcting effect on slight mispositionings. However, if the layout leaves something to be desired the same effect can result in undesirable shifts; particularly if the soldering areas on the substrate and the components are not concentrally arranged. This problem can be solved using a standard contact pattern, which leaves sufficient scope for the self-positioning effect (see Figs 4 and 5).

After cooling the connections may be visually inspected and, where necessary, repaired with a light soldering iron. Finally any remaining flux must be removed carefully.

WAVE SOLDERING

The normal (dual) wave soldering process can also be aplied to SOT-23 and SOT-143 envelopes
We do not recommend SOT-89 for wave soldering.

IMMERSION SOLDERING

Where a complete substrate or printed circuit board is immersed in solder:

a. The temperature of the soldering bath should not exceed 280 °C.
b. The duration of the soldering cycle should not exceed 10 seconds.
c. Forced cooling may be applied (see Fig. 1).

HAND SOLDERING

It is possible to solder microminiature devices with a light hand-held soldering iron, but this method has obvious drawbacks and should therefore be restricted to laboratory use and/or incidental repairs on production circuits.

1. It is time-consuming and expensive.
2. The device cannot be positioned accurately and therefore the connecting tags may come into contact with the substrate and damage it.
3. There is a great risk of breaking either substrate or even internal connections inside the encapsulation.
4. The envelope may be damaged by the iron.

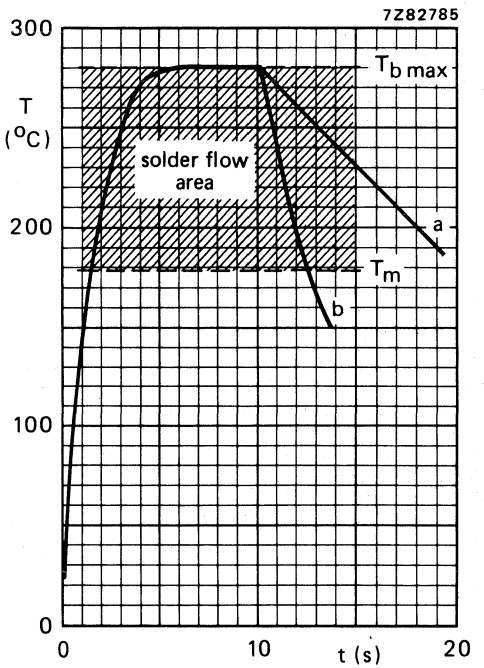
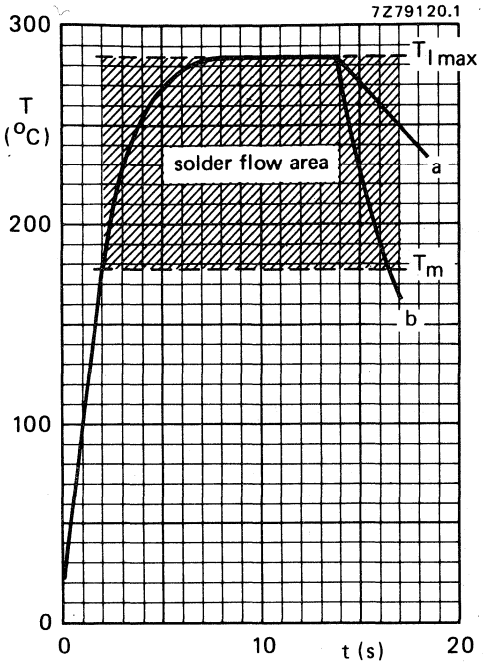


Fig. 1 Device temperature during *immersion* soldering.

Maximum time of immersion in soldering bath is 10 seconds at an ambient temperature of 25 °C.
a = free convection cooling; b = forced cooling.
$T_{b\ max}$ = maximum bath temperature (280 °C).
T_m = melting temperature of solder (179 °C).



a = free convection cooling.

b = permissible forced cooling.

$T_{l\,max}$ = Maximum lead or tab temperature = 285 °C.

T_m = Melting point of the solder is 179 °C.

T_{amb} = 25 °C.

Time of heat supply:
without preheating max. 14 s
with preheating max. 10 s

Maximum time of preheating 45 s

Fig. 2 Reflow soldering without preheating.

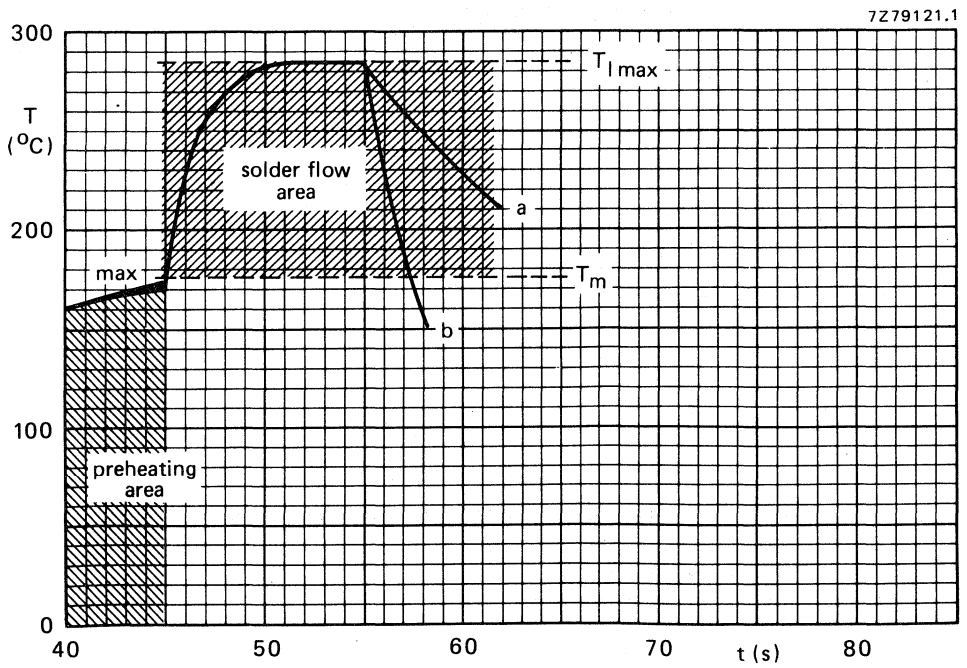


Fig. 3 Reflow soldering with preheating.

Minimum required dimensions of metal connection pads on hybrid thick and thin-film substrates.

Dimensions in mm

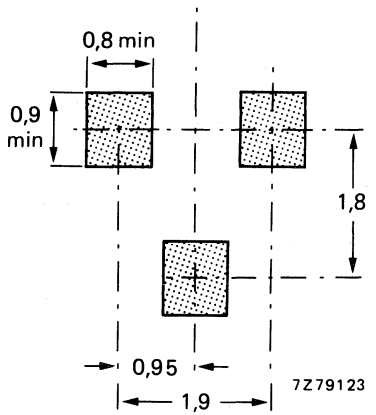


Fig. 4 SOT-23 pattern.

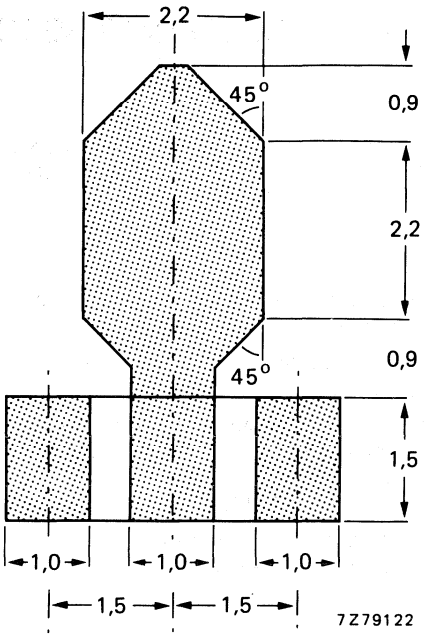


Fig. 5 SOT-89 pattern.

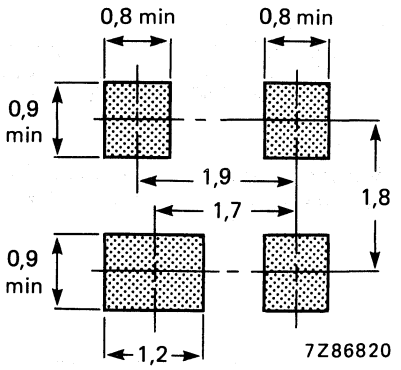


Fig. 6 SOT-143 pattern.

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

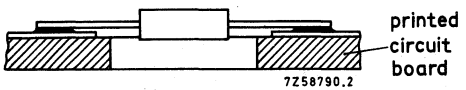


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

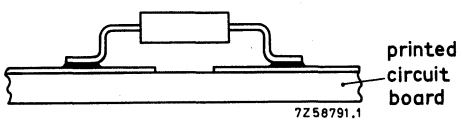


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

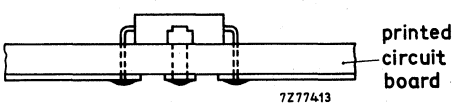


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s

THERMAL CHARACTERISTICS OF SOT-23 AND SOT-143 ENVELOPES

The heat generated in a semiconductor chip normally flows by various paths to the surroundings (ambient).

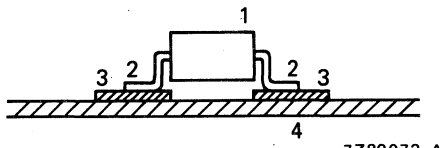


Fig. 1.

1. Heat radiation from the envelope to ambient (1).
   This heat transfer can be neglected when the envelope is mounted on a substrate or printed circuit board.
2. Heat transmission via leads (2) soldering points (3) and substrate (4).

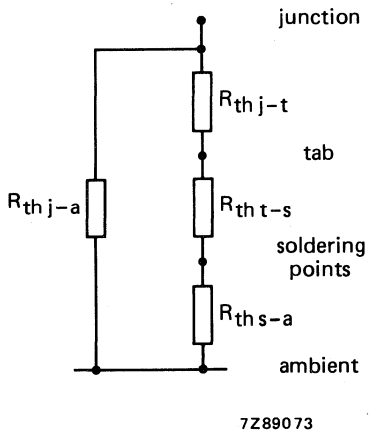


Fig. 2 Thermal behaviour of heat flow when the device is mounted on a substrate or printed-circuit board.

$R_{th\ j\text{-}t}$ = Thermal resistance from junction to tab.

$R_{th\ t\text{-}s}$ = Thermal resistance from tab to soldering points.

$R_{th\ s\text{-}a}$ = Thermal resistance from soldering points to ambient.

$R_{th\ j\text{-}a}$ = Thermal resistance from junction to ambient.

Heat transfer directly from envelope to ambient

This depends on the difference between the temperatures of envelope and the surroundings. When the device is mounted on a substrate or printed-circuit board direct heat flow can usually be neglected in relation to the heat flow via leads and substrate.
Thus the thermal model can be as in Fig. 3.

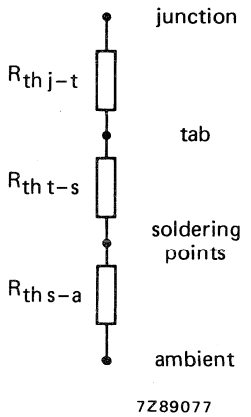


Fig. 3 Basic thermal model.

Heat transfer from junction to tab

This is an internal heat transfer and has been measured. In general it is:

for high-frequency transistors, low-power diodes and (MOS) FETs	60 K/W
for low-frequency and switching transistors	50 K/W
for low-frequency medium-power transistors	30 K/W

Heat transfer from tab to soldering points

This value has also been measured for SOT-23 with $P_{tot} < 350$ mW	280 K/W
for types of semiconductors in this envelope with $P_{tot} < 425$ mW	260 K/W
for types of semiconductors in a SOT-143 envelope this value is	310 K/W

Heat transfer from soldering points to ambient

This depends on the shape and material of tracks and substrate. In figures 4 and 5 standard mounting conditions are given to set up the maximum power ratings for SOT-23 and SOT-143 encapsulations.

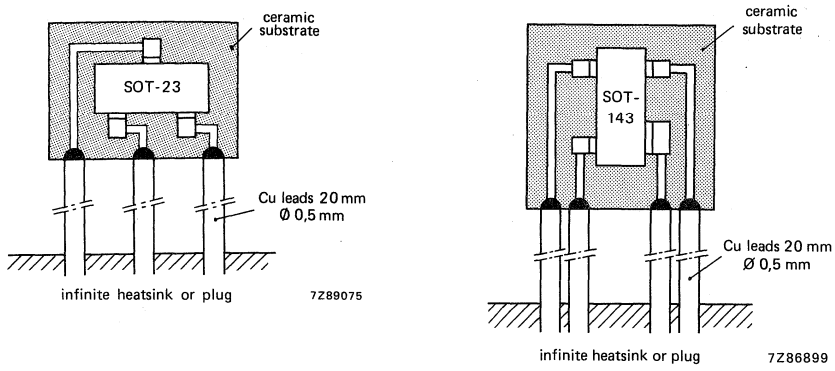


Fig. 4 Test circuits SOT-23 and SOT-143 mounting conditions on a ceramic substrate.

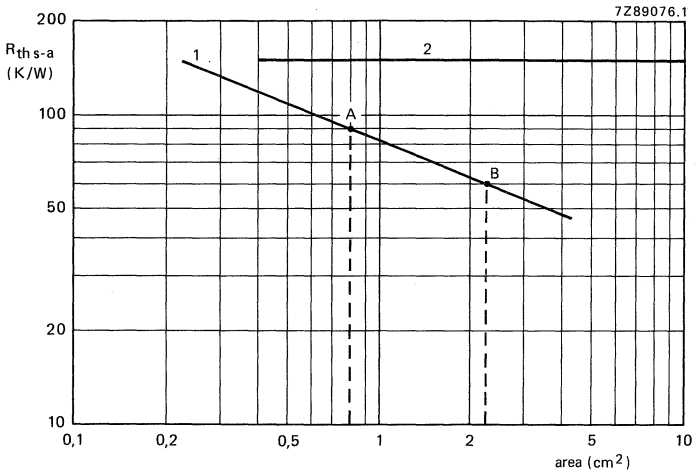


Fig. 5 Heat transfer from soldering points to ambient.

1. Ceramic substrate

Point A on the curve in Fig. 5 is for an area of the ceramic substrate of 8 mm x 10 mm x 0,7 mm for the maximum rating of all high-frequency, low-frequency and switching transistors and also for all diodes.
Point B on the curve in Fig. 5 is for an area of the ceramic substrate of 15 mm x 15 mm x 0,7 mm for the maximum rating of low-frequency medium-power semiconductors.

2. Printed-circuit board

$R_{th\ s\text{-}a}$ = 150 K/W for SOT-23 and SOT-143 envelopes mounted on a printed-circuit board.

The values for the thermal resistance from junction to tab, and tab to soldering points, are mentioned on page 2 and Fig. 5.
The formula for devices in SOT-23 with one crystal can be generalized:

$$T_j = P\,(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$$

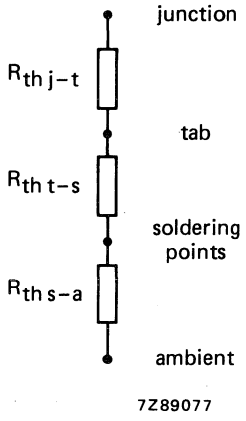


Fig. 6 Thermal model of SOT-23 envelopes with one crystal.

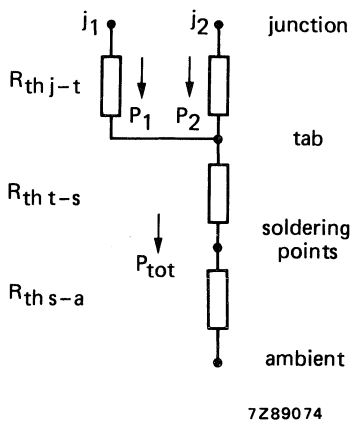


Fig. 7 Thermal model of SOT-23 envelopes with two crystals (double diode).

The formulae for devices with two crystals (double diodes) are:

$$T_{tab} = P_{tot} \cdot (R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb} = P_{tot}\,(280 + 90) + T_{amb}$$

$$T_{j1} = (P_1 \times R_{th\ j\text{-}t}) + T_{tab} = P_1 \cdot 60 + T_{tab}$$

$$T_{j2} = (P_2 \times R_{th\ j\text{-}t}) + T_{tab} = P_2 \cdot 60 + T_{tab}$$

As mentioned on page 2:

$R_{th\ j\text{-}t}$ for diodes is 60 K/W.

$R_{th\ s\text{-}a}$ (area 8 mm x 10 mm x 0,7 mm) = 90 K/W.

$R_{th\ t\text{-}s}$ for all semiconductors in SOT-23 = 280 K/W.

Thus:

$$T_{j1} = 60\,P_1 + 370\,P_{tot} + T_{amb}.$$

$$T_{j2} = 60\,P_2 + 370\,P_{tot} + T_{amb}.$$

DEVICE DATA
J-FETs

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for hi-fi amplifiers and other audio-frequency equipment.

QUICK REFERENCE DATA

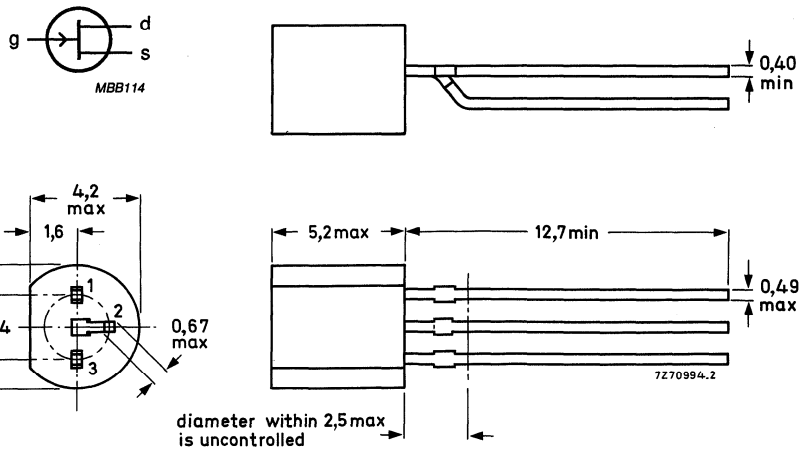
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 °C
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 12 mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|Y_{fs}\|$	typ.	3,5 mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 1 kHz; R_G = 1 MΩ	F	<	2 dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}	−65 to +150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	250	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	5	5	5	5	nA
Drain current							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 µA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\lvert y_{fs} \rvert$	>	2,5	3,0	3,5	4,0	mS
V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz							
Input capacitance	C_{is}		typ.	4,0			pF
Feedback capacitance	C_{rs}		typ.	1,2			pF
Output capacitance	C_{os}		typ.	1,6			pF
Noise figure at f = 1 kHz; R_G = 1 MΩ							
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C	F		typ.	0,5			dB
		<		2			dB
Equivalent noise voltage at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n/\sqrt{B}$		typ.	40			nV/$\sqrt{\text{Hz}}$

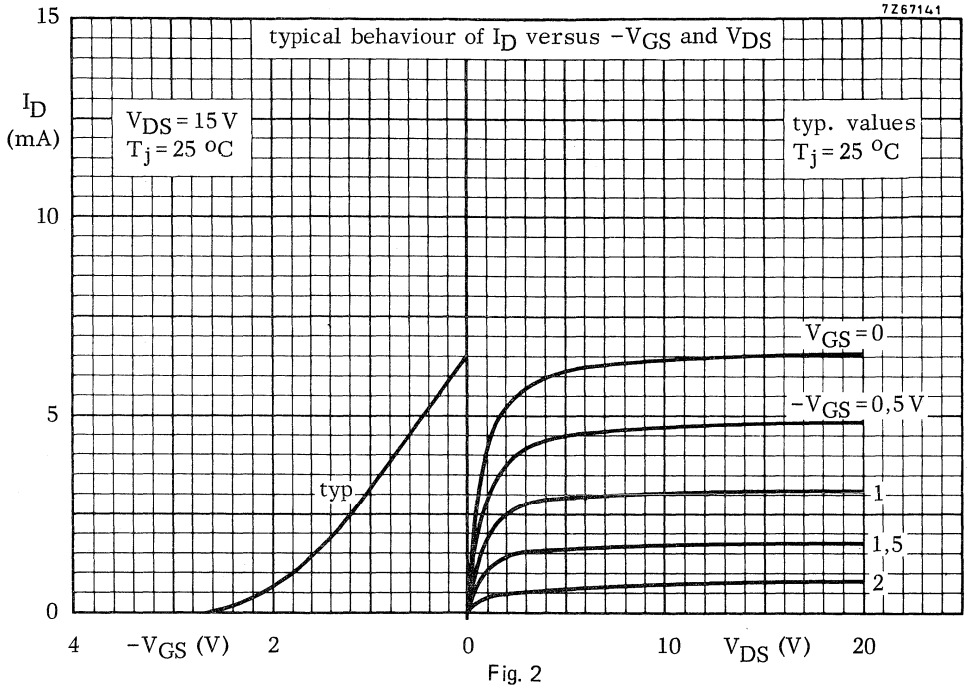


Fig. 2

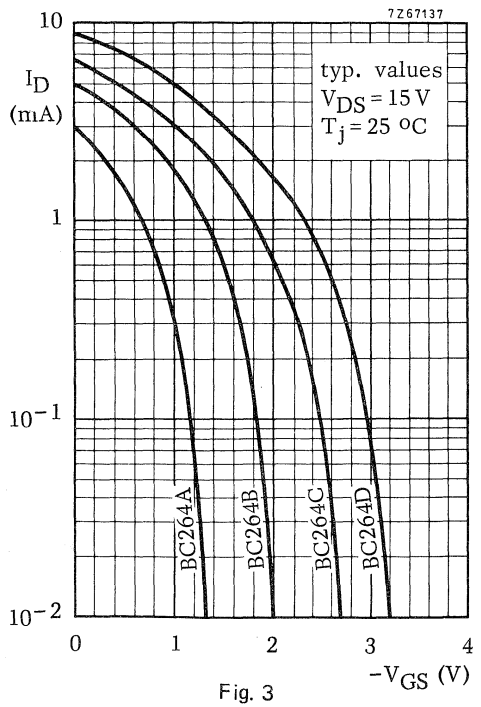


Fig. 3

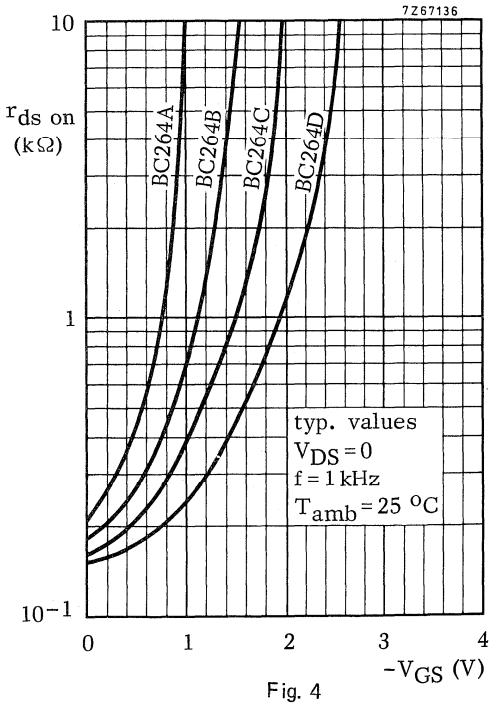


Fig. 4

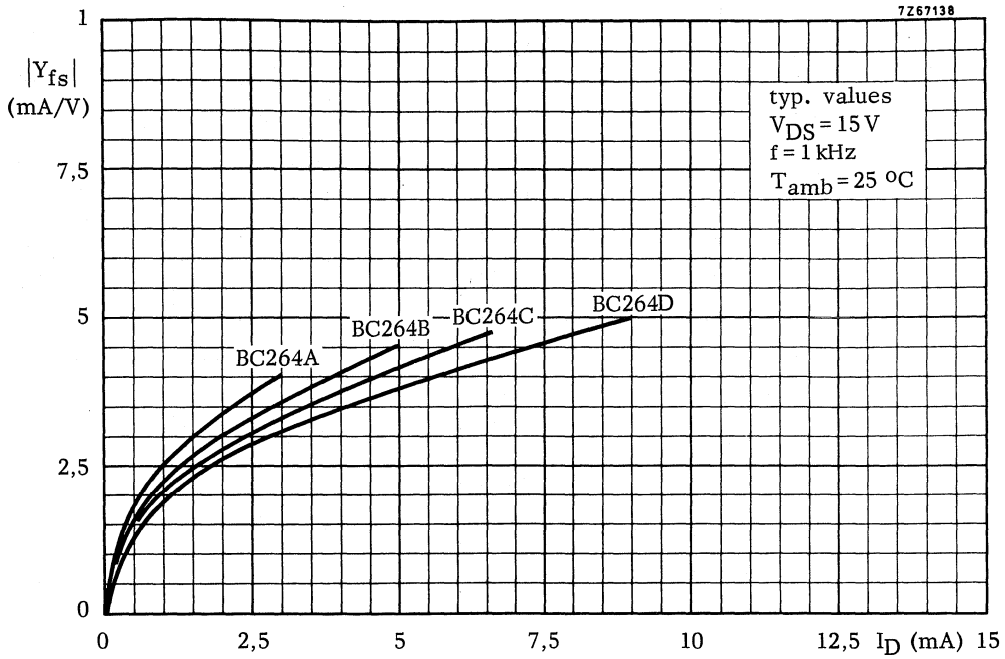


Fig. 5

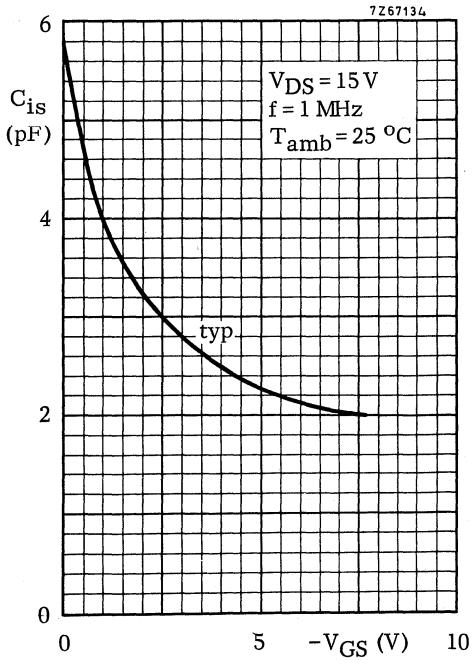


Fig. 6

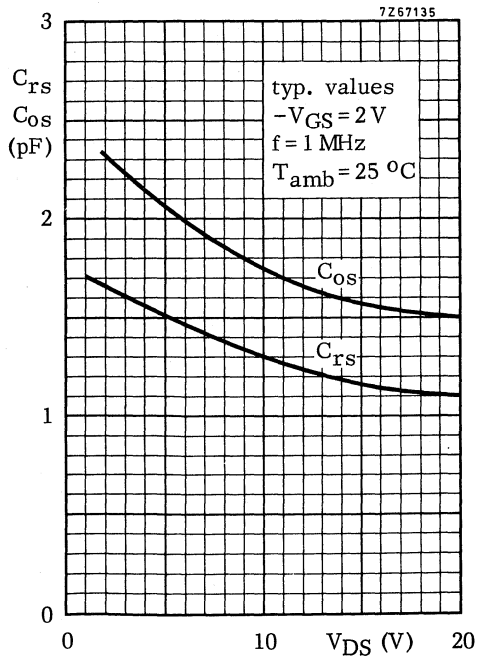


Fig. 7

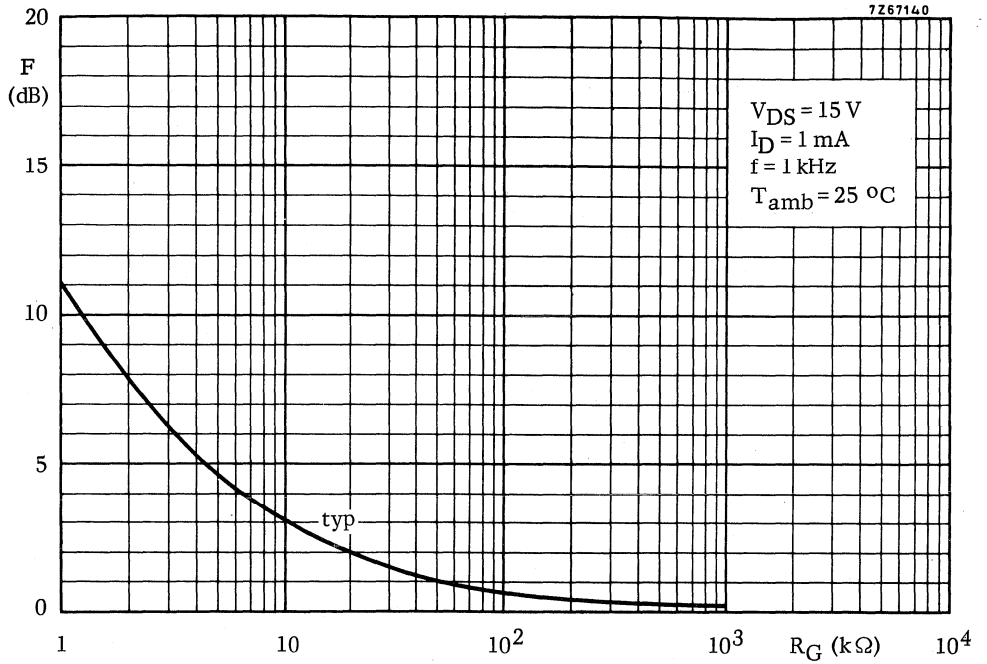

7Z67140
20
F
(dB)
15
10
5
0
typ
V_{DS} = 15 V
I_D = 1 mA
f = 1 kHz
T_{amb} = 25 °C
1
10
10^2
10^3
R_G (kΩ)
10^4

Fig. 8

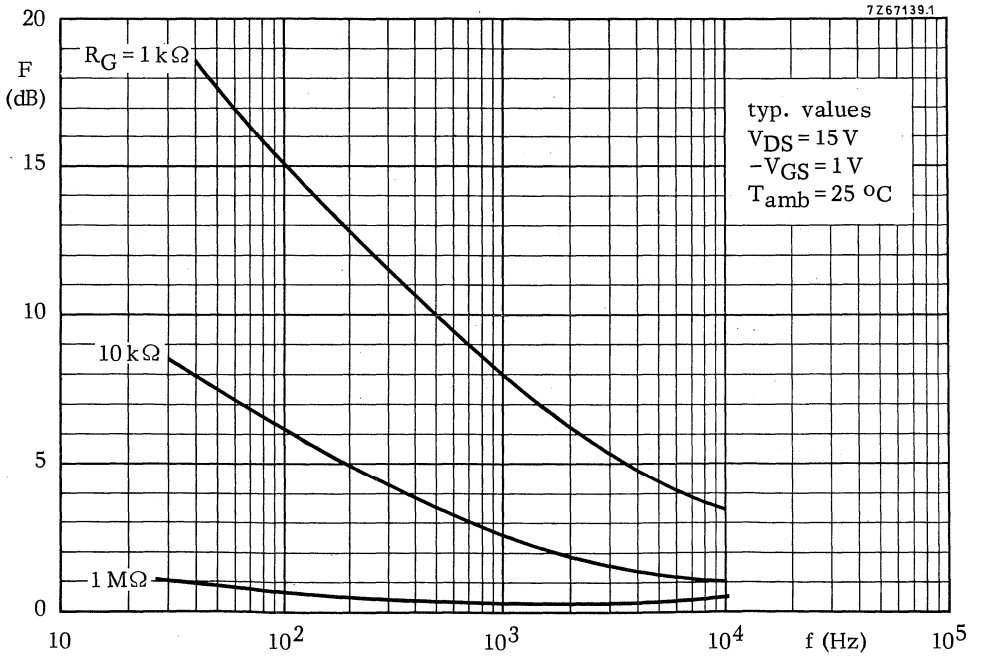

7Z67139.1
20
F
(dB)
15
10
5
0
R_G = 1 kΩ
10 kΩ
1 MΩ
typ. values
V_{DS} = 15 V
$-V_{GS}$ = 1 V
T_{amb} = 25 °C
10
10^2
10^3
10^4
f (Hz)
10^5

Fig. 9

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

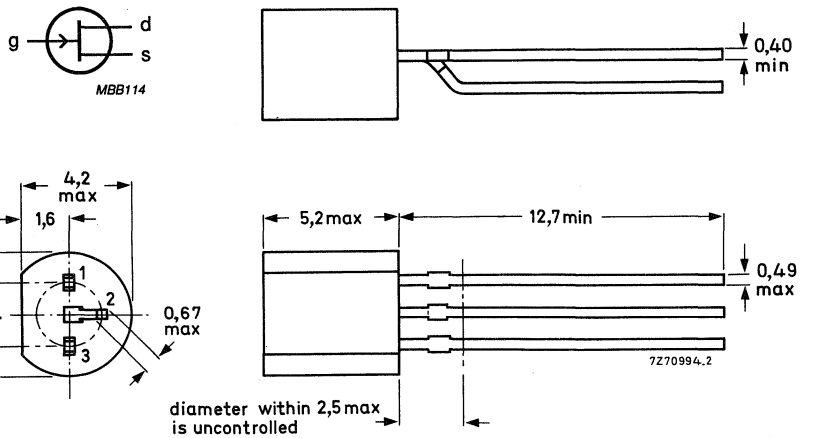
Drain-source voltage	$\pm V_{DS}$			max. 30		V
Gate-source voltage (open drain)	$-V_{GSO}$			max. 30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}			max. 300		mW
		BF245A/0	A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 0,5	2,0	6	12	mA
		< 2,1	6,5	15	25	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,25 to 8,0		V
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}			typ. 1,1		pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|Y_{fs}\|$			3,0 to 6,5		mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	25 mA
Gate current	I_G	max.	10 mA
Power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5	μA
Drain current 2)					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	> 2	6,0	12	mA
		< 6,5	15,0	25	mA
Gate-source breakdown voltage					
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30	V
Gate-source voltage					
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)	> 0,4	1,6	3,2	V
		< 2,2	3,8	7,5	V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF245A/0: I_{DSS} = 0,5 to 2,1 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 1,9 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

Gate-source cut-off voltage				
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0	V
y-parameters at T_{amb} = 25 °C (common source)				
V_{DS} = 15 V; V_{GS} = 0				
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5	mS
	Output admittance	$\|y_{os}\|$	typ. 25	μS
f = 200 MHz	Input conductance	g_{is}	typ. 250	μS
	Reverse transfer admittance	$\|y_{rs}\|$	typ. 1,4	mS
	Transfer admittance	$\|y_{fs}\|$	typ. 6	mS
	Output conductance	g_{os}	typ. 40	μS
V_{DS} = 20 V; $-V_{GS}$ = 1 V				
f = 1 MHz	Input capacitance	C_{is}	typ. 4,0	pF
	Feedback capacitance	C_{rs}	typ. 1,1	pF
	Output capacitance	C_{os}	typ. 1,6	pF
Cut-off frequency *				
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ. 700	MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)				
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ. 1,5	dB

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

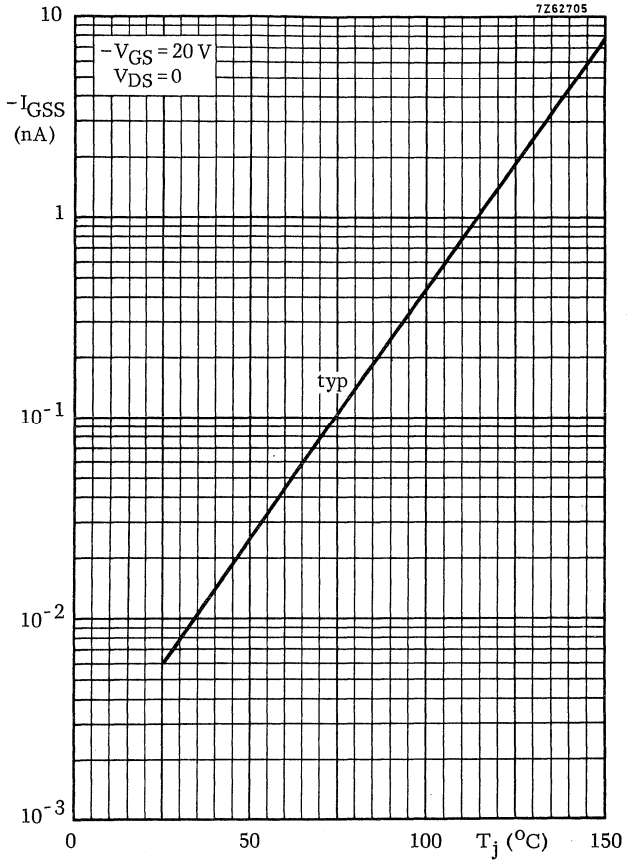

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (^oC)
150

Fig. 2

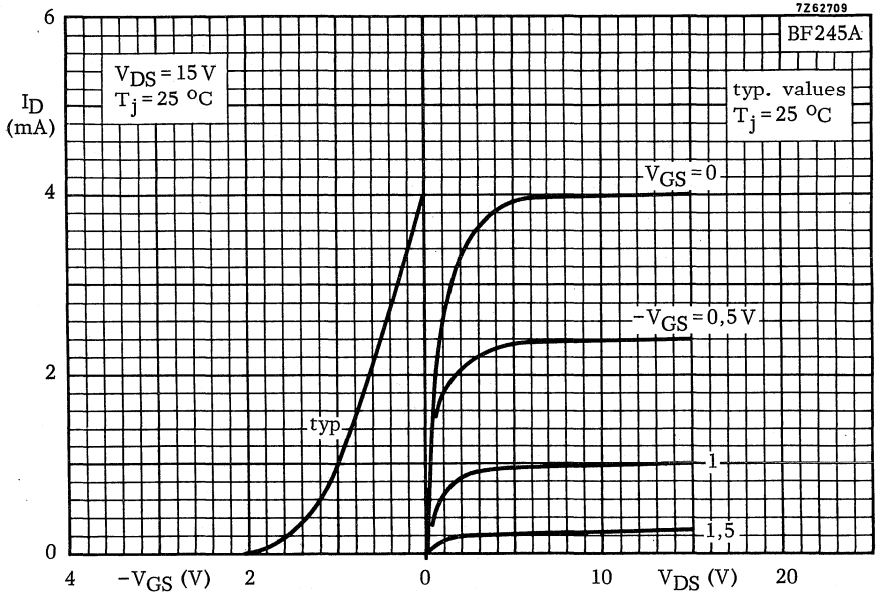

7Z62709
BF245A
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

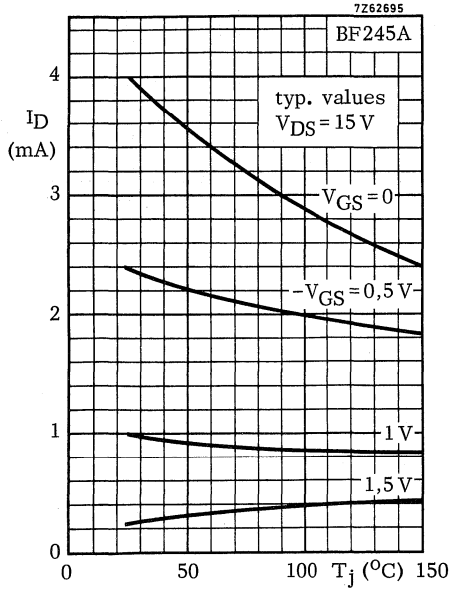

7Z62695
BF245A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
4
3
2
1
0
0
50
100
T_j (°C)
150

Fig. 4

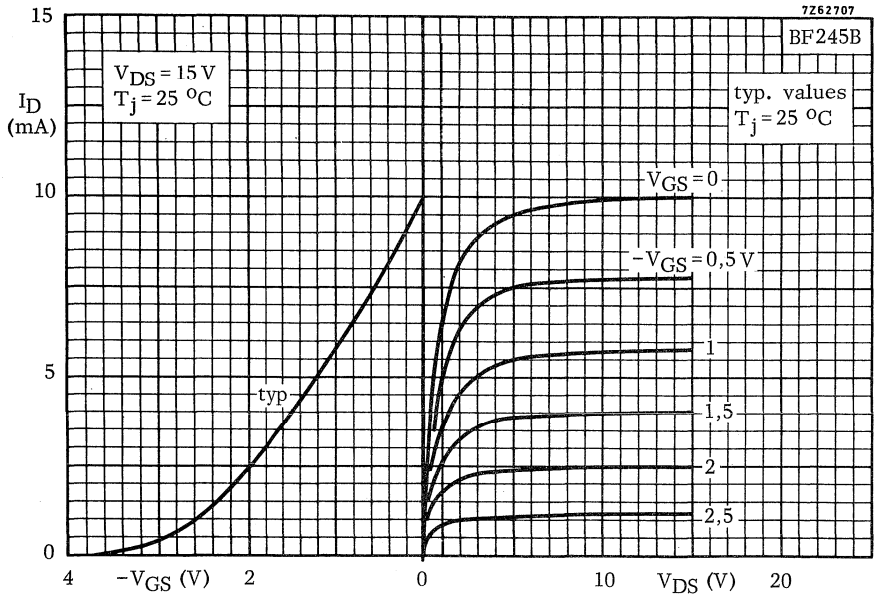

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

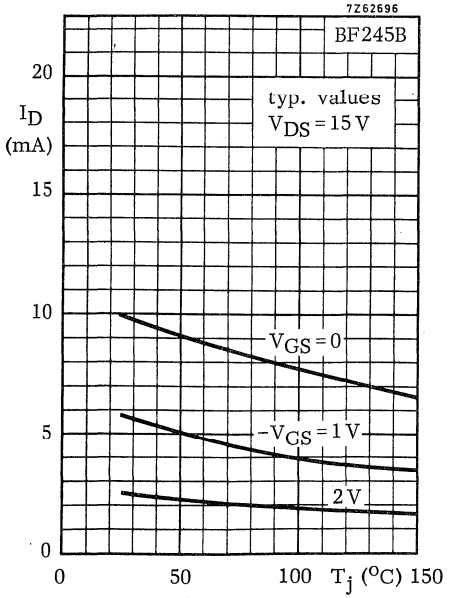

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

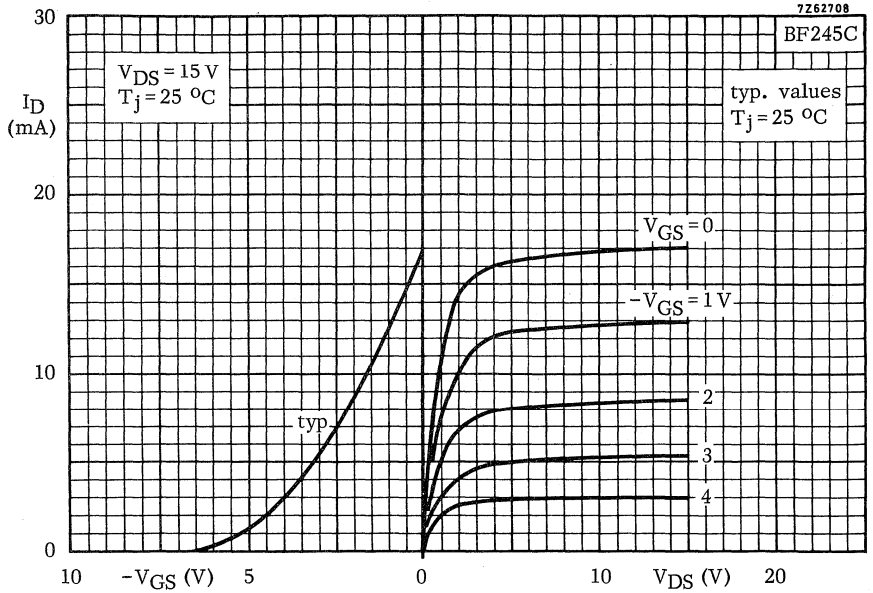

7Z62708
BF245C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
30
20
10
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

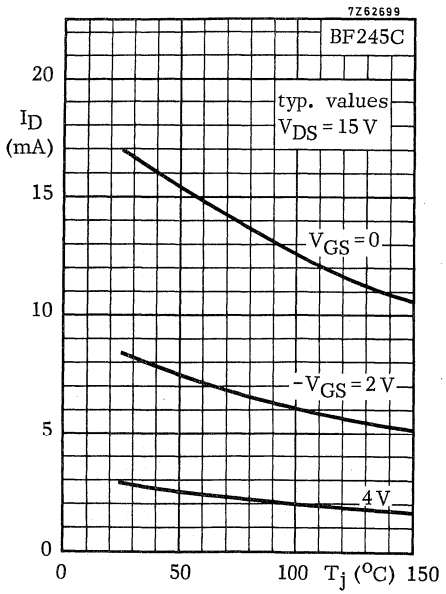

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

Fig. 8

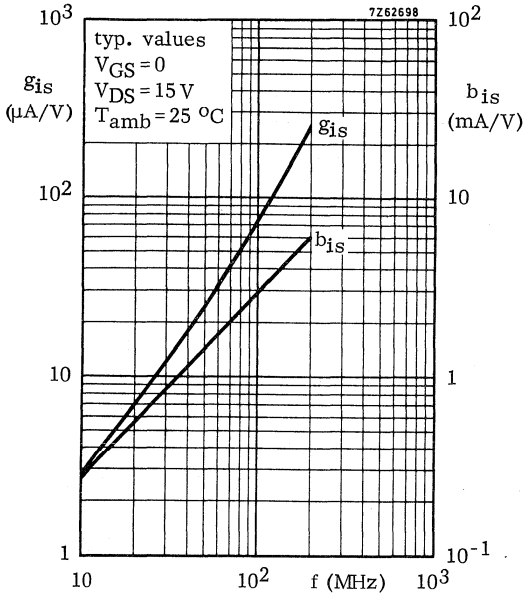

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
g_{is}
b_{is}
g_{is} (μA/V)
b_{is} (mA/V)
10^3
10^2
10
1
10^{-1}
f (MHz)

Fig. 9

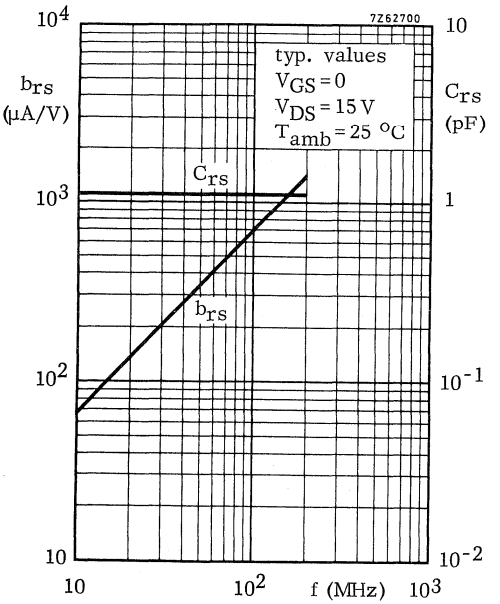

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
C_{rs}
b_{rs}
b_{rs} (μA/V)
C_{rs} (pF)
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
f (MHz)

Fig. 10

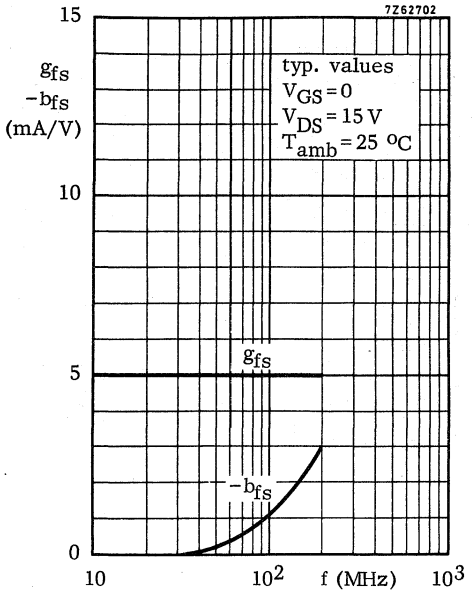

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

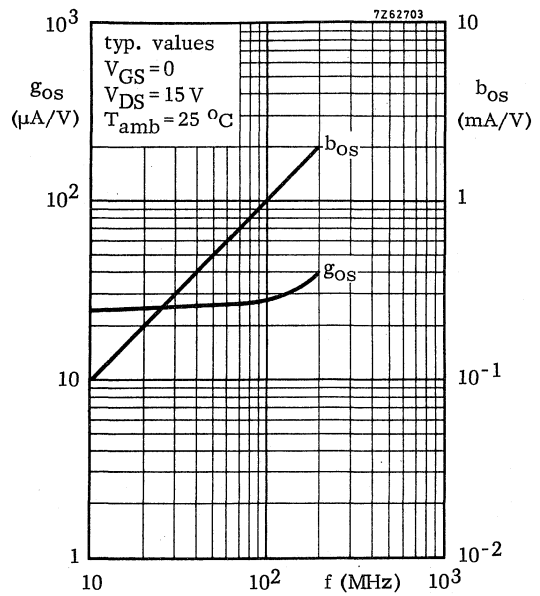

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
b_{os}
(mA/V)
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 12

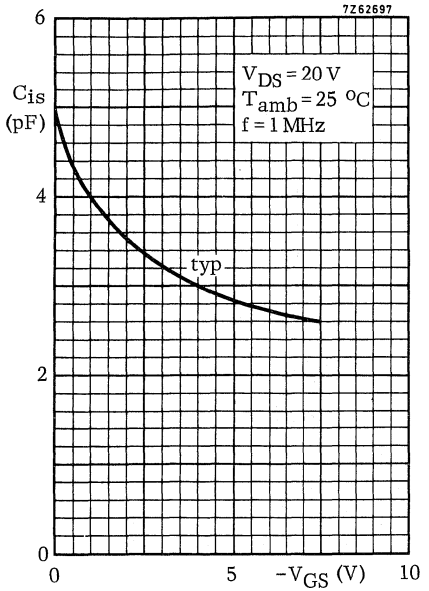


Fig. 13

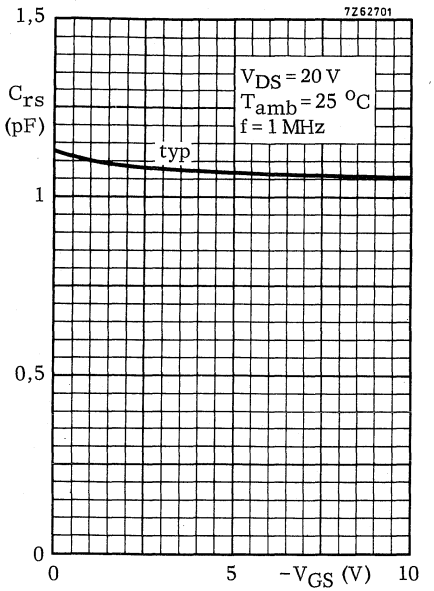


Fig. 14

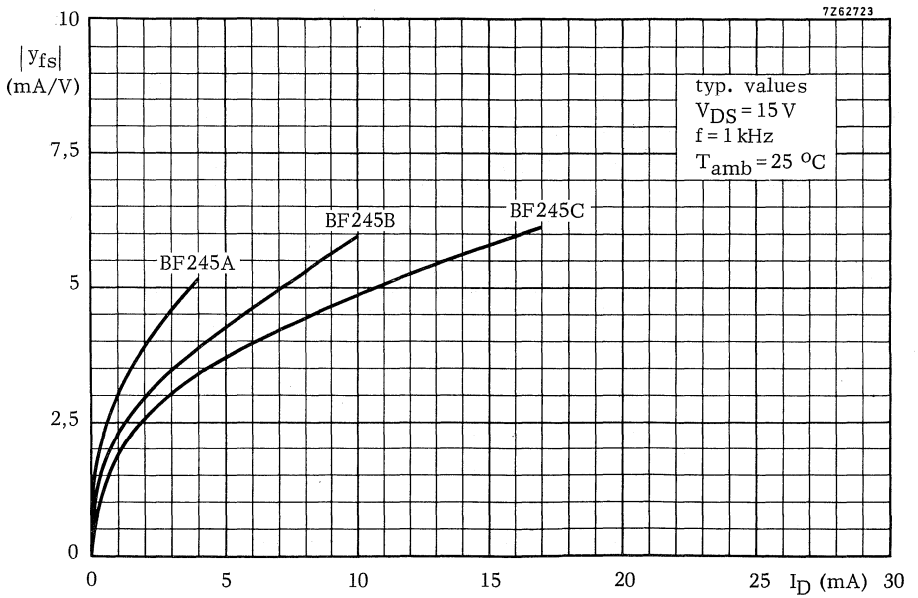


Fig. 15

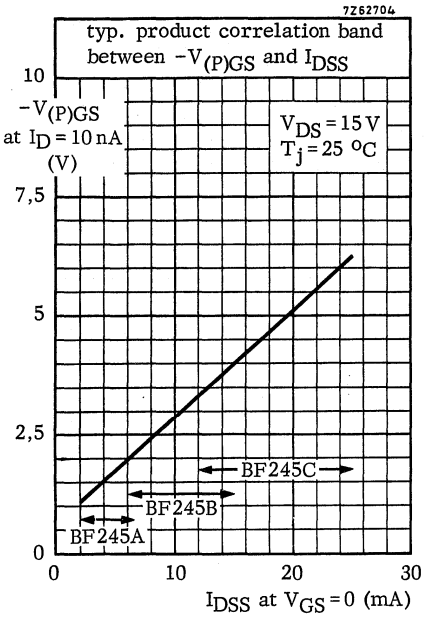


Fig. 16

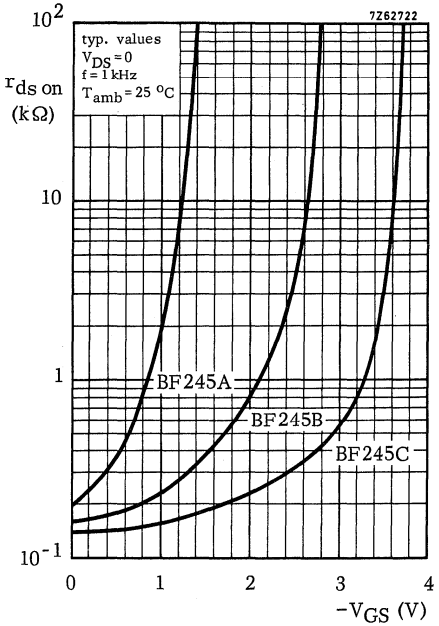


Fig. 17

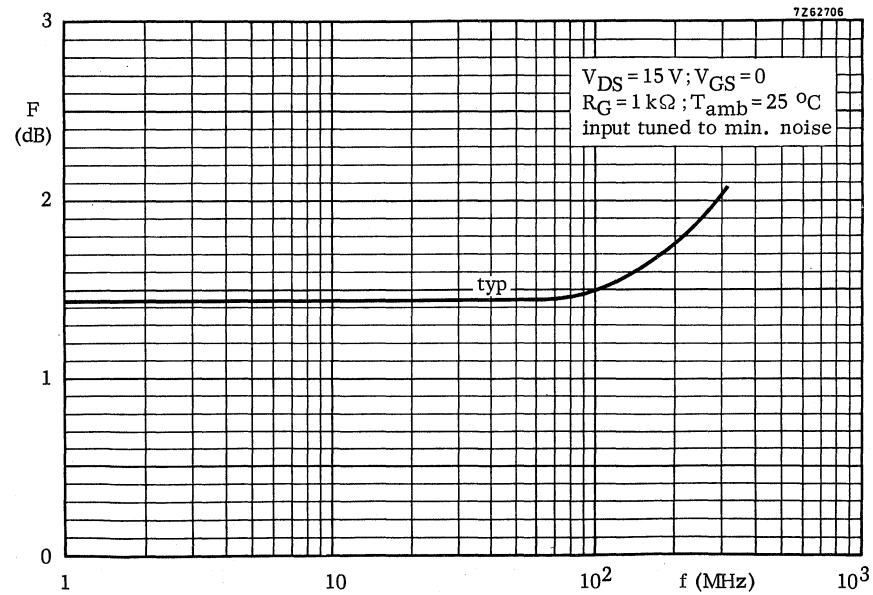


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for VHF and UHF amplifiers, mixers and general purpose switching.

QUICK REFERENCE DATA

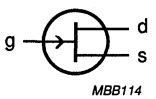
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
			A	B	C	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$				0.6 to 14.5	V
Feedback capacitance at f = 1 MHz						
I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3.5	pF
Transfer admittance (common source)						
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	min.			8	mS

MECHANICAL DATA

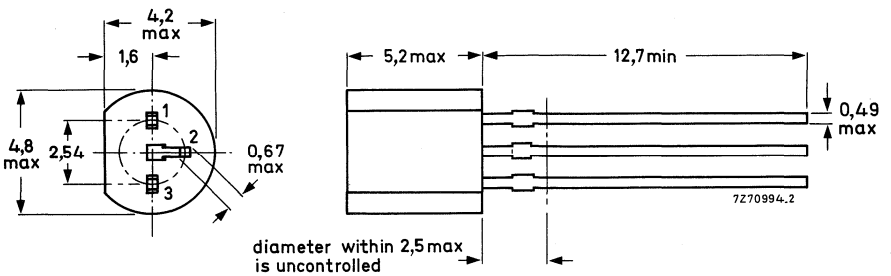
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning (BF246):
1 = drain
2 = gate
3 = source



Pinning (BF247):
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

T_{amb} = 25 °C

			A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	min.	1.5	3.0	5.5	V
		max.	4.0	7.0	12.0	V
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0.6 to 14.5		V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	min.			8	mS
		typ.			17	mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V						
feed-back capacitance	C_{rs}	typ.			3.5	pF
input capacitance	C_{is}	typ.			11	pF
output capacitance	C_{os}	typ.			5	pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.			450	MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0.02$.
** The frequency at which g_{fs} is 0.7 of its value at 1 kHz.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA

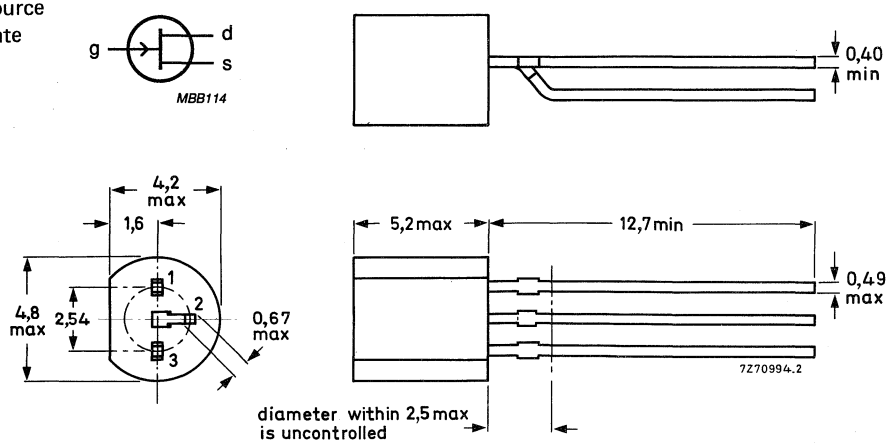
Drain-source voltage	$\pm V_{DS}$		max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$		max.	30	V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}		max.	300	mW
		BF256A | B | C			
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>3 | 6 | 11			mA
		<7 | 13 | 18			mA
Feedback capacitance at f = 1 MHz					
V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}		typ.	0,7	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|y_{fs}\|$		>	4,5	mS
Power gain at f = 800 MHz					
V_{DS} = 15 V; R_S = 47 Ω	G_p		typ.	11	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning;
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C	P_{tot}	max.	300 mW 1)
Storage temperature	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200 K/W 1)

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<			5	nA
			BF256A	B	C	
Drain current 2)						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	>	3	6	11	mA
		<	7	13	18	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>			30	V
Gate-source voltage						
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)				0,5 to 7,5	V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF256B/1: I_{DSS} = 6 to 8 mA; $-V_{GS}$ = 1,4 to 2,6 V.

y-parameters (common source)				
Transistor admittance at f = 1 kHz				
V_{DS} = 15 V; V_{GS} = 0	$\|y_{fs}\|$	>	4,5 mS	1)
		typ.	5 mS	1)
Output capacitance at f = 1 MHz				
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.	1,2 pF	
Feedback capacitance at f = 1 MHz				
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.	0,7 pF	
Cut-off frequency				
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	1 GHz	2)
Noise figure at f = 800 MHz				
V_{DS} = 10 V; R_S = 47 Ω	F	typ.	7,5 dB	
Power gain at f = 800 MHz				
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11 dB	

1) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

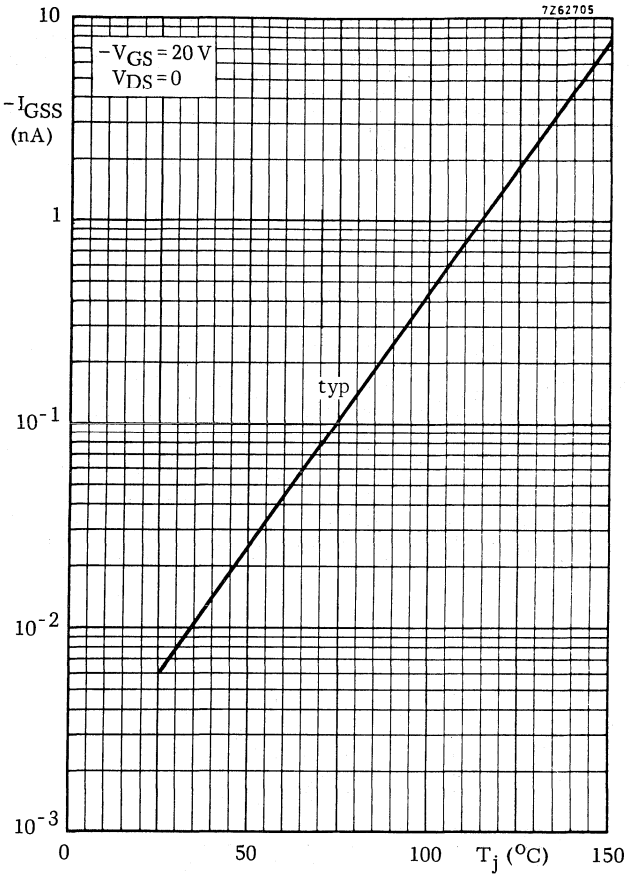

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

Fig. 2

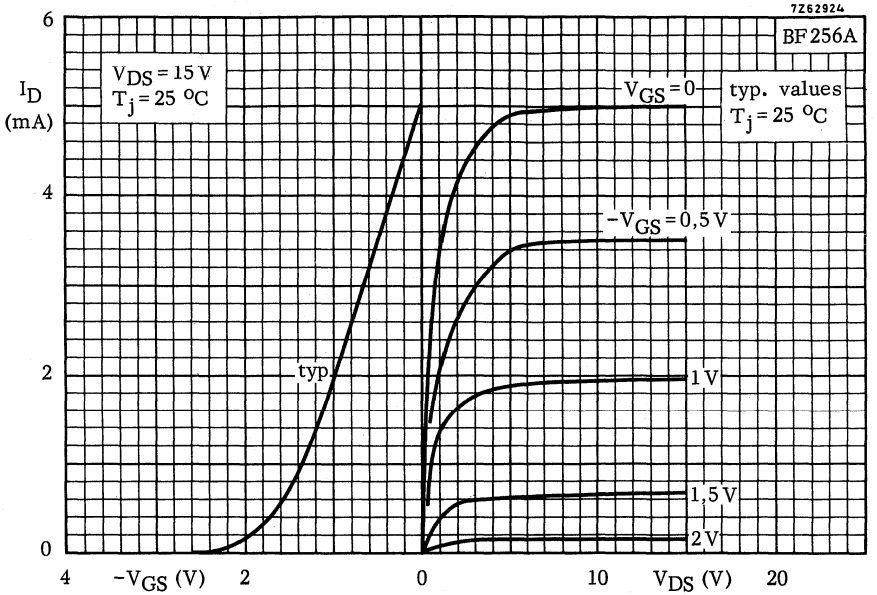

7Z62924
BF256A
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
typ.
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

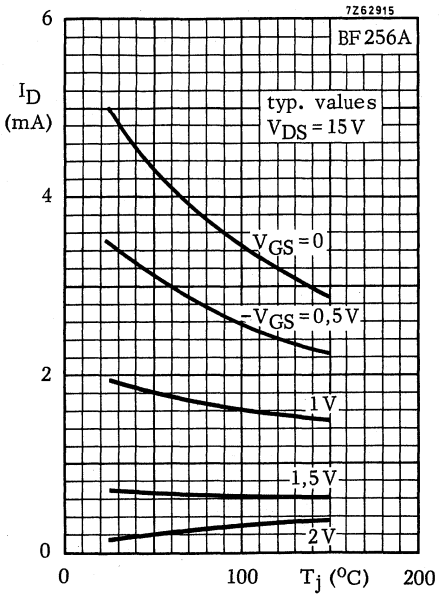

7Z62915
BF256A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
6
4
2
0
0
100
T_j (°C)
200

Fig. 4

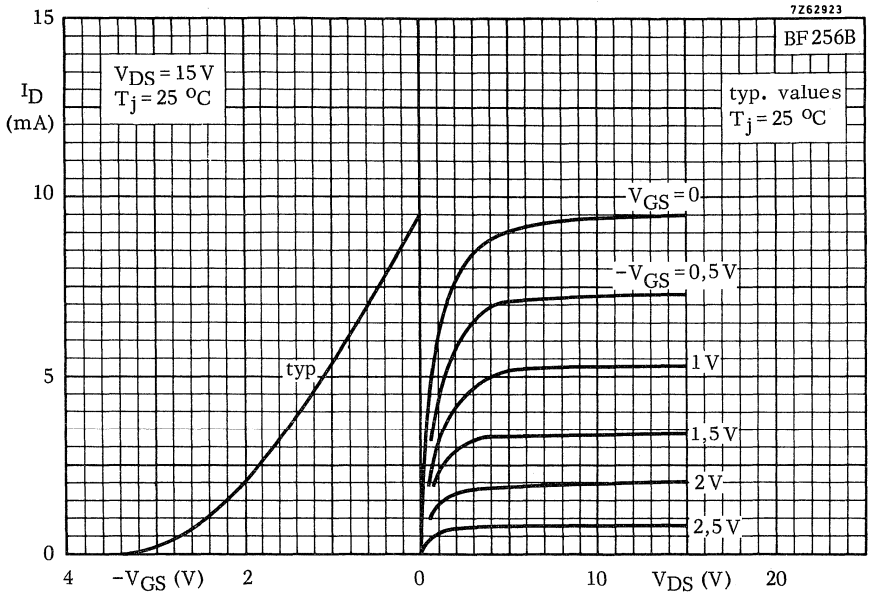

7Z62923
BF256B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
$-V_{GS}$ = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
2,5 V
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

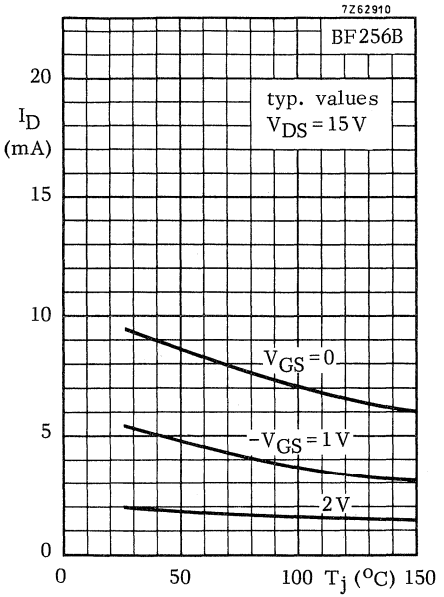

7Z62910
BF256B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

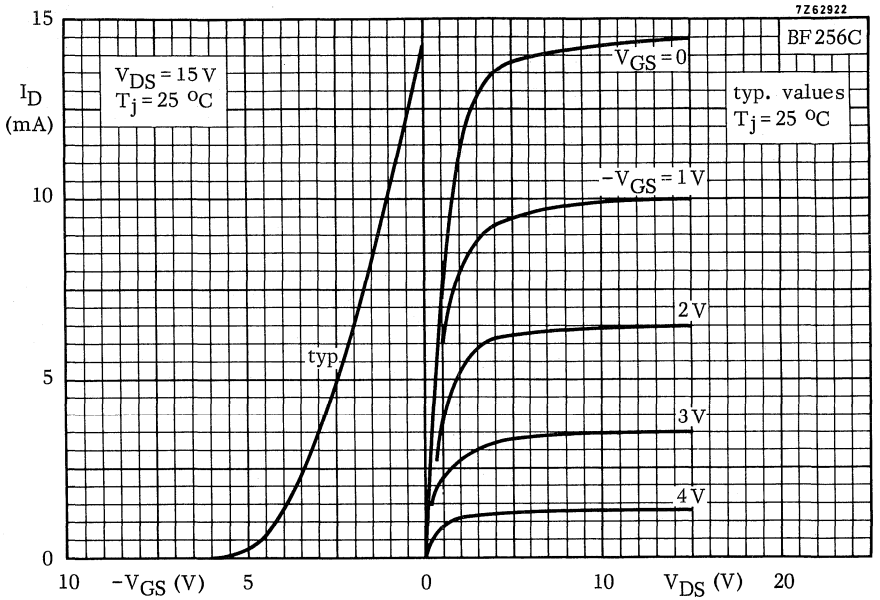

7Z62922
BF256C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
3 V
4 V
typ.
15
10
5
0
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

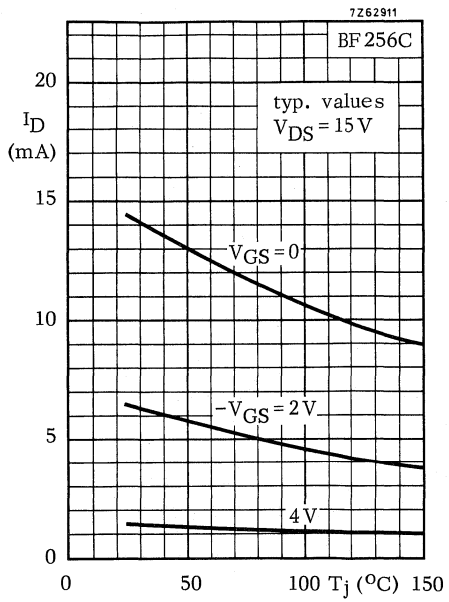

7Z62911
BF256C
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
20
15
10
5
0
0
50
100 T_j (°C)
150

Fig. 8

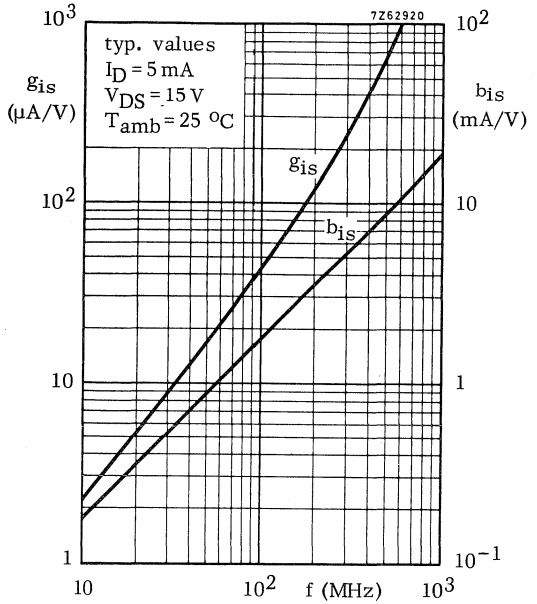

7Z62920
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
f (MHz)

Fig. 9

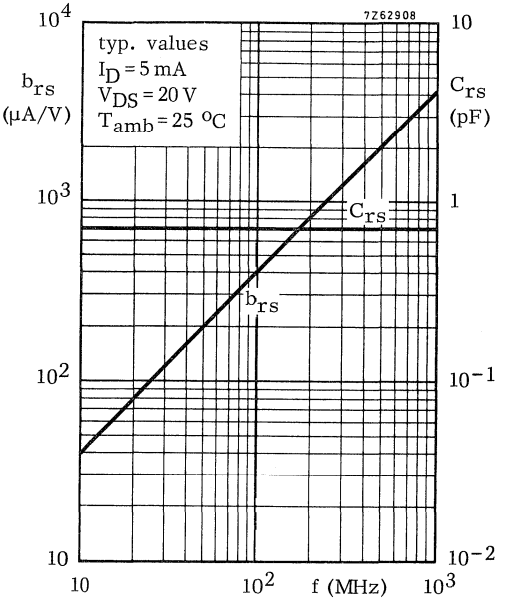

7Z62908
typ. values
I_D = 5 mA
V_{DS} = 20 V
T_{amb} = 25 °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
f (MHz)

Fig. 10

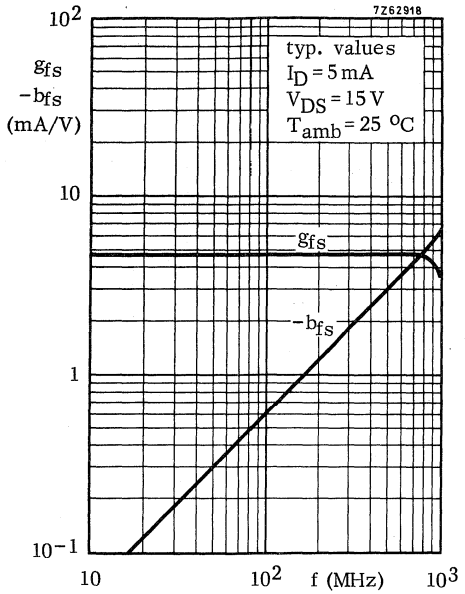

7Z62918
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{fs}
$-b_{fs}$
(mA/V)
10^2
10
1
10^{-1}
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

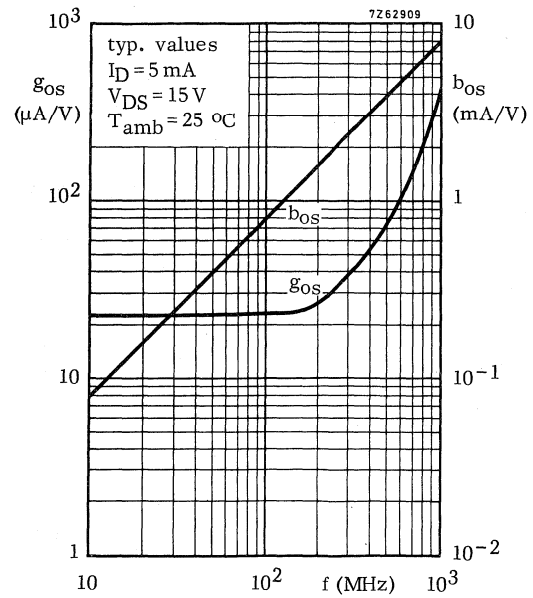

7Z62909
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{os}
(μA/V)
b_{os}
(mA/V)
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

Fig. 12

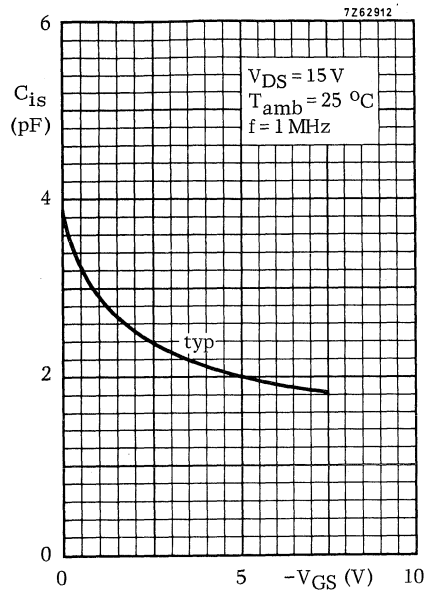


Fig. 13

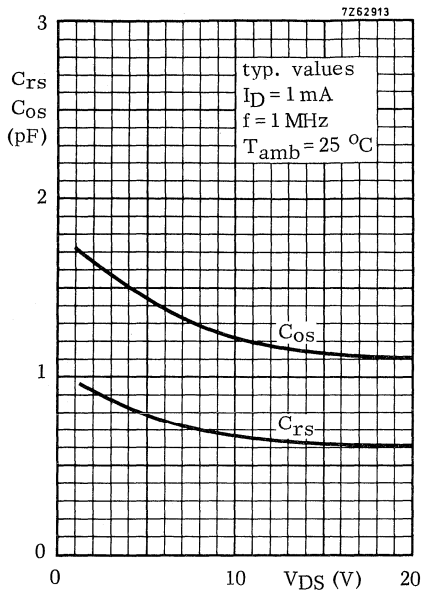


Fig. 14

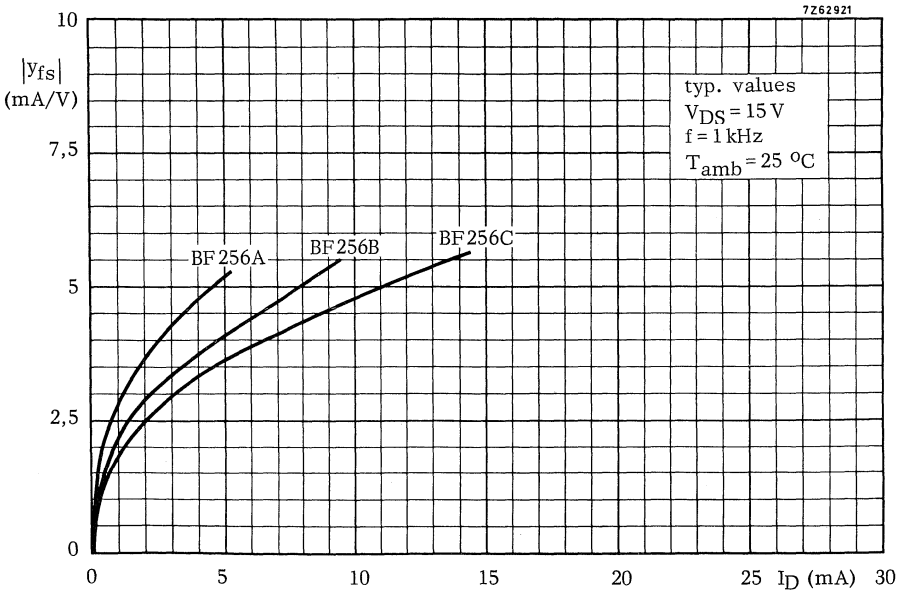


Fig. 15

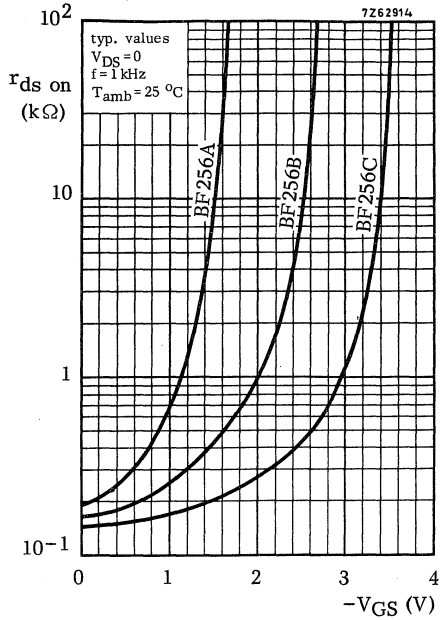


Fig.16

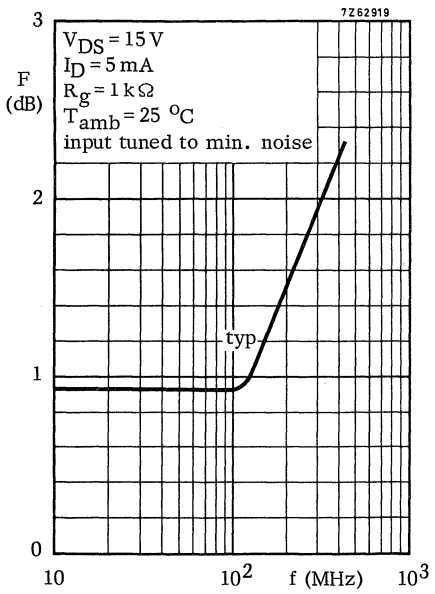


Fig. 17

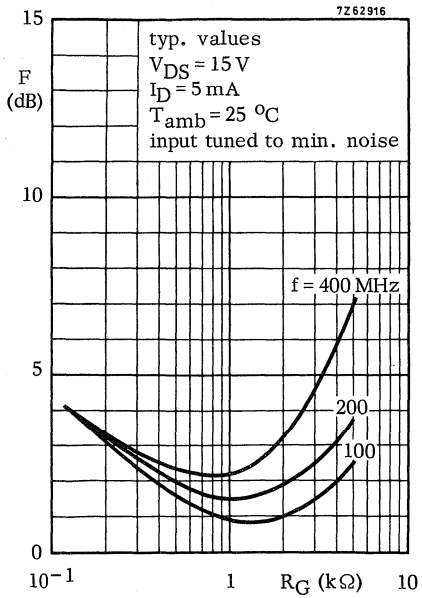


Fig.18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications up to the VHF range.
These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the RF stages in FM portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

QUICK REFERENCE DATA

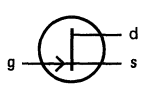
Drain-source voltage	V_{DS}	max.		20			V
Drain current (DC or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.		300			mW
			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Transfer admittance V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.5	0.5	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0.5	0.5	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1.5	1.5	dB

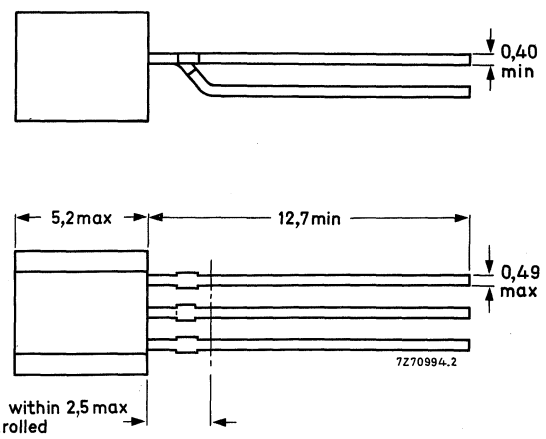
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	max.	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	min.	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	0.7	2.5	6	10	mA
		max.	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and **B**
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	max.	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.5	0.5	0.5	0.5	pF
		max.	0.7	0.7	0.7	0.7	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	min.	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	max.	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	max.	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

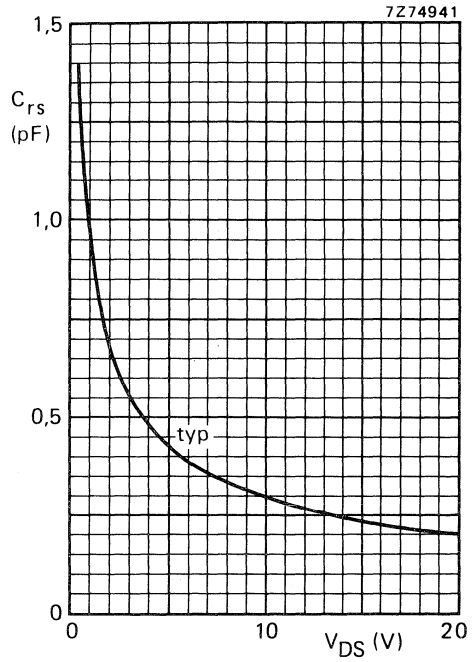


Fig. 2 V_{GS} = 0 for **BF410A** and **BF410B**; I_D = 5 mA for **BF410C** and **BF410D**; f = 1 MHz; T_{amb} = 25 °C.

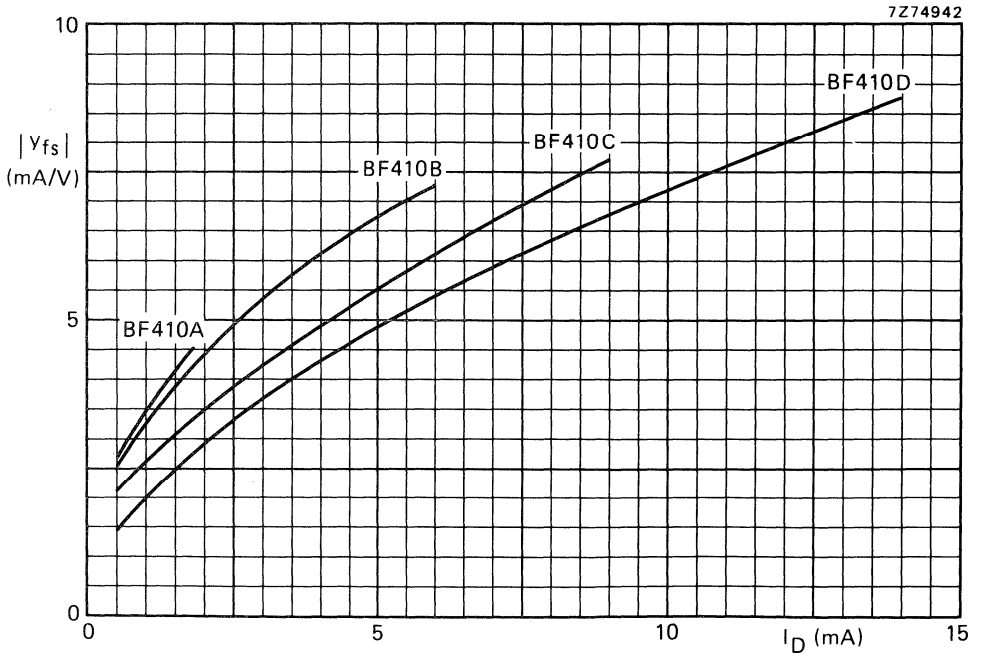


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.		20			V
Drain current (DC or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.		250			mW
			BF510	511	512	513	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2.5	4	6	7	mS
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0.3	0.3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0.3	0.3	pF
Noise figure at optimum source admittance G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz							
V_{DS} = 10 V; V_{GS} = 0	F	typ.	1.5	1.5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1.5	1.5	dB

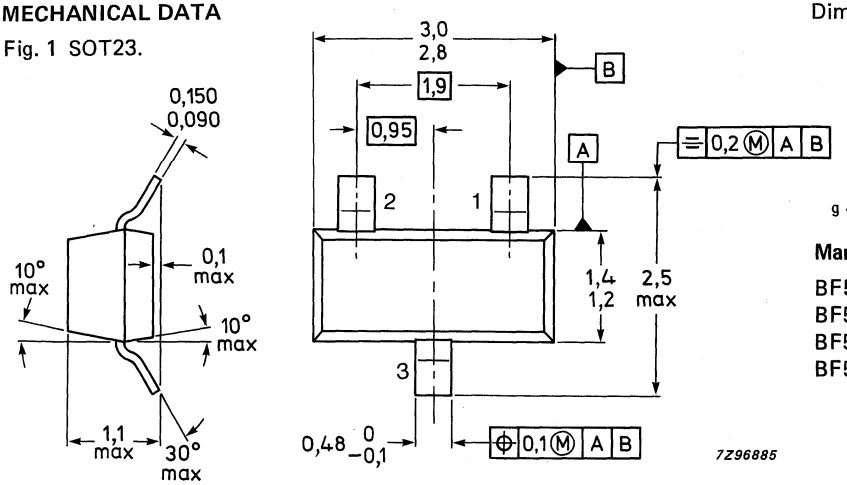
MECHANICAL DATA

SOT23.

See also *Soldering recommendations.*

MECHANICAL DATA

Fig. 1 SOT23.

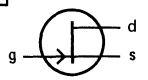


TOP VIEW

Dimensions in mm

Pinning

1 = gate
2 = drain
3 = source



Marking code

BF510 = S6p
BF511 = S7p
BF512 = S8p
BF513 = S9p

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-gate voltage (open source)	V_{DGO}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

Note

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF510	511	512	513	
Gate cut-off current							
$-V_{GS}$ = 0.2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0.7	2.5	6	10	mA
		<	3.0	7.0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for BF510 and BF511

V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for BF512 and BF513

y-parameters (common source)			BF510	511	512	513	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μS
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0.3	0.3	0.3	0.3	pF
		<	0.4	0.4	0.4	0.4	pF
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	2.5	4.0	4.0	3.5	mS
V_{GS} = 0 instead of I_D = 5 mA	$\|y_{fs}\|$	>	–	–	6.0	7.0	mS
Transfer admittance at f = 100 MHz	$\|y_{fs}\|$	typ.	3.5	5.5	5.0	5.0	mS
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μS
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μS
Noise figure at optimum source admittance							
G_S = 1 mS; $-B_S$ = 3 mS; f = 100 MHz	F	typ.	1.5	1.5	1.5	1.5	dB

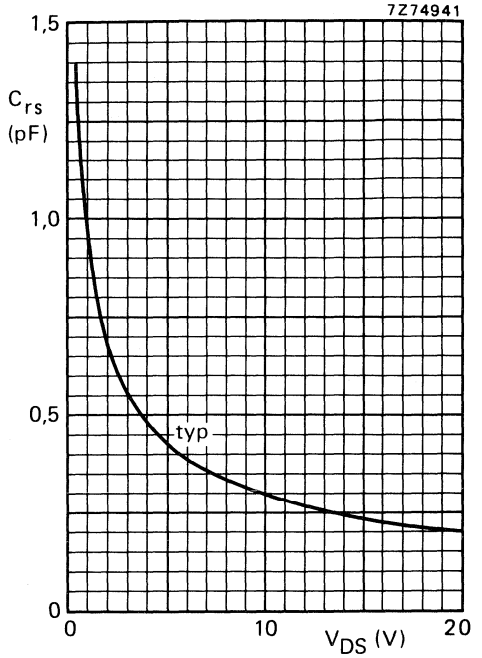


Fig. 2 V_{GS} = 0 for BF510 and BF511; I_D = 5 mA for BF512 and BF513; f = 1 MHz; T_{amb} = 25 °C.

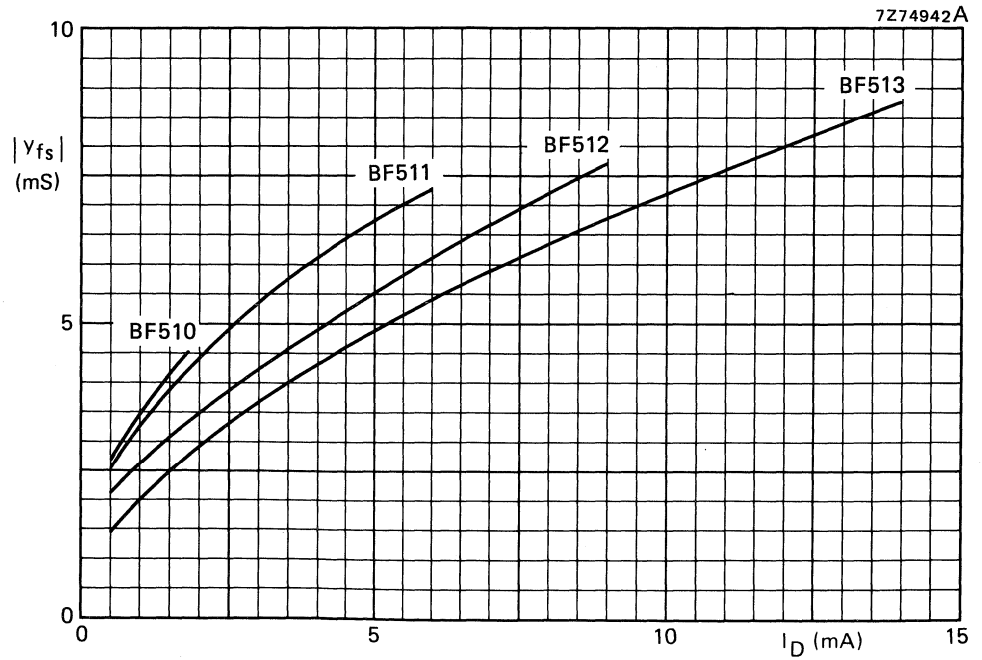


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

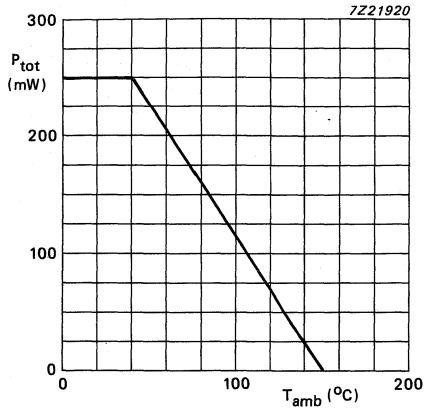


Fig.4 Power derating curve.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

		BFQ10	11	12	13	14	15	16	
Difference in gate current	$\lvert\Delta I_G\rvert$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	< 5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0.98 < 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.95 1.05	0.95 1.05	
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	< 18	30	40	50	60	70	100	μV/V
Common mode rejection ratio	CMRR	> 95	90	85	85	80	80	80	dB

MECHANICAL DATA

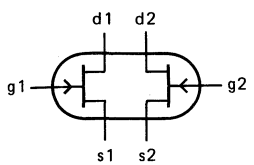
Dimensions in mm

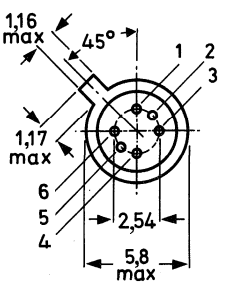
Fig. 1 TO-71.

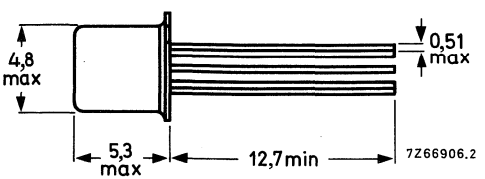
All leads insulated from the case.

Pinning

1 = source 1
2 = drain 1
3 = gate 1
4 = source 2
5 = drain 2
6 = gate 2







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500	K/W

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

Measured at: I_D = 200 μA; V_{DG} = 15 V except for drain current ratio.

			BFQ10	11	12	13	14	15	16	
Drain current ratio (note 1) V_{DG} = 15 V; V_{GS} = 0	$\frac{I_{1D\text{-}1SS}}{I_{2D\text{-}2SS}}$	>	0.97	0.95	0.95	0.95	0.92	0.90	0.80	
		<	1.03	1.05	1.05	1.05	1.08	1.10	1.20	
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0.98	0.98	0.98	0.98	0.98	0.95	0.95	
		<	1.02	1.02	1.02	1.02	1.02	1.05	1.05	
Difference in transfer impedance (note 2)	$\lvert\Delta\frac{1}{g_{fs}}\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor (note 3)	$\lvert\Delta\frac{g_{os}}{g_{fs}}\rvert$	<	18	30	40	50	60	70	100	μV/V
Common mode rejection ratio (note 4)	CMRR	>	95	90	85	85	80	80	80	dB

Notes

1. Measured under pulse conditions.
2. The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.
   $(\Delta\frac{1}{g_{fs}} = \frac{d\Delta V_{GS}}{dI_D}$ at V_{DG} = constant).
3. The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.
   $(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\Delta V_{GS}}{dV_{DG}}$ at I_D = constant).
4. Common mode rejection ratio:
   CMRR (in dB) = $-20\log\lvert\Delta\frac{g_{os}}{g_{fs}}\rvert$.

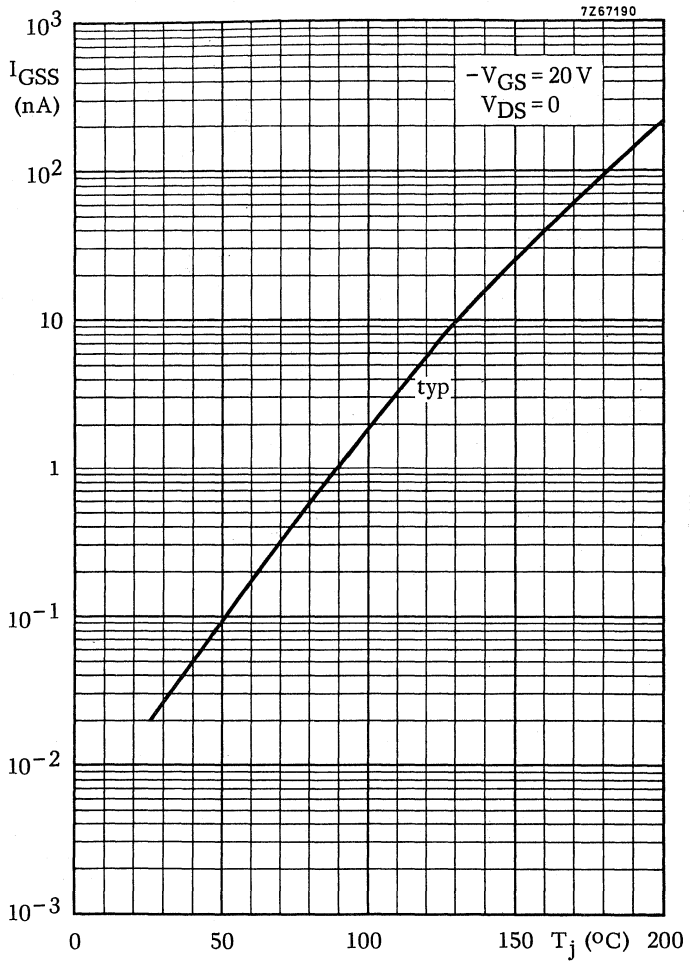
CHARACTERISTICS (Individual transistor)

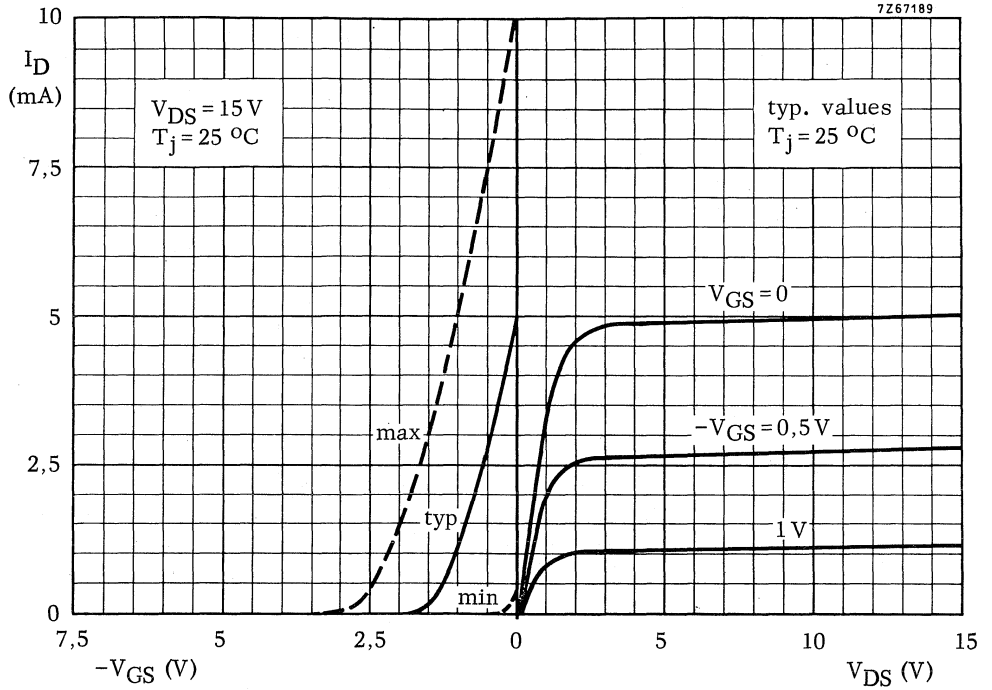
T_{amb} = 25 °C unless otherwise specified

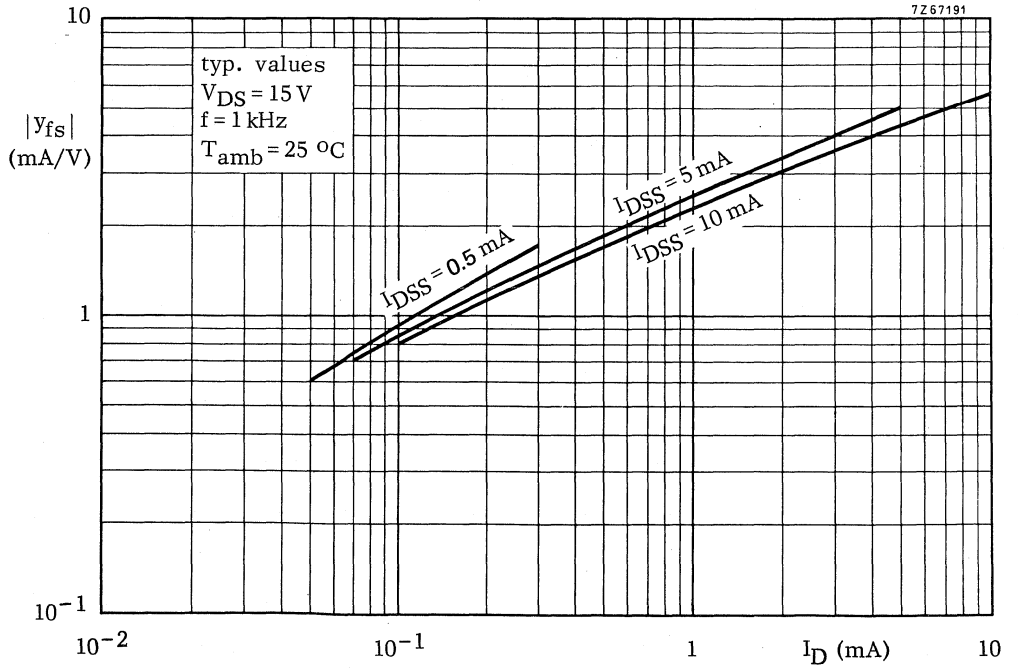
Gate cut-off current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100 pA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20 nA
Gate current			
I_D = 200 μA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10 nA
Drain current (note 1)			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		0.5 to 10 mA
Gate-source voltage			
I_D = 200 μA; V_{DG} = 15 V	$-V_{GS}$	<	2.7 V
Gate-source cut-off voltage			
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$		0.5 to 3.5 V
Transfer conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{os}	<	5 μS
Input capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{is}	<	8 pF
Feedback capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{rs}	<	1.0 pF
Equivalent noise voltage			
I_D = 200 μA; V_{DS} = 15 V; B = 0.6 to 100 Hz	V_n	<	0.5 μV

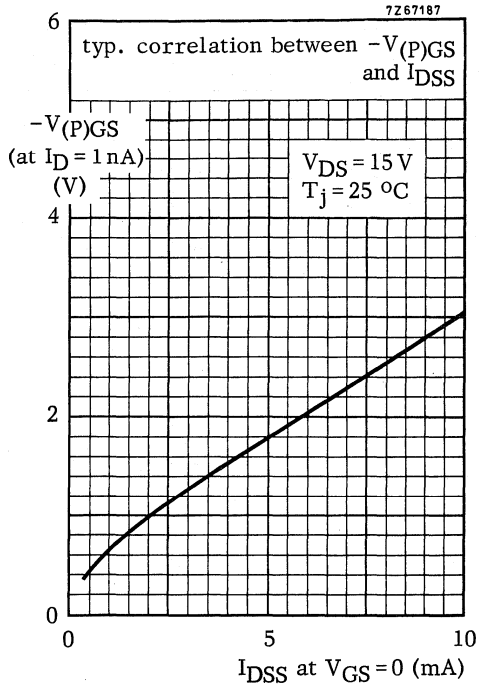
Notes

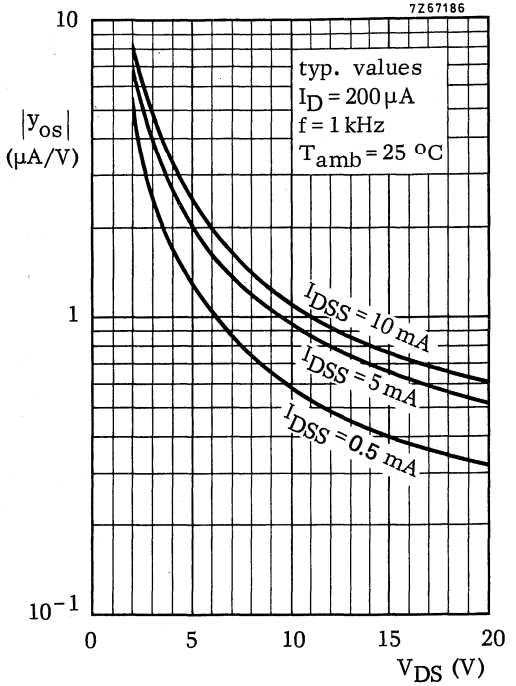
1. Measured under pulse conditions.
2. Measured with case grounded.

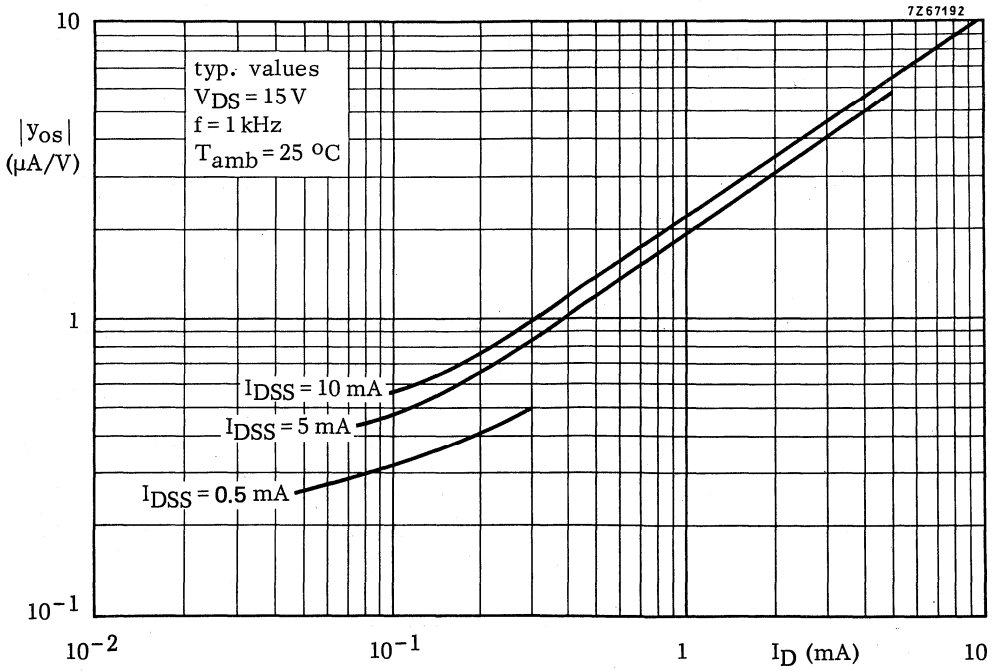

7Z67190
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 20$ V
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

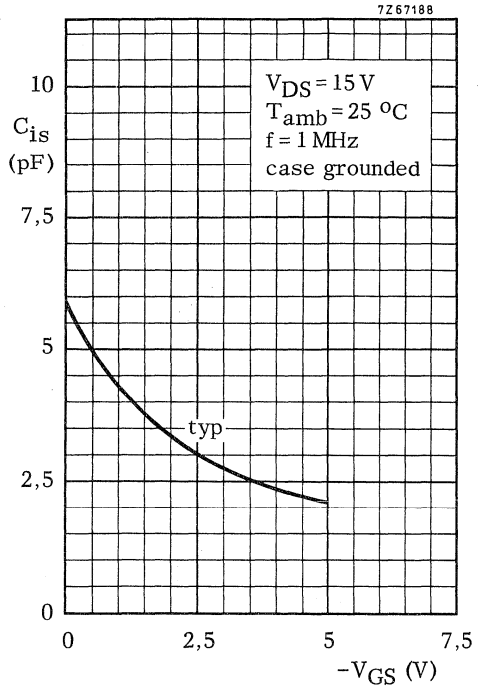

7Z67189
10
I_D (mA)
7,5
5
2,5
0
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
max
typ
min
7,5
5
2,5
0
5
10
15
$-V_{GS}$ (V)
V_{DS} (V)

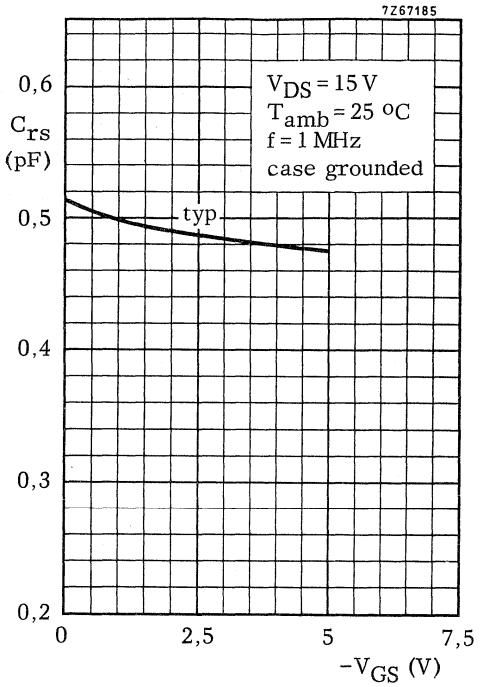

7Z67191
10
$|y_{fs}|$ (mA/V)
1
10^{-1}
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
I_{DSS} = 0.5 mA
I_{DSS} = 5 mA
I_{DSS} = 10 mA
10^{-2}
10^{-1}
1
I_D (mA)
10

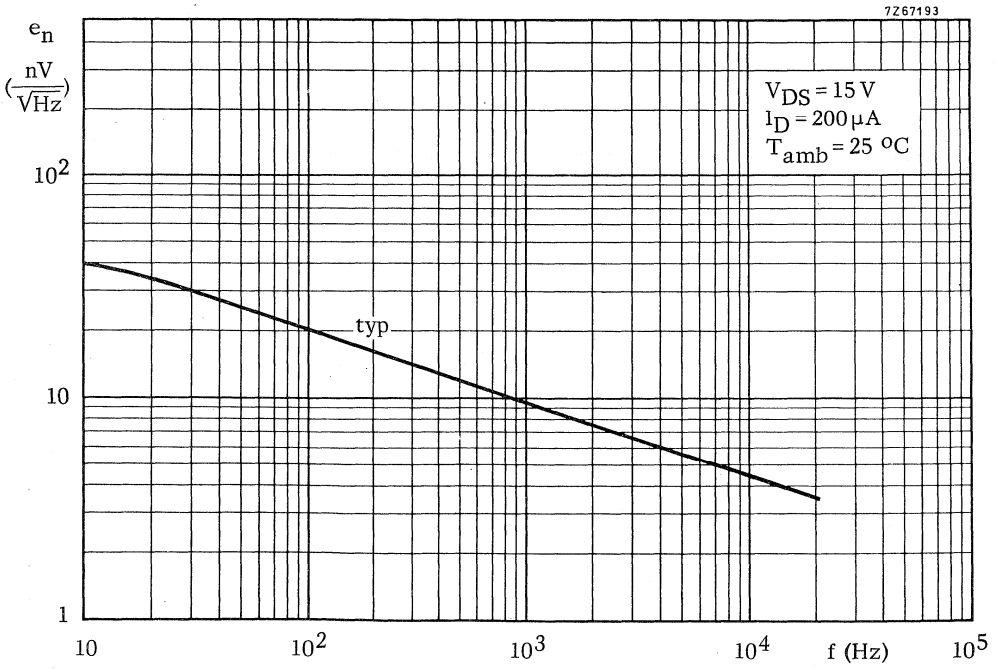

7Z67187
typ. correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ (at I_D = 1 nA) (V)
V_{DS} = 15 V
T_j = 25 °C
6
4
2
0
0
5
10
I_{DSS} at V_{GS} = 0 (mA)


7Z67186
typ. values
I_D = 200 µA
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0.5 mA
10
1
10^{-1}
0
5
10
15
20
V_{DS} (V)


7Z67192
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0.5 mA
10
1
10^{-1}
10^{-2}
10^{-1}
1
I_D (mA)
10


7Z67188
10
C_{is} (pF)
7,5
5
2,5
0
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67185
0,6
C_{rs} (pF)
0,5
0,4
0,3
0,2
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67193
e_n ($\frac{nV}{\sqrt{Hz}}$)
10^2
10
1
V_{DS} = 15 V
I_D = 200 μA
T_{amb} = 25 °C
typ
10
10^2
10^3
10^4
f (Hz)
10^5

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Planar epitaxial symmetrical junction field effect transistor in a microminiature plastic envelope. It is intended for low level general purpose amplifiers in thick and thin-film circuits.

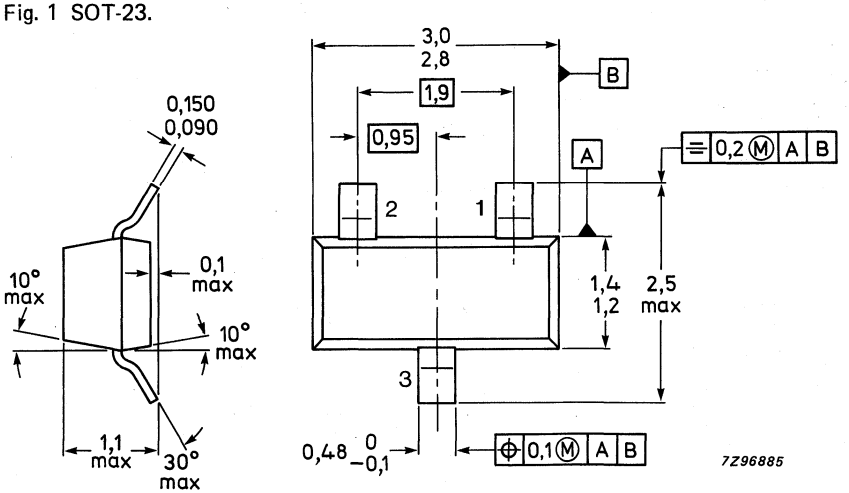
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25		V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250		mW
			BFR30	BFR31	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min. max.	4 10	1 5	mA mA
Transfer admittance (common source) I_D = 1 mA; V_{DS} = 10 V; f = 1 kHz	$\|y_{fs}\|$	min. max.	1.0 4.0	1.5 4.5	mS mS

MECHANICAL DATA

Fig. 1 SOT-23.

Dimensions in mm



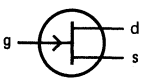
TOP VIEW

Marking code

BFR30 = M1p
BFR31 = M2p

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 40 °C*	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BFR30	BFR31	
Gate cut-off current					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	max.	0.2	0.2	nA
Drain current					
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	min.	4	1	mA
		max.	10	5	mA
Gate-source voltage					
I_D = 1 mA; V_{DS} = 10 V	$-V_{GS}$	min.	0.7	0	V
		max.	3.0	1.3	V
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	max.	4.0	2.0	V
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	max.	5	2.5	V
y parameters					
Transfer admittance at f = 1 kHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	1.0	1.5	mS
		max.	4.0	4.5	mS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{fs}\rvert$	min.	0.5	0.75	mS
Output admittance at f = 1 kHz					
I_D = 1 mA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	40	25	μS
I_D = 200 μA; V_{DS} = 10 V	$\lvert y_{os}\rvert$	max.	20	15	μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

y parameters (continued)

			BFR30	BFR31	
Input capacitance at f = 1 MHz					
I_D = 1 mA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
I_D = 200 μA; V_{DS} = 10 V	C_{is}	max.	4	4	pF
Feedback capacitance at f = 1 MHz; T_{amb} = 25 °C					
I_D = 1 mA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
I_D = 200 μA; V_{DS} = 10 V	C_{rs}	max.	1.5	1.5	pF
Equivalent noise voltage					
I_D = 200 μA; V_{DS} = 10 V B = 0.6 to 100 Hz	V_n	max.	0.5	0.5	μV

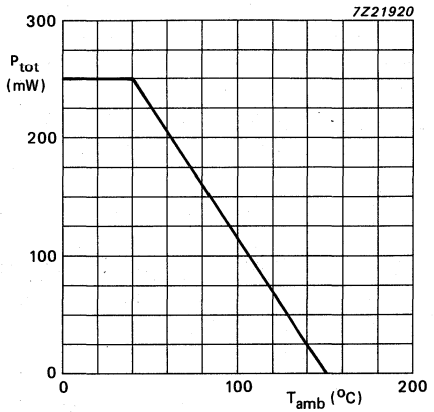


Fig.2 Power derating curve.

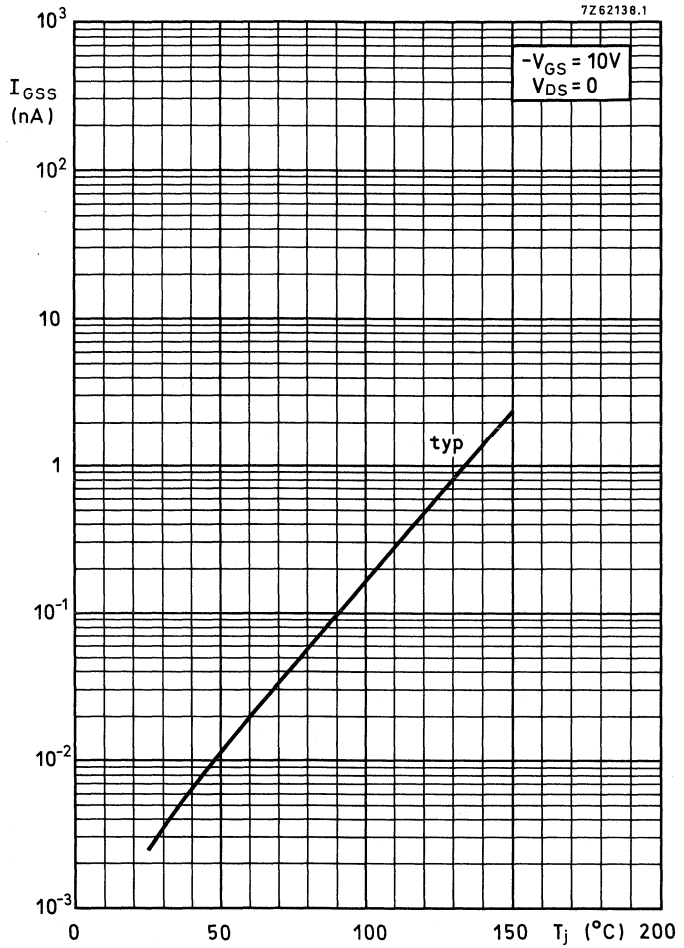

7Z62138.1
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

Fig.3.

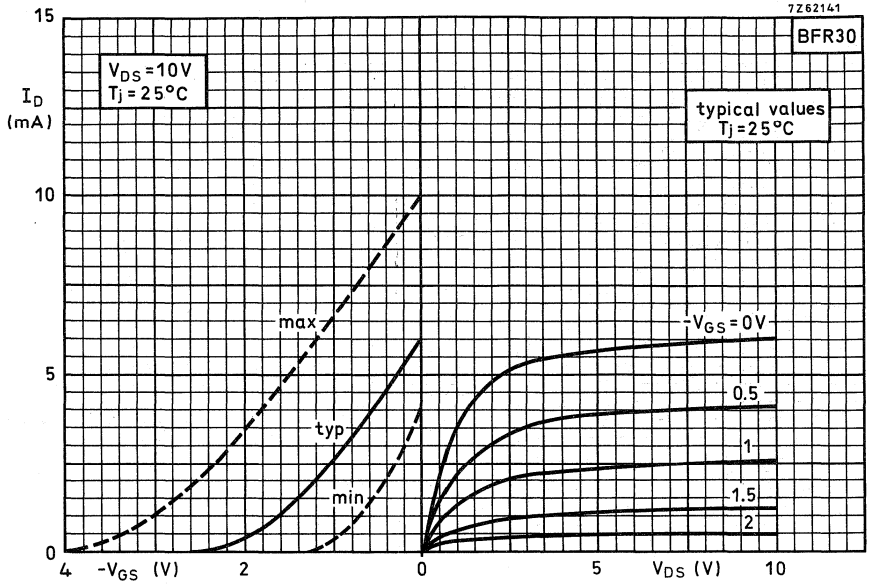

7Z62141
BFR30
V_{DS} = 10 V
T_j = 25 °C
typical values
T_j = 25 °C
I_D (mA)
15
10
5
0
max
typ
min
$-V_{GS}$ = 0 V
0.5
1
1.5
2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.4.

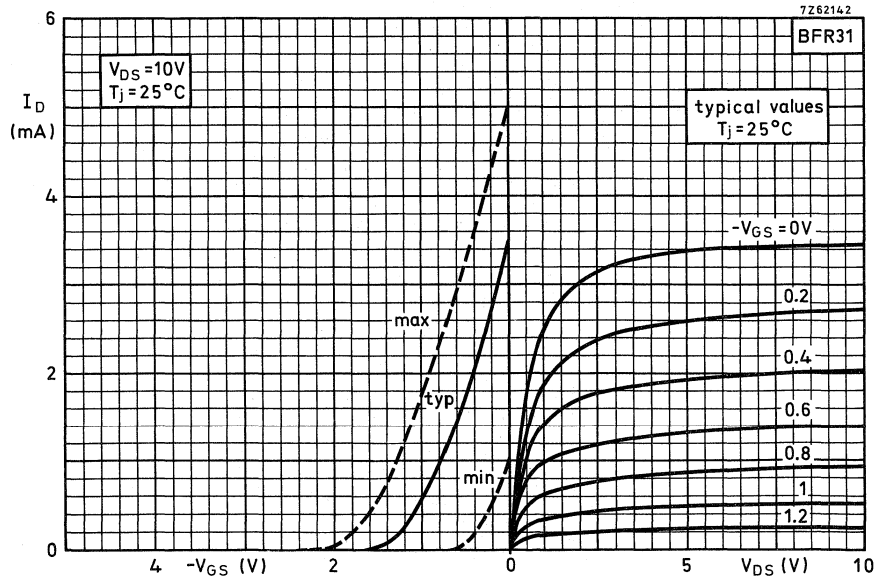

7Z62142
BFR31
V_{DS} = 10 V
T_j = 25 °C
typical values
T_j = 25 °C
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0 V
0.2
0.4
0.6
0.8
1
1.2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

Fig.5.

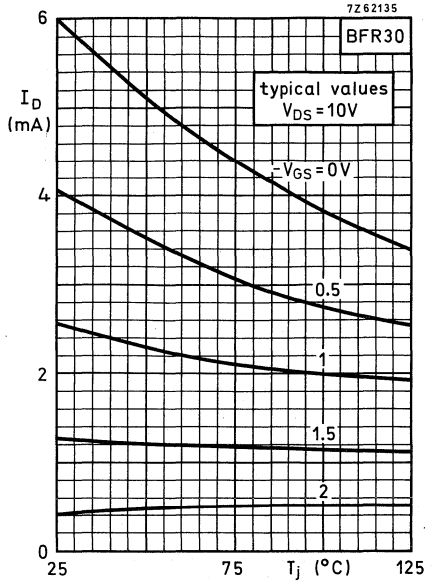


Fig.6.

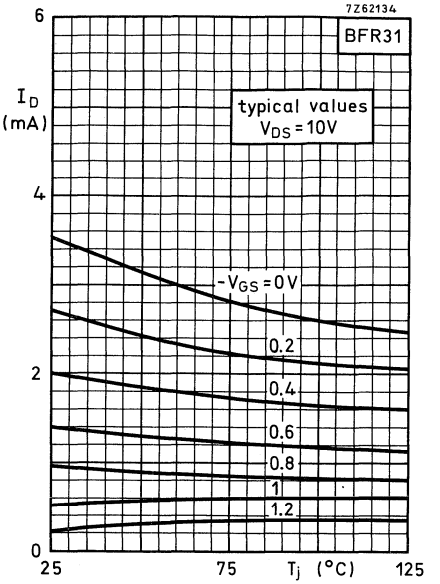


Fig.7.

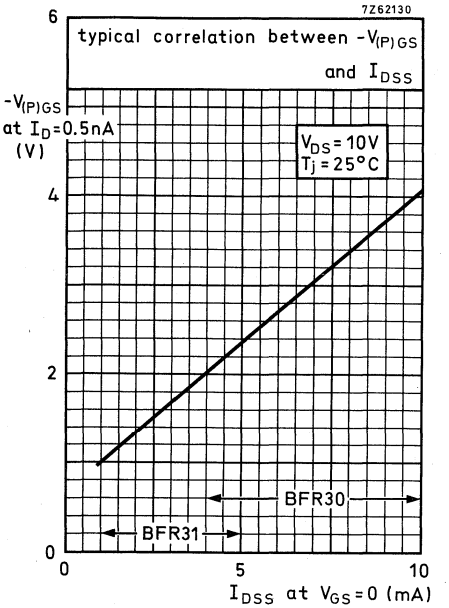


Fig.8.

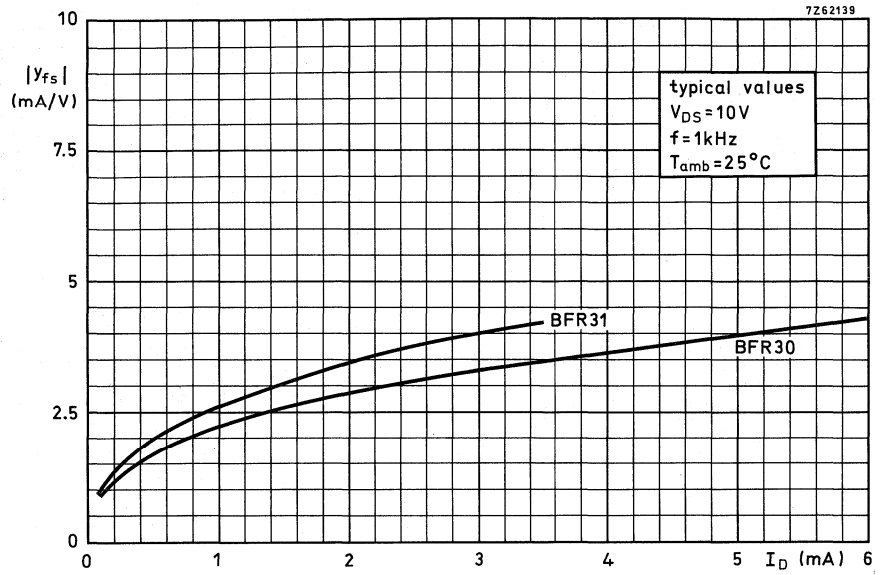

7Z62139
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR31
BFR30
0
1
2
3
4
5
ID (mA)
6

Fig.9.

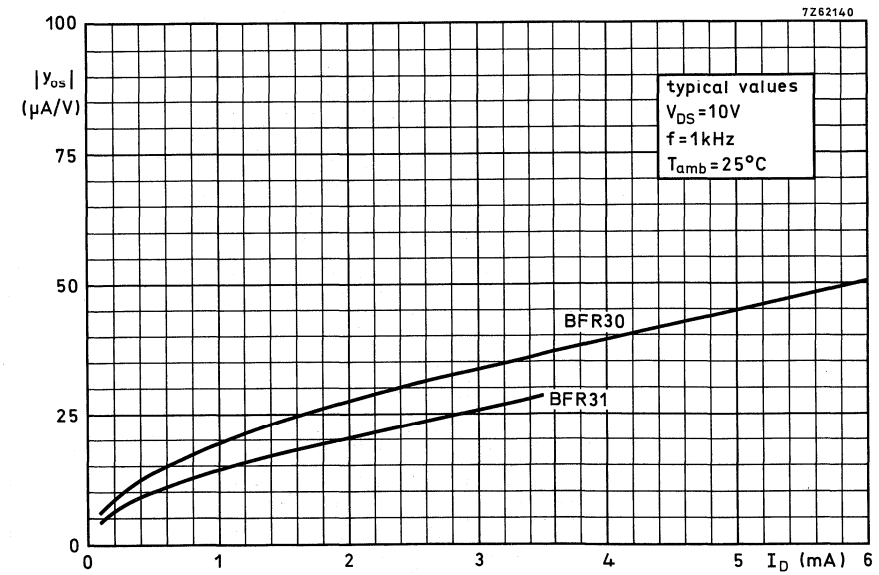

7Z62140
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS=10V
f=1kHz
Tamb=25°C
BFR30
BFR31
0
1
2
3
4
5
ID (mA)
6

Fig.10.

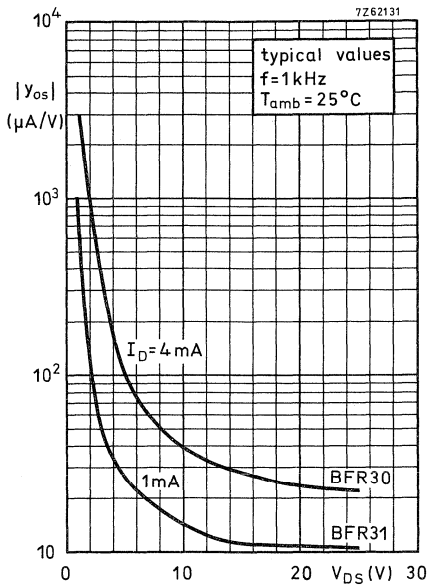


Fig.11.

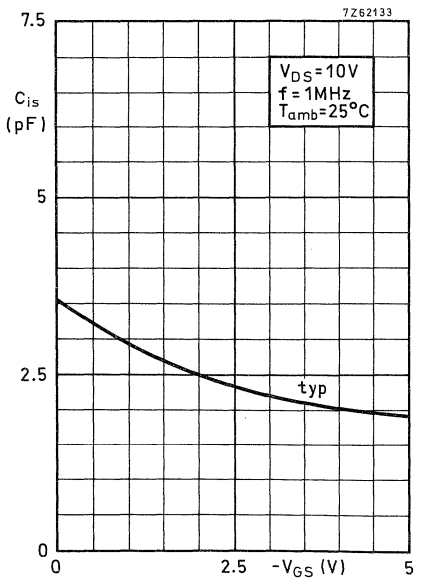


Fig.12.

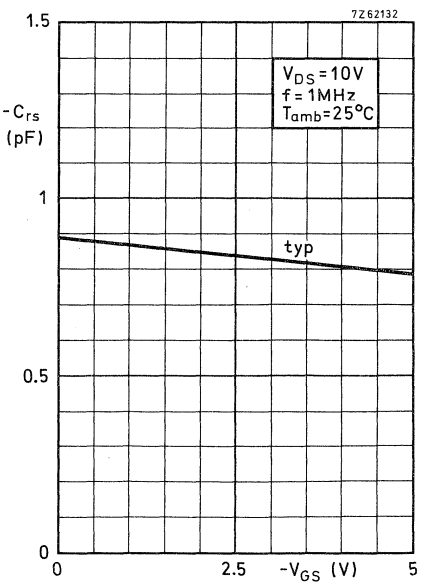


Fig.13.

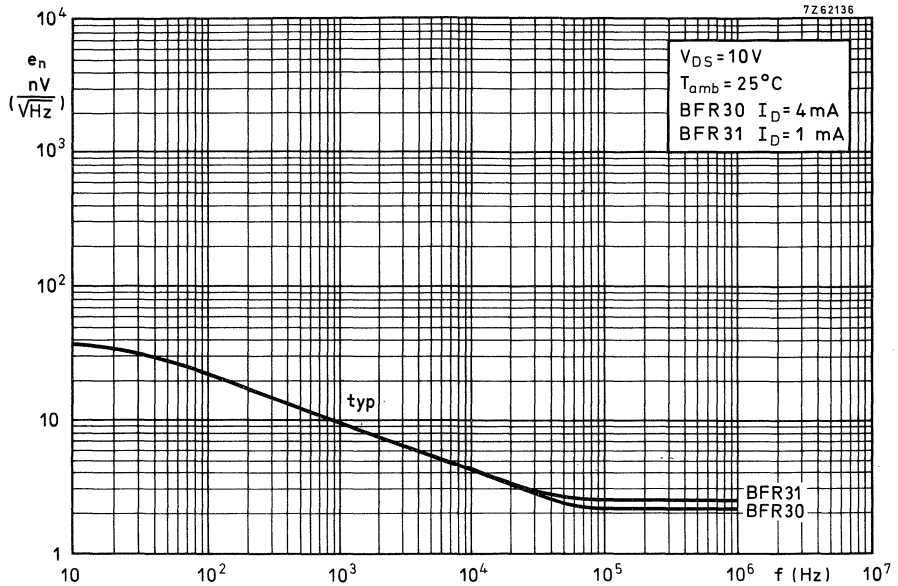

7Z62136
10^4
e_n
nV
($\frac{}{\sqrt{Hz}}$)
10^3
10^2
10
1
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.14.

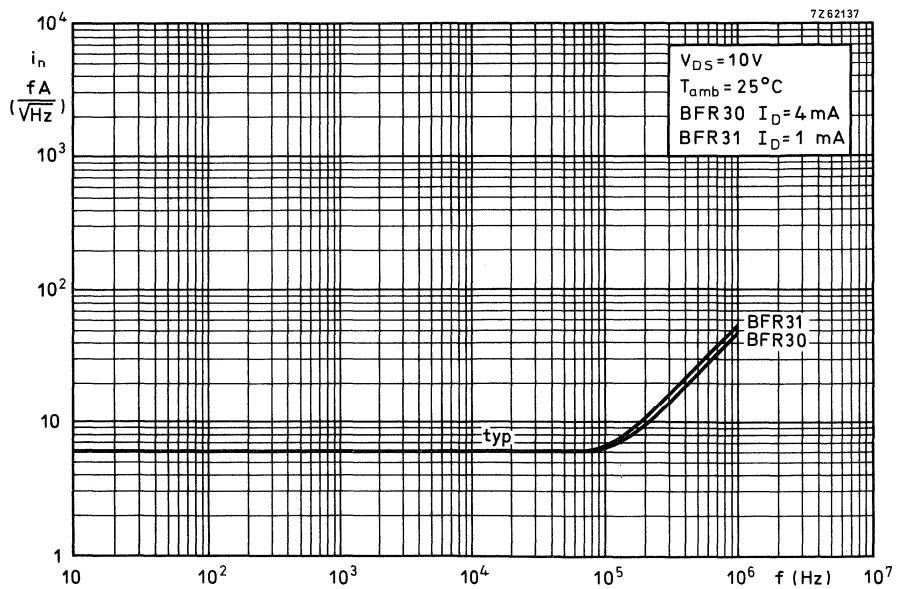

7Z62137
10^4
i_n
fA
($\frac{}{\sqrt{Hz}}$)
10^3
10^2
10
1
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4mA
BFR31 I_D = 1 mA
BFR31
BFR30
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

Fig.15.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel silicon junction field-effect transistor, designed primarily for use as a source follower with the input protected against successive voltage surges by a forward and reverse integrated diode.

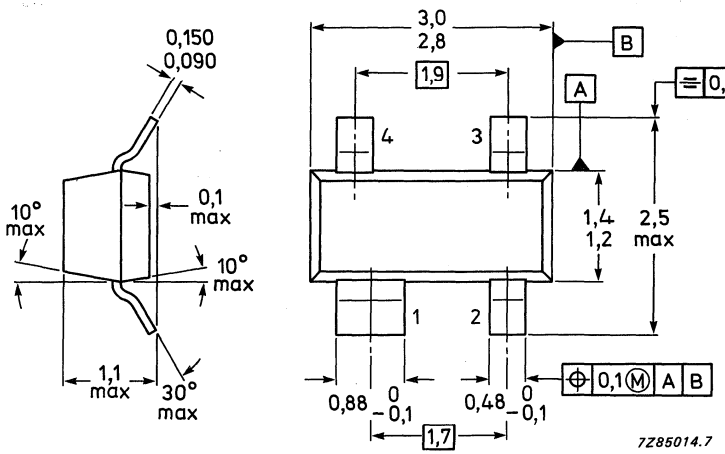
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GS}$	max.	30	V
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200	mW
Drain current				
V_{DS} = 6 V; V_{GS} = 0: BFR101A	I_{DSS}		0,2 to 1,5	mA
V_{DS} = 6 V; V_{GS} = 0: BFR101B	I_{DSS}		1,0 to 5,0	mA
Transfer admittance (common source)				
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101A	$\|y_{fs}\|$	>	1,2	mS
V_{DS} = 6 V; V_{GS} = 0; f = 1 kHz: BFR101B	$\|y_{fs}\|$	>	2,5	mS

MECHANICAL DATA

Fig. 1 SOT-143.

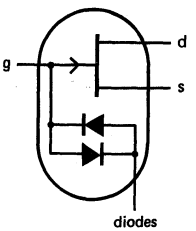
Dimensions in mm



TOP VIEW

Marking code

BFR101A = M97
BFR101B = M98



Pinning

1 = gate
2 = diodes
3 = source
4 = drain

Note: Drain and source are interchangeable.

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current (d.c.)	I_D	max.	20 mA
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C*	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	460 K/W

CHARACTERISTICS with source connected to case for all measurements

T_j = 25 °C unless otherwise specified

		BFR101A	BFR101B
Gate leakage current V_{DS} = 6 V; I_D = 10 μA	$-I_G$	< 5	5 nA
Drain current V_{DS} = 6 V; V_{GS} = 0	I_{DSS}	0,2 to 1,5	1 to 5 mA
Gate-source cut-off voltage V_{DS} = 6 V; I_D = 1 μA	$-V_{(P)GS}$	0,2 to 1	0,5 to 2,5 V
Small-signal common-source characteristics V_{DS} = 6 V; V_{GS} = 0, T_{amb} = 25 °C			
Transfer admittance f = 1 kHz	$\lvert y_{fs}\rvert$	> 1,2	2,5 mS
Output admittance at f = 1 kHz	$\lvert y_{os}\rvert$	typ. 10	50 mS
Input capacitance at f = 1 MHz diodes not connected	C_{is}	< 5	5 pF
Diode capacitance V_D = 0; source and drain not connected	C_d	typ. 0,7	0,7 pF
Diode forward voltage $\pm I_F$ = 10 mA	V_F	0,7 to 1,2	0,7 to 1,2 V

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

BFR200

N-channel junction field-effect transistor

FEATURES

- Ultra-low leakage performance ($-I_{GSS}$ max. 3 pA); important for use in highly sensitive equipment, such as burglar alarms, infrared sensors, etc.
- Insensitive to radio frequency interference (RFI), owing to an integrated low pass filter.
- Input protected against successive voltage surges by a forward and reverse integrated diode.
- Low LF noise performance (20 nV/√Hz).

DESCRIPTION

Silicon asymmetrical n-channel junction FET in a surface mount SOT143 envelope, with an integrated RC low pass filter and two anti-parallel diodes connected to the gate. It is designed primarily for use as a source follower in infrared detectors, burglar alarms, electret microphones, smoke alarms and radiation detectors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	-	30	V
I_{DSS}	drain current	0.2	3.5	mA
$-V_{GS(off)}$	gate-source cut-off voltage	0.5	2	V

N-channel junction field-effect transistor BFR200

MECHANICAL DATA

Dimensions in mm

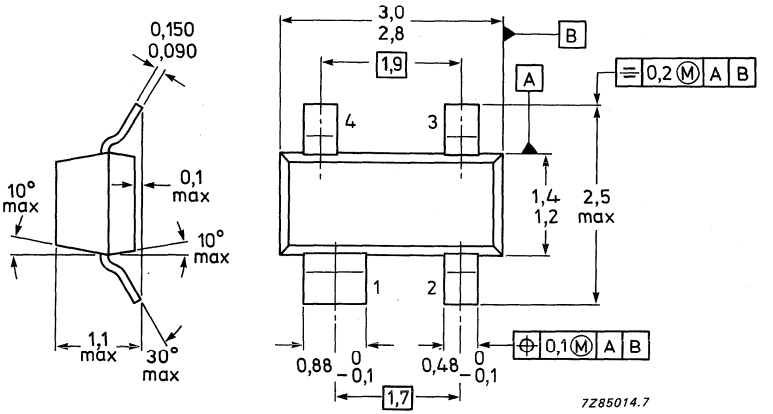


Fig.1 SOT143.

PIN CONFIGURATION

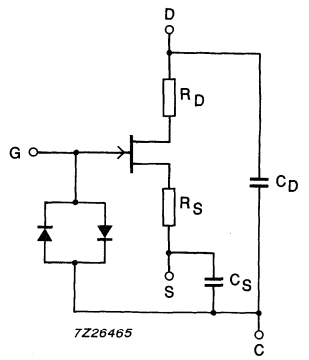


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	gate
2	common
3	source
4	drain

Marking: BFR200 = M20

N-channel junction field-effect transistor BFR200

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	30	V
$-V_{GSO}$	gate-source voltage		-	30	V
$-V_{GDO}$	gate-drain voltage		-	30	V
I_D	drain current	DC	-	20	mA
I_G	forward gate current	DC	-	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on FR4 printboard.

N-channel junction field-effect transistor BFR200

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 $-I_G$ = 1 μA	30	-	-	V
I_{DSS}	drain current	V_{DS} = 6 V V_{GS} = 0	0.2	-	3.5	mA
$-I_{GSS}$	gate-source leakage current (note 1)	$-V_{GS}$ = 6 V V_{DS} = 0 V_{GC} = 0	-	-	3	pA
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 0.1 μA V_{DS} = 6 V	0.5	-	2	V
V_F	diode forward voltage	$\pm I_F$ = 10 mA	0.7	-	1.2	V
R_D	drain resistance		-	800	-	Ω
R_S	source resistance		-	180	-	Ω

Notes

1. Based on level I, AQL 1.5%.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	V_{DS} = 6 V V_{GS} = 0	1.3	-	-	mS
$\lvert Y_{os} \rvert$	output admittance	V_{DS} = 6 V V_{GS} = 0	-	40	-	μS
C_{iss}	input capacitance (note 1)	V_{DS} = 6 V V_{GS} = 0 V_{GC} = 0 f = 1 MHz	-	-	6	pF
C_{GC}	diode capacitance	V_{GC} = 0 drain and source grounded	-	3	-	pF
C_D	drain decoupling capacitance	V_{DC} = 0 gate and source grounded	-	8	-	pF
C_S	source decoupling capacitance	V_{SC} = 0 gate and drain grounded	-	8	-	pF

Notes

1. Value is inclusive of the capacitance of the diodes.

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7,5	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA

SOT-52 (see next page)

TOTAL DEVICE

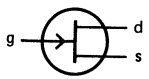
Dimensions in mm

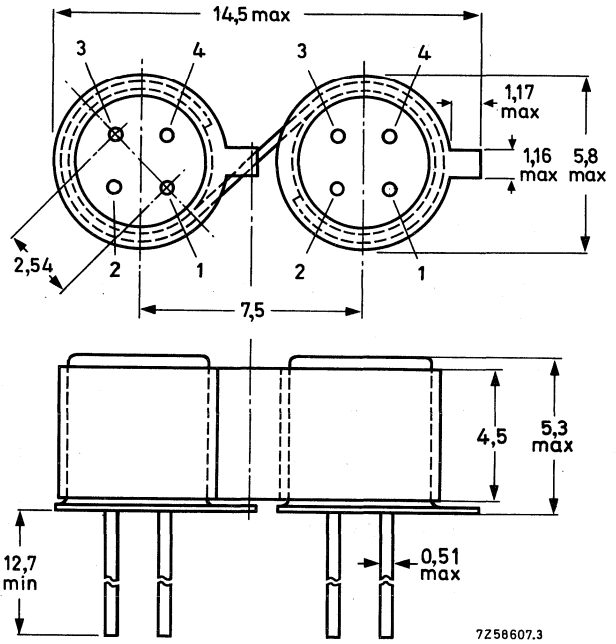
MECHANICAL DATA

SOT52

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case





Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}	−20 to + 100	°C

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

			BFS21	BFS21A	
Drain current ratio					
V_{DG} = 15 V; V_{GS} = 0; T_j = 25 °C	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	>	0.95	0.95	
		<	1.05	1.05	
Gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Change of gate-source voltage difference with ambient temperature					
T_{amb} = 25 to 100 °C					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
Difference of penetration factors*					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
Difference of transfer impedances**					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7.8	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	75	37.5	Ω

* The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,V_{DG}} \text{ at } I_D = \text{constant}\right)$$

** The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta\frac{1}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,I_D} \text{ at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

			BFS21	BFS21A	
Common mode rejection ratio*					
I_D = 500 μA; V_{DG} = 15 V	CMRR	>	60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	>	60	66	dB

INDIVIDUAL TRANSISTOR RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25°	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

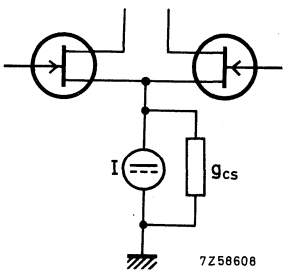
From junction to ambient in free air (for individual transistor without S-clip)	$R_{th\ j\text{-}a}$	=	590	K/W

* **Common mode rejection ratio**

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \tfrac{1}{2} g_{cs} \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.

The guaranteed values of CMRR apply at g_{cs} = 0.1 μΩ^{-1}



CHARACTERISTICS (individual transistor)

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
I_D = 500 μA; V_{DS} = 15 V	I_G	<	0.5 nA
I_D = 500 μA; V_{DS} = 15 V; T_{amb} = 100 °C	I_G	<	25 nA
Drain current			
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C	I_{DSS}	>	1 mA
Gate-source cut-off voltage			
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	6 V
Transfer conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 500 μA; V_{DS} = 15 V	g_{os}	<	15 μS
Input capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz			
I_D = 500 μA; V_{DS} = 15 V	C_{rs}	<	0.75 pF
Equivalent noise voltage			
f = 10 Hz			
I_D = 500 μA; V_{DS} = 15 V	$V_n/\sqrt{B}$	<	200 nV/$\sqrt{Hz}$
V_{DS} = 15 V; V_{GS} = 0	$V_n/\sqrt{B}$	<	75 nV/$\sqrt{Hz}$

N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

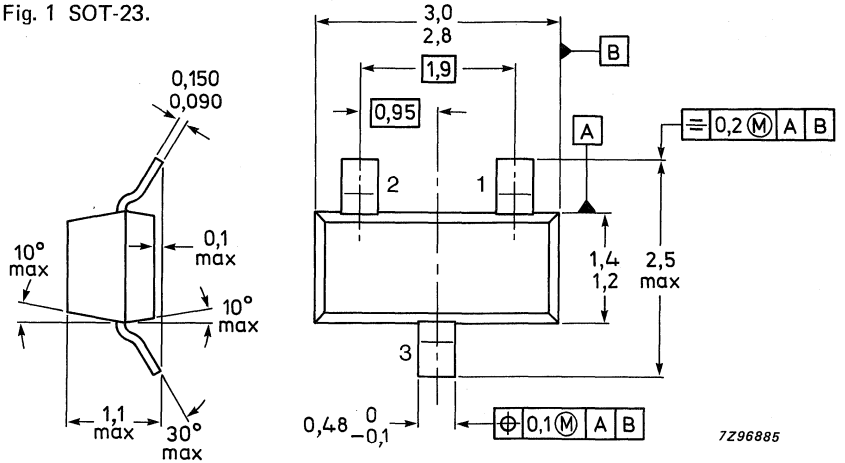
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250 mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	$>$ $<$	0,2 mA 1,5 mA
Transfer admittance (common source) I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs} \rvert$	$>$	0,5 mS
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	$<$	0,5 μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



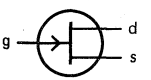
TOP VIEW

Marking code

BFT46 = M3

Pinning

1 = drain
2 = source
3 = gate



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2 nA
Drain current			
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2 mA
		<	1,5 mA
Gate-source voltage			
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1 V
		<	1,0 V
Gate-source cut-off voltage			
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2 V
y-parameters at f = 1 kHz;			
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	1,0 mS
Output admittance	$\lvert y_{os} \rvert$	<	10 μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	0,5 mS
Output admittance	$\lvert y_{os} \rvert$	<	5 μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	<	0,5 μV

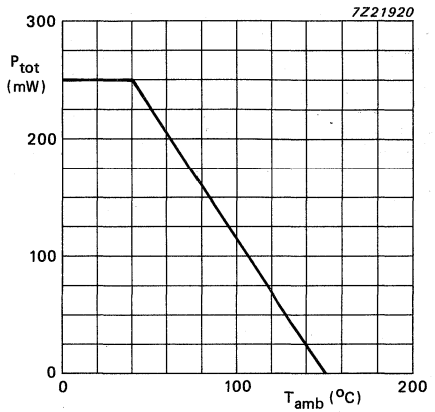


Fig.2 Power derating curve.

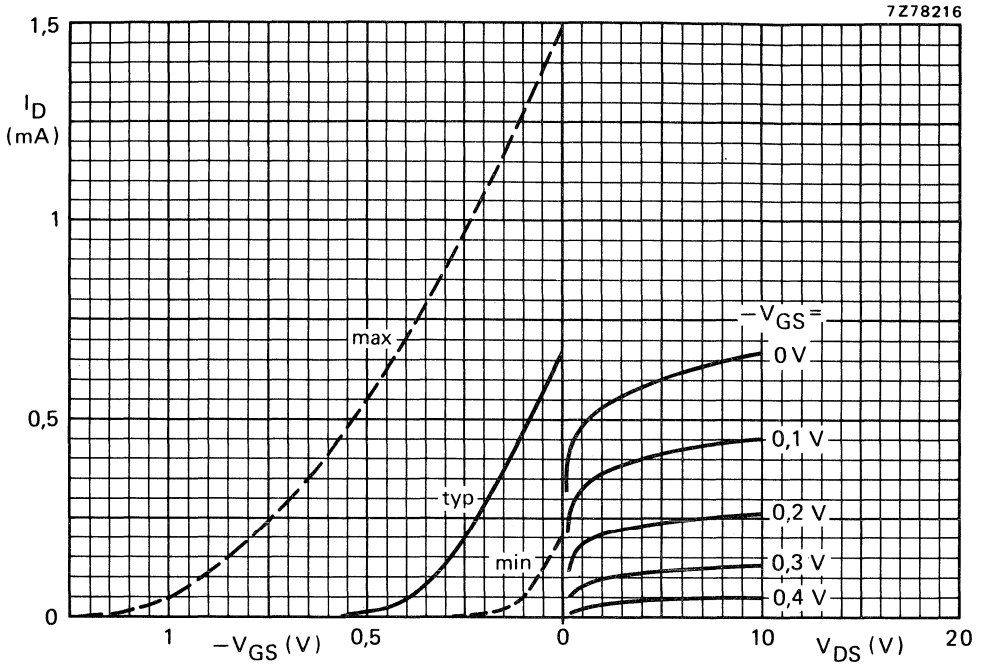


Fig. 3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

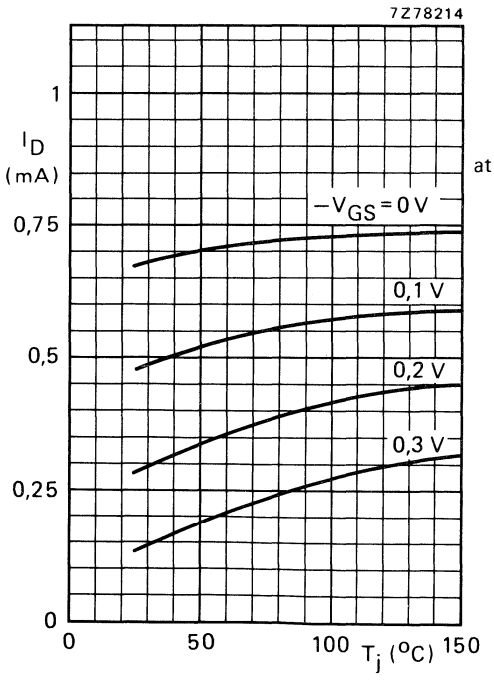


Fig. 4 Typical values. V_{DS} = 10 V.

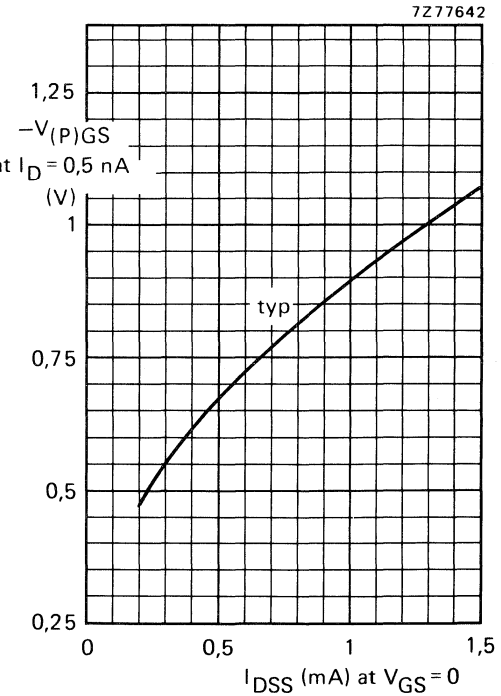


Fig. 5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

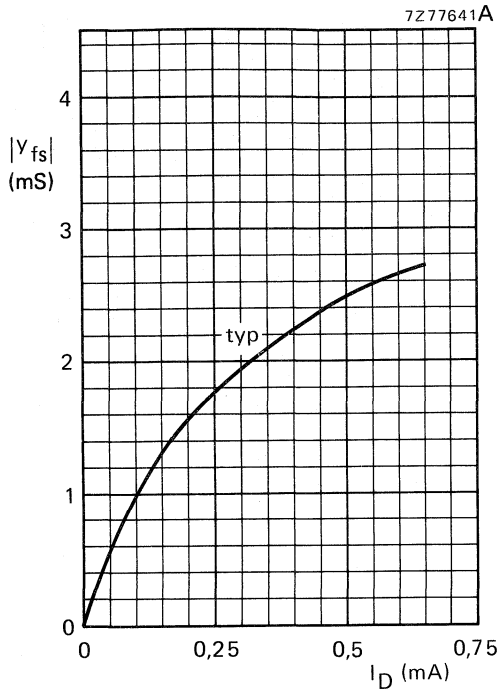


Fig. 6

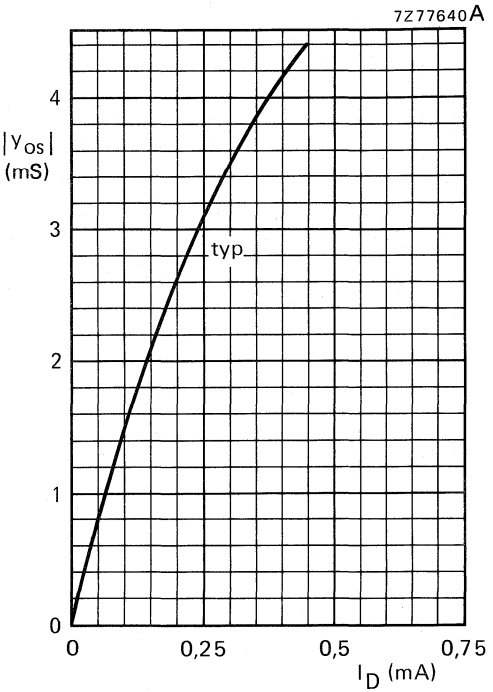


Fig. 7

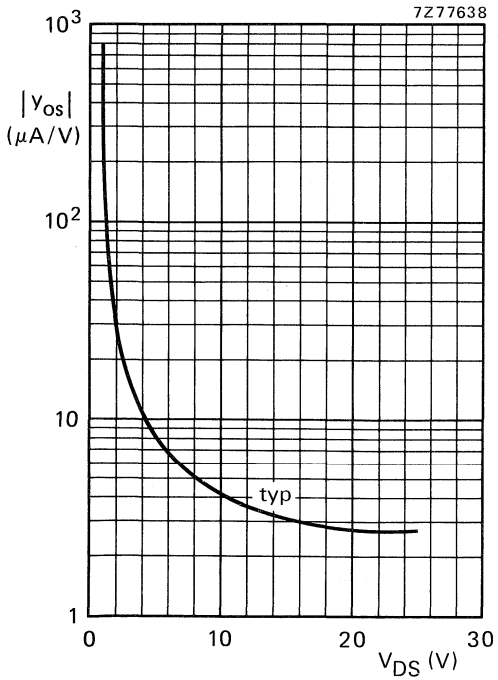


Fig. 8

Fig. 6 $|y_{fs}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 7 $|y_{os}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 8 $|y_{os}|$ versus V_{DS}.
I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

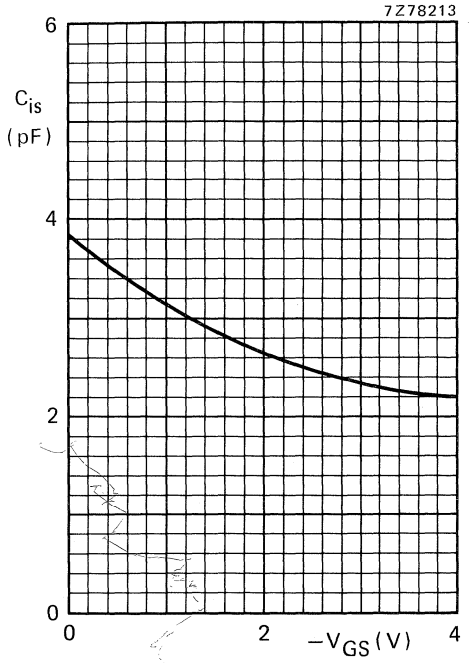


Fig. 9

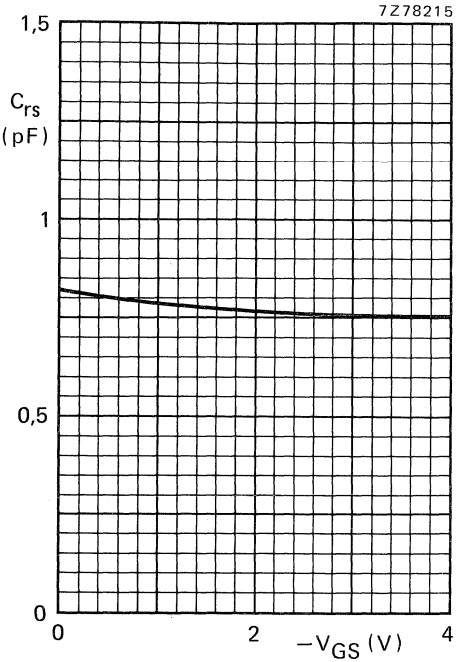


Fig. 10

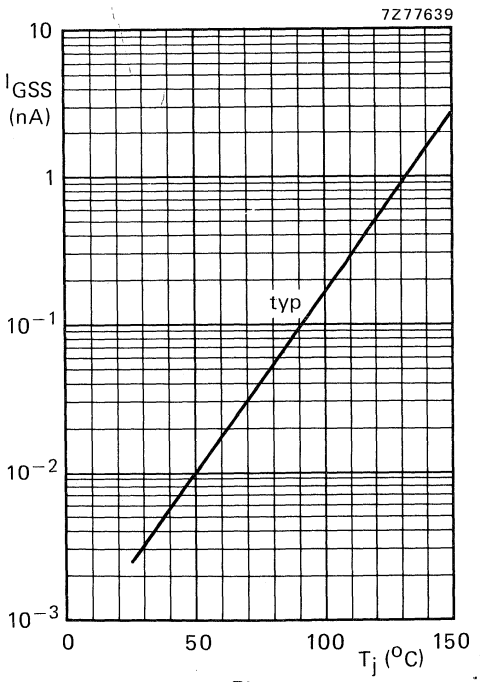


Fig. 11

Fig. 9 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 11 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

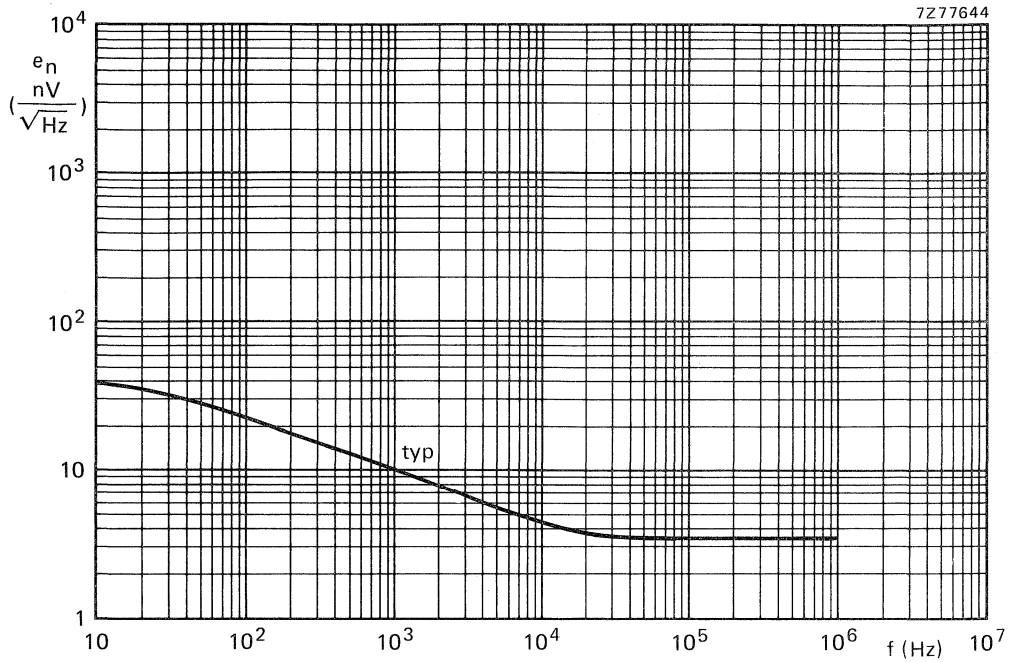


Fig. 12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

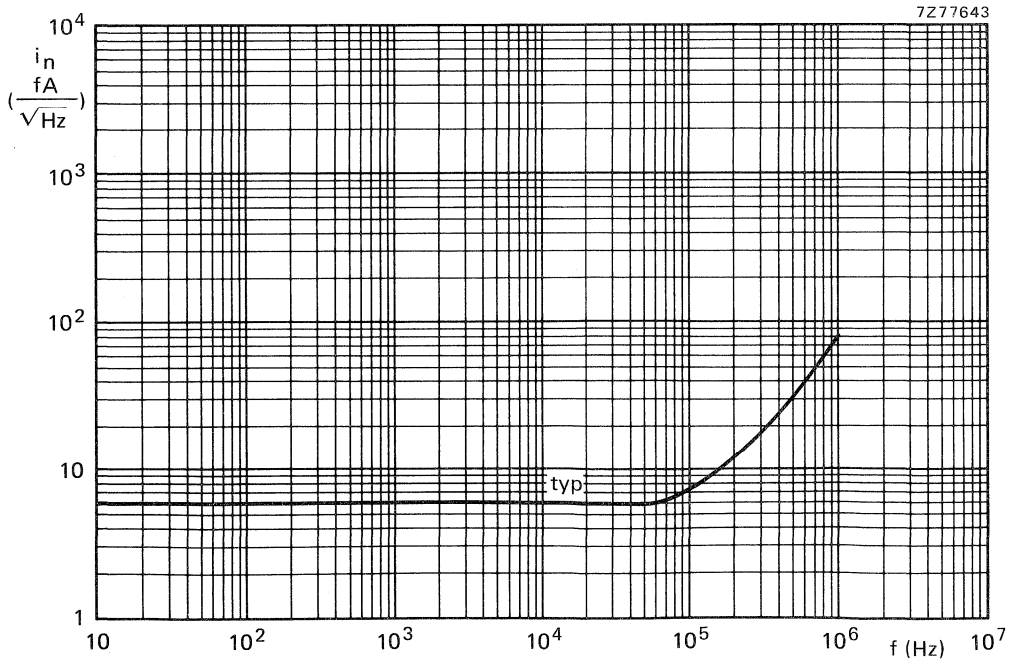


Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250		mW
			BFW10	**BFW11**	
Drain current		>	8	4	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	20	10	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\|y_{fs}\|$	>	3,2	3,2	mS
Noise figure at V_{DS} = 15 V; V_{GS} = 0					
f = 100 MHz; R_G = 1 kΩ	F	<	2,5	2,5	dB
Equivalent noise voltage					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

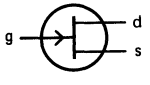
MECHANICAL DATA

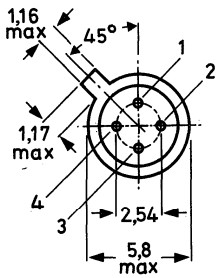
Dimensions in mm

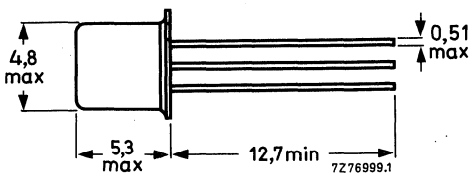
Fig.1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

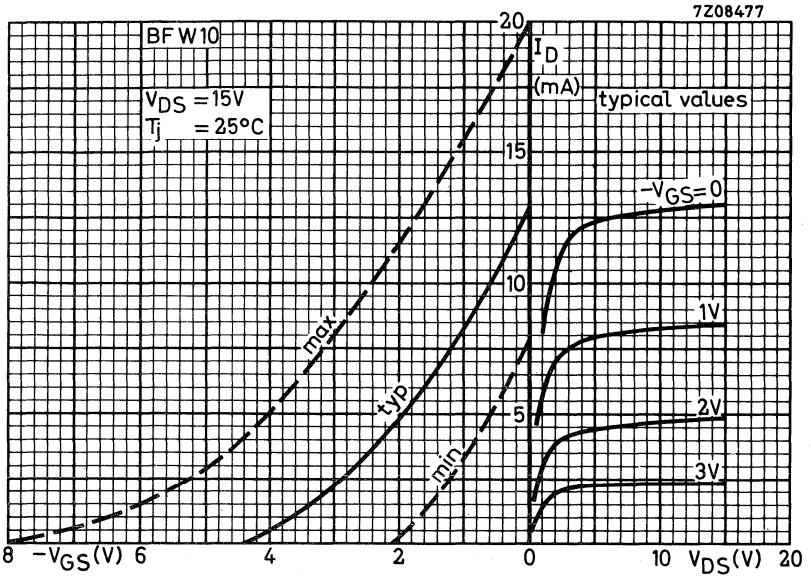
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

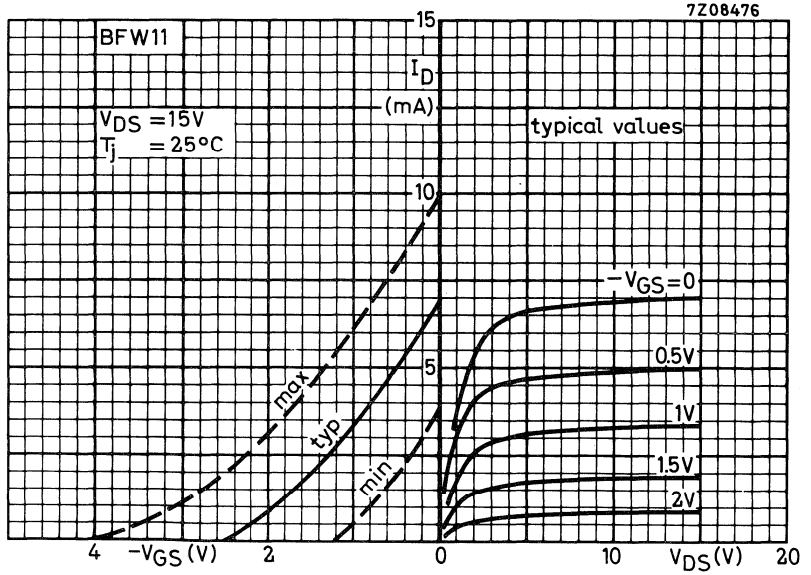
CHARACTERISTICS

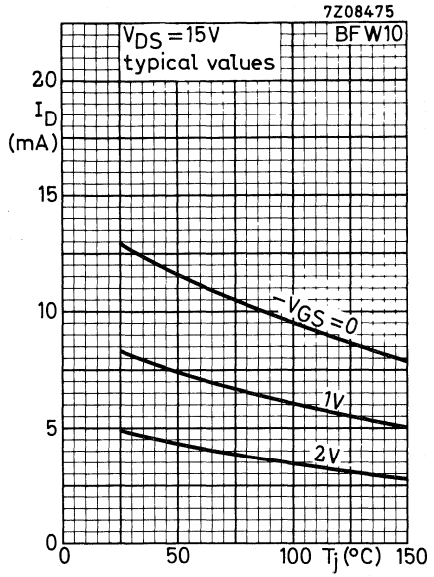
T_j = 25 °C unless otherwise specified

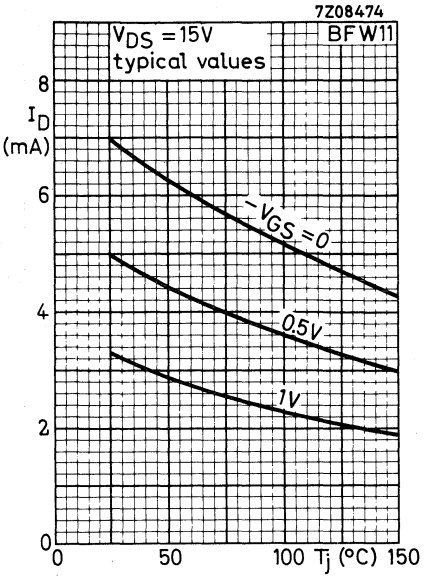
			BFW10	BFW11	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current*					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 1 kHz					
Transfer admittance	$\lvert y_{fs} \rvert$	>	3.5	3.0	mS
		<	6.5	6.5	mS
Output admittance	$\lvert y_{os} \rvert$	<	85	50	μS
f = 1 MHz; input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz; transfer admittance	$\lvert y_{fs} \rvert$	>	3.2	3.2	mS
Input capacitance	g_{is}	<	800	800	μS
Output capacitance	g_{os}	<	200	100	μS
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

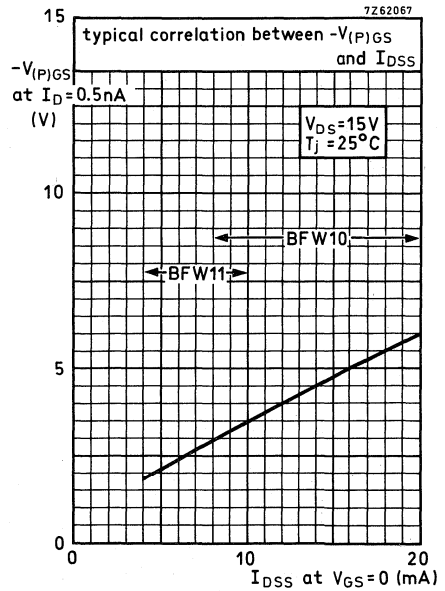
* Measured under pulsed conditions.

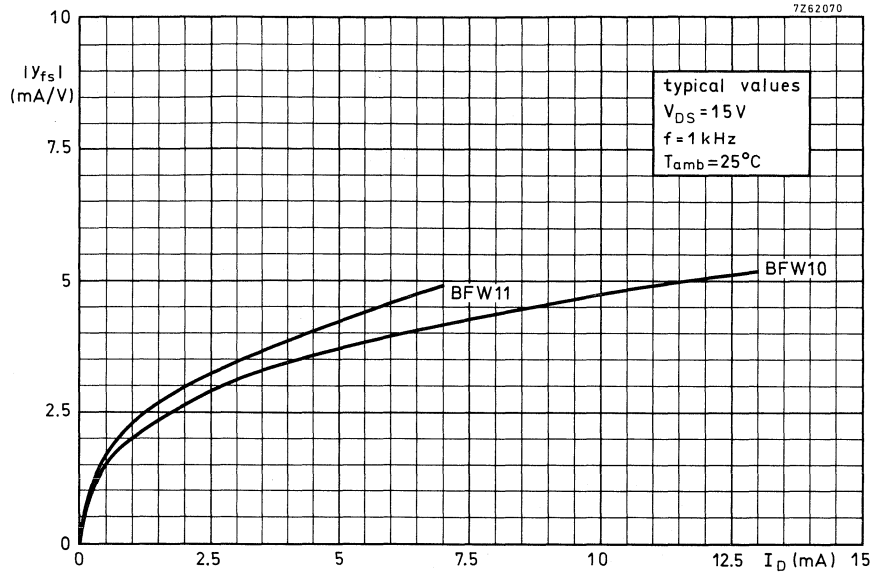

7Z08477
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
20
15
10
5
8
6
4
2
0
10
20
$-V_{GS}$(V)
V_{DS}(V)

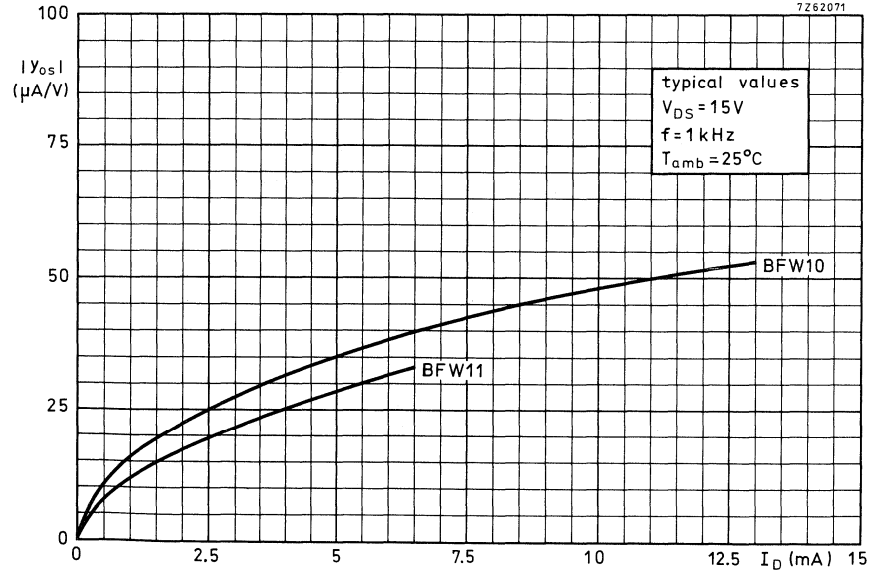

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
15
10
5
4
2
0
10
20
$-V_{GS}$(V)
V_{DS}(V)

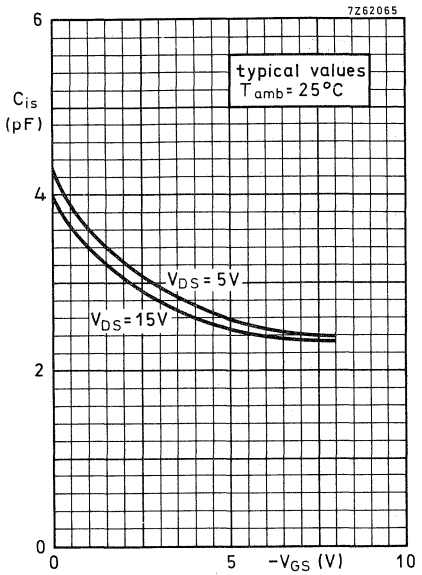

7Z08475
V_{DS} = 15V
typical values
BFW10
I_D (mA)
20
15
10
5
0
$-V_{GS}$ = 0
1V
2V
0
50
100
T_j (°C)
150

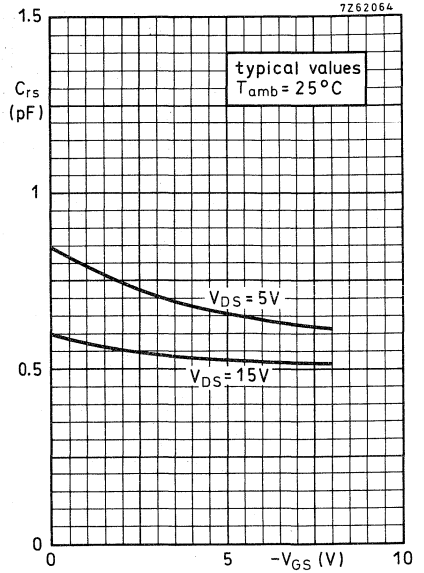

7Z08474
V_{DS} = 15V
typical values
BFW11
I_D (mA)
8
6
4
2
0
$-V_{GS}$ = 0
0.5V
1V
0
50
100
T_j (°C)
150

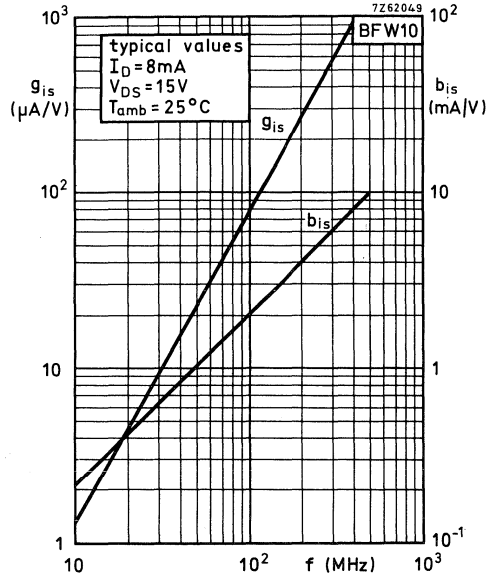

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
15
10
5
0
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

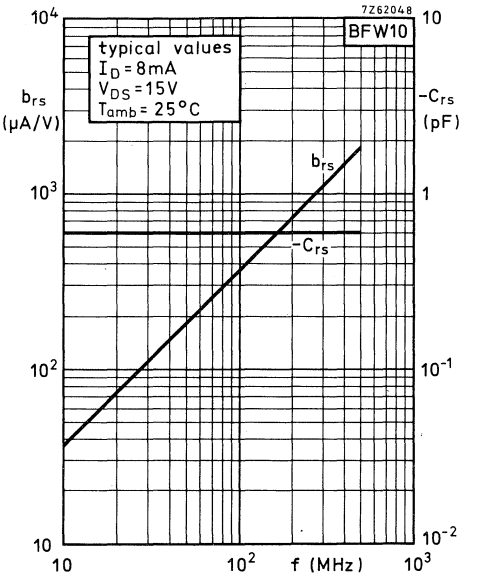

7Z62070
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1 kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

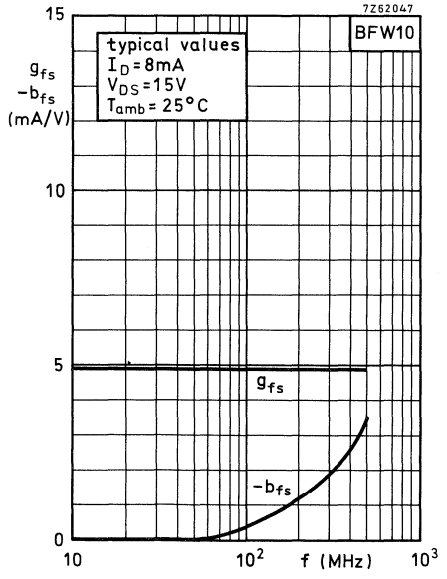

7Z62071
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS = 15V
f = 1 kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

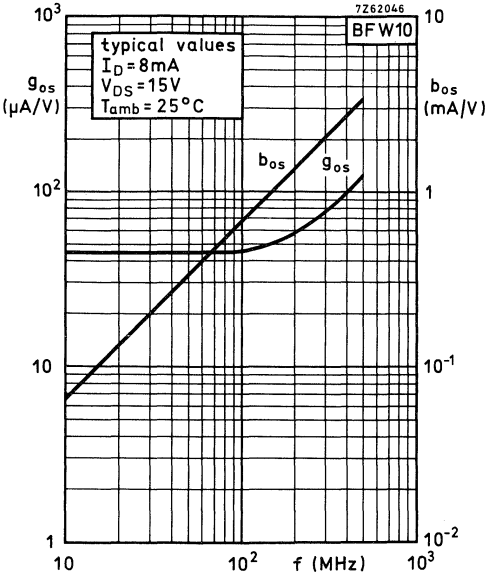

7Z62065
typical values
T_{amb} = 25 °C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
10
$-V_{GS}$ (V)

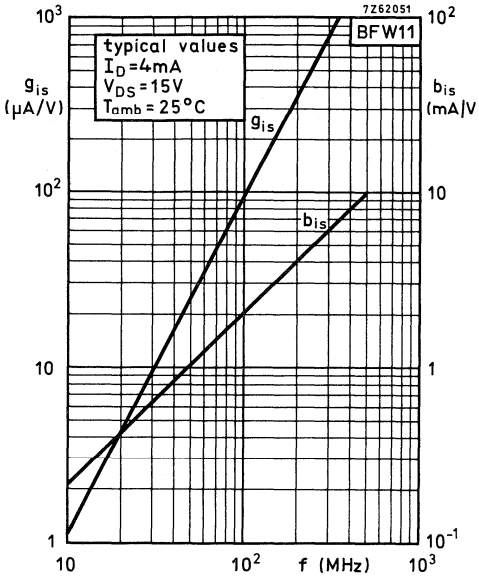

7Z62064
typical values
T_{amb} = 25 °C
C_{rs} (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
10
$-V_{GS}$ (V)

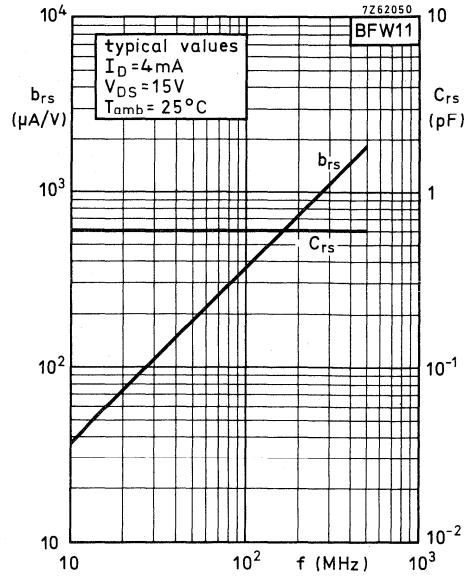

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

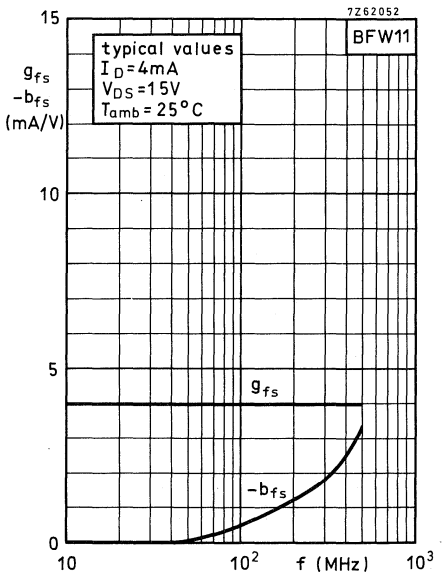

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
f (MHz)

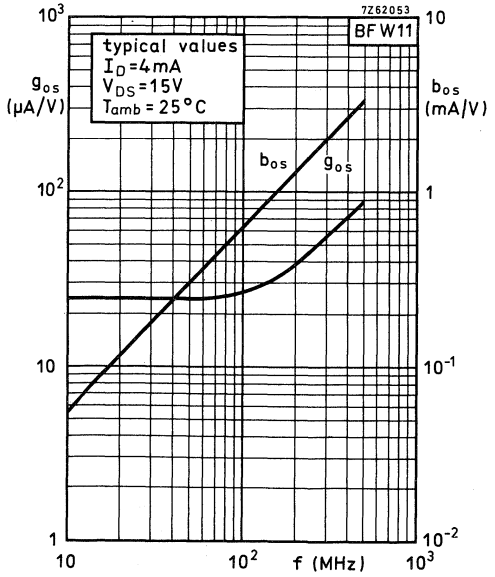

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)

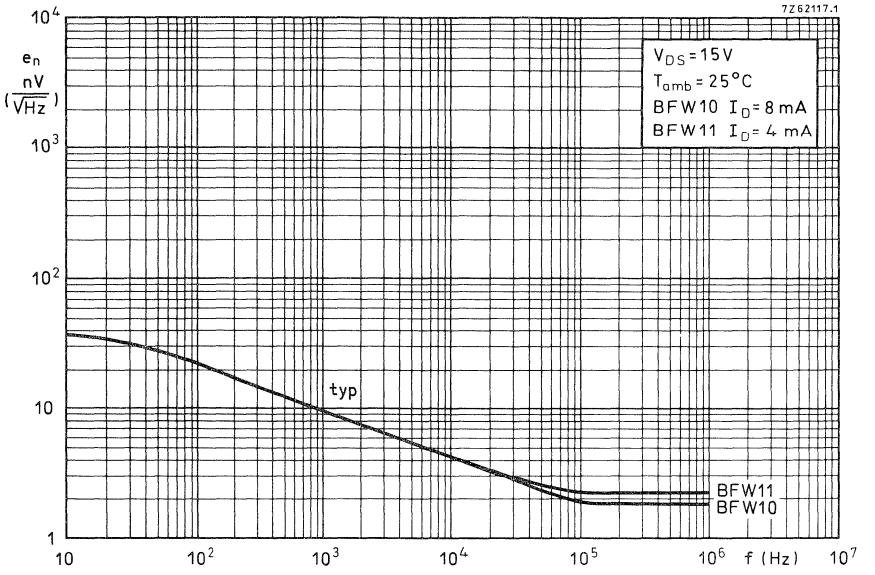

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)

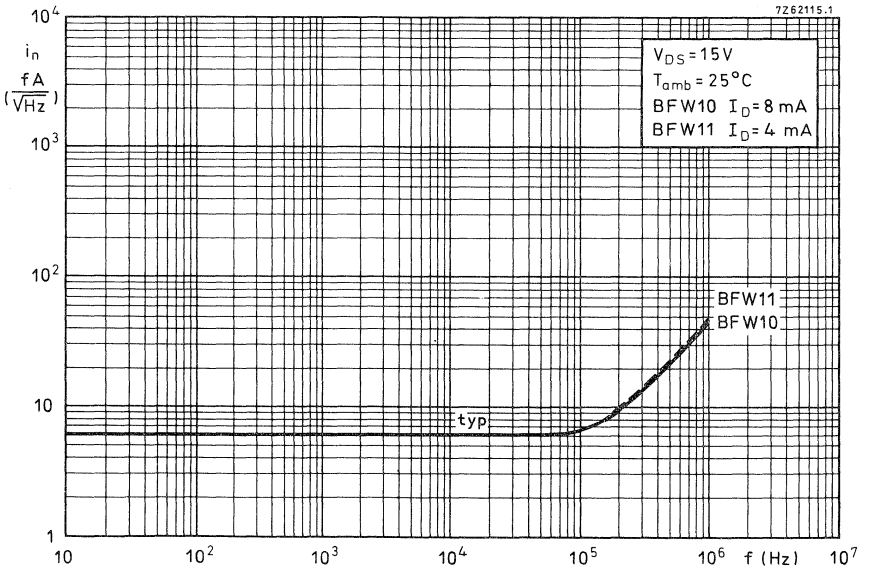

7Z62051
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

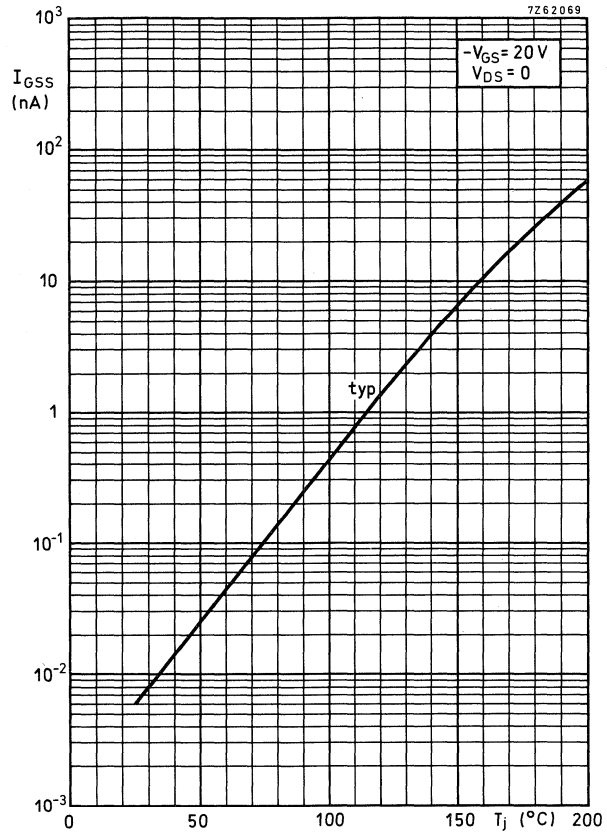

7Z62050
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
f (MHz)


7Z62052
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)


7Z62053
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)


7Z62117.1
10^4
e_n
$\frac{nV}{\sqrt{Hz}}$
10^3
10^2
10
1
typ
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62115.1
10^4
i_n
$\frac{fA}{\sqrt{Hz}}$
10^3
10^2
10
1
typ
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62069
$-V_{GS}$= 20 V
V_{DS} = 0
typ
I_{GSS} (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
			BFW12	**BFW13**	
Drain current		>	1	0,2	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	5	1,5	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mS
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

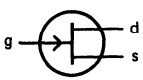
MECHANICAL DATA

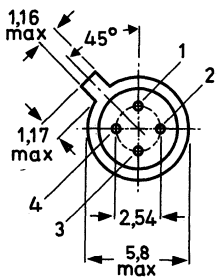
Dimensions in mm

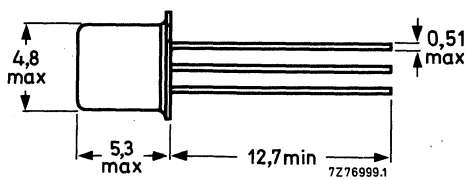
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Total power dissipation up to T_{amb} = 85 °C	P_{tot}	max.	150	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

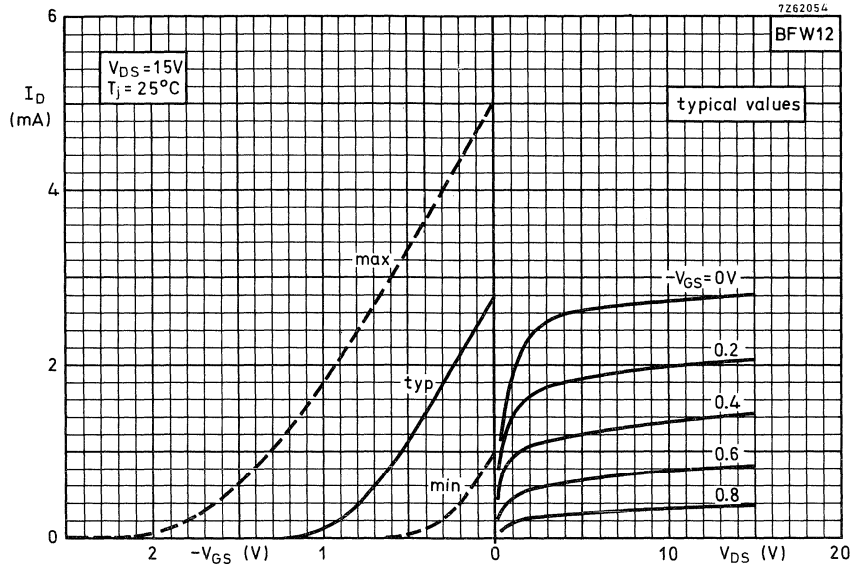
From junction to ambient	$R_{th\ j\text{-}a}$	=	590	K/W

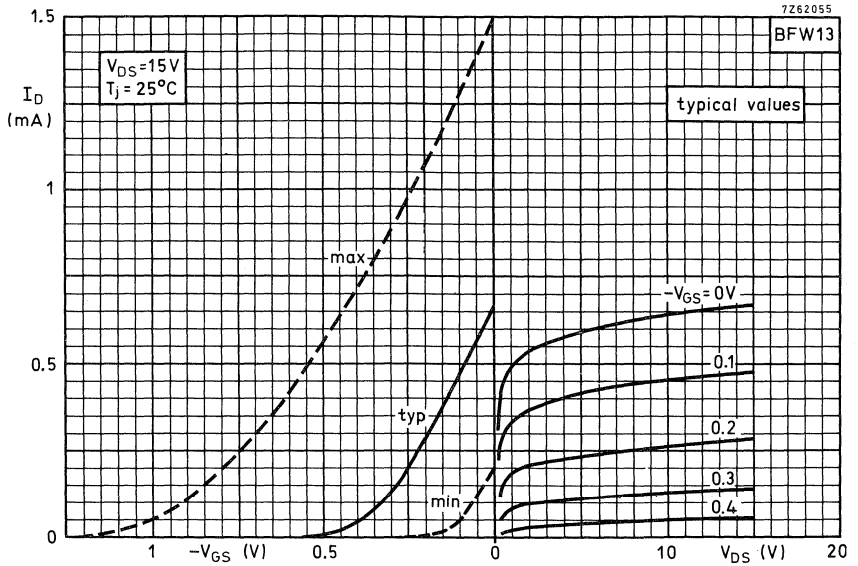
CHARACTERISTICS

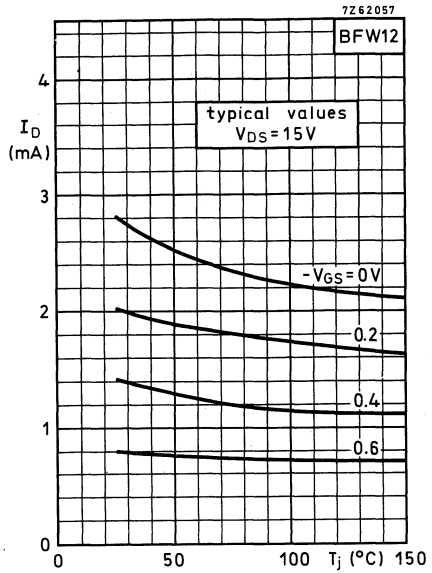
T_j = 25 °C unless otherwise specified

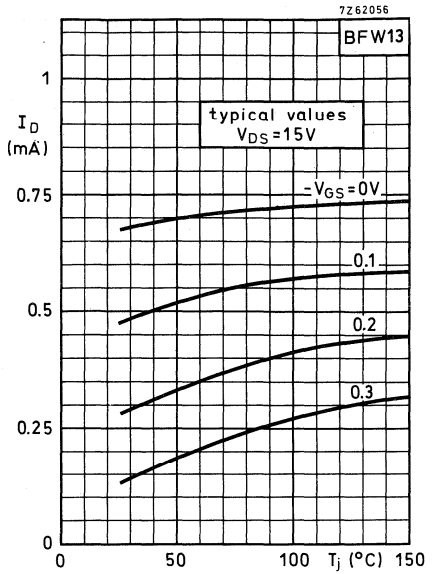
			BFW12	BFW13	
Gate cut-off currents					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	µA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 µA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mS
Output admittance	$\|y_{os}\|$	<	30	10	µS
V_{DS} = 15 V; I_D = 500 µA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mS
Output admittance	$\|y_{os}\|$	<	10	–	µS
V_{DS} = 15 V; I_D = 200 µA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mS
Output admittance	$\|y_{os}\|$	<	5	5	µS
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 µA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	µV

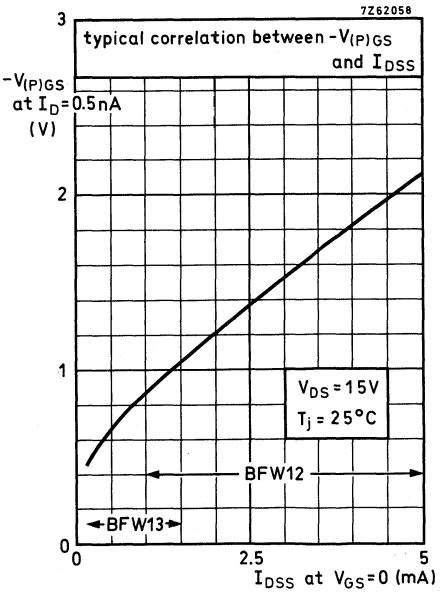
[1]) Measured under pulsed conditions.

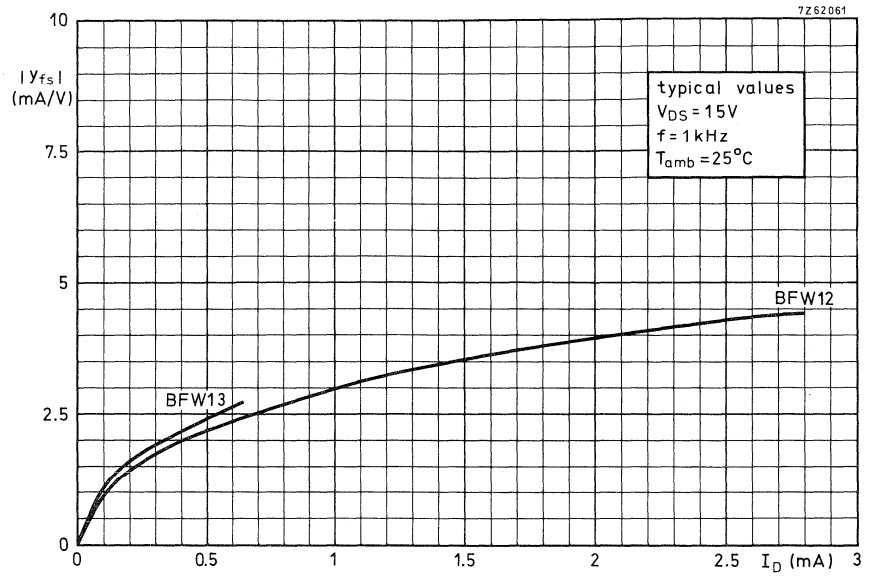

7Z62054
BFW12
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
2
$-V_{GS}$ (V)
1
0
10
V_{DS} (V)
20

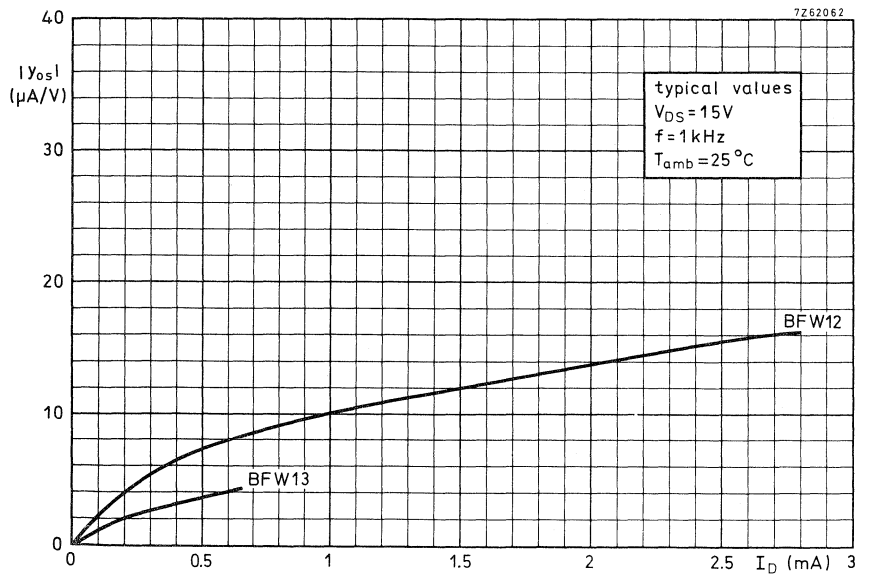

7Z62055
BFW13
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
1.5
1
0.5
0
max
typ
min
$-V_{GS}$ = 0V
0.1
0.2
0.3
0.4
1
$-V_{GS}$ (V)
0.5
0
10
V_{DS} (V)
20

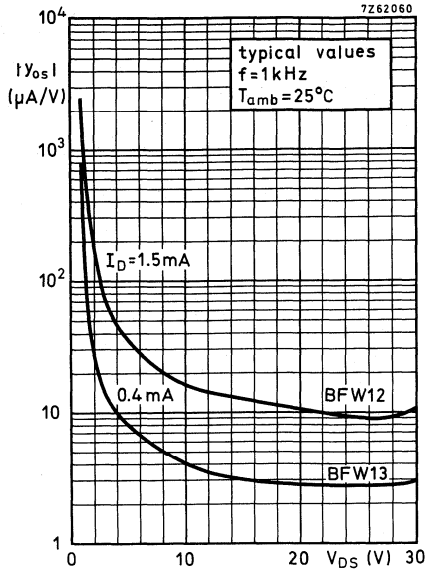

7Z62057
BFW12
typical values
V_{DS}=15V
I_D (mA)
4
3
2
1
0
-V_{GS}=0V
0.2
0.4
0.6
0
50
100
T_j (°C)
150

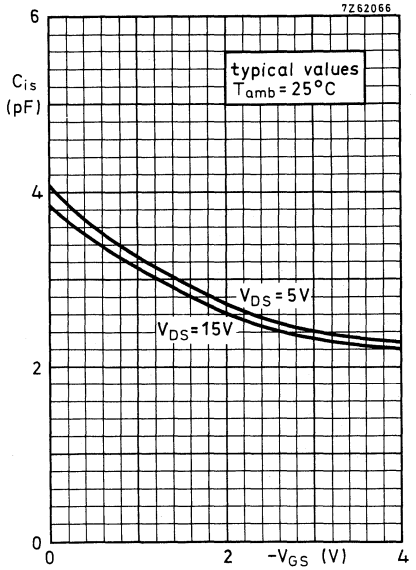

7Z62056
BFW13
typical values
V_{DS}=15V
I_D (mA)
1
0.75
0.5
0.25
0
-V_{GS}=0V
0.1
0.2
0.3
0
50
100
T_j (°C)
150

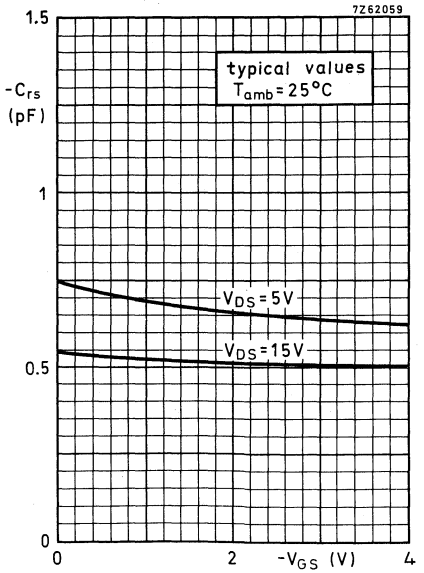

7Z62058
typical correlation between -$V_{(P)GS}$ and I_{DSS}
-$V_{(P)GS}$ at I_D=0.5nA (V)
3
2
1
0
V_{DS}=15V
T_j=25°C
BFW12
BFW13
0
2.5
5
I_{DSS} at V_{GS}=0 (mA)

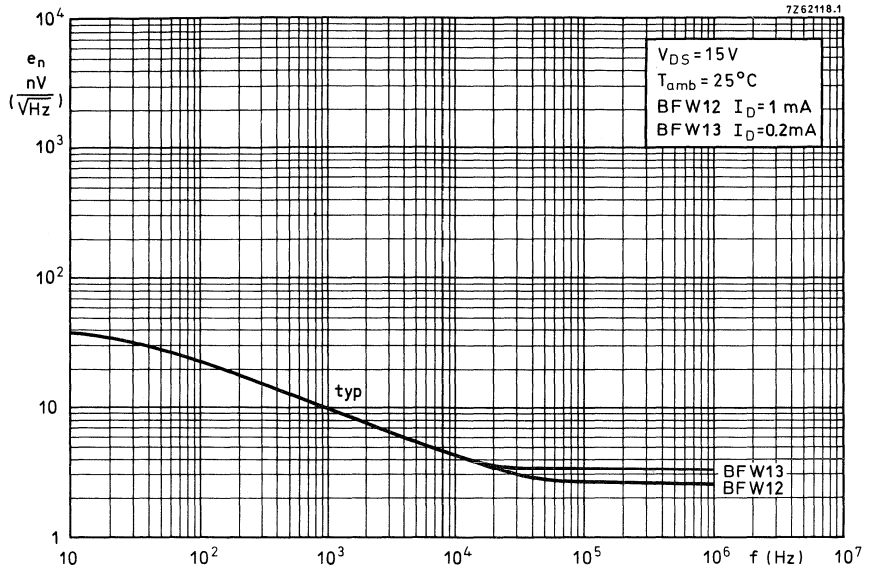

7Z62061
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

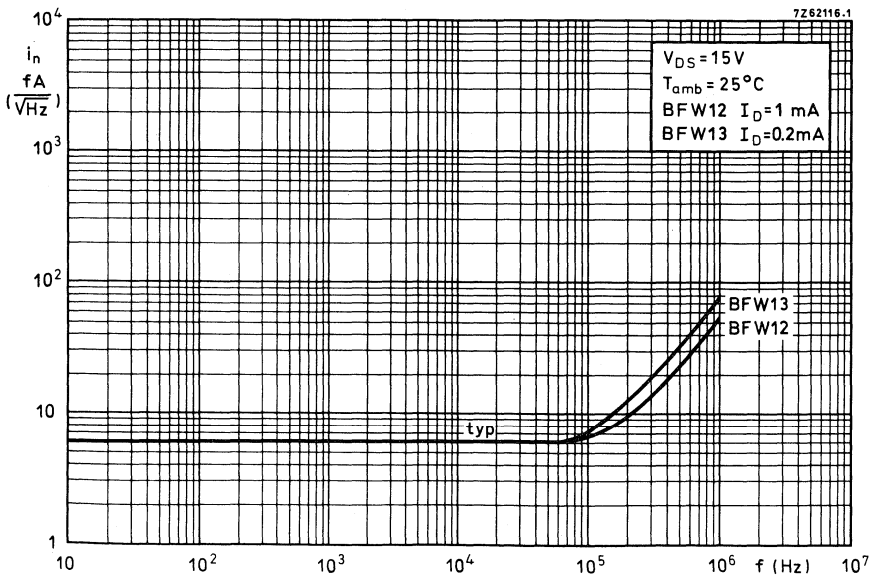

7Z62062
40
|yos|
(μA/V)
30
20
10
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

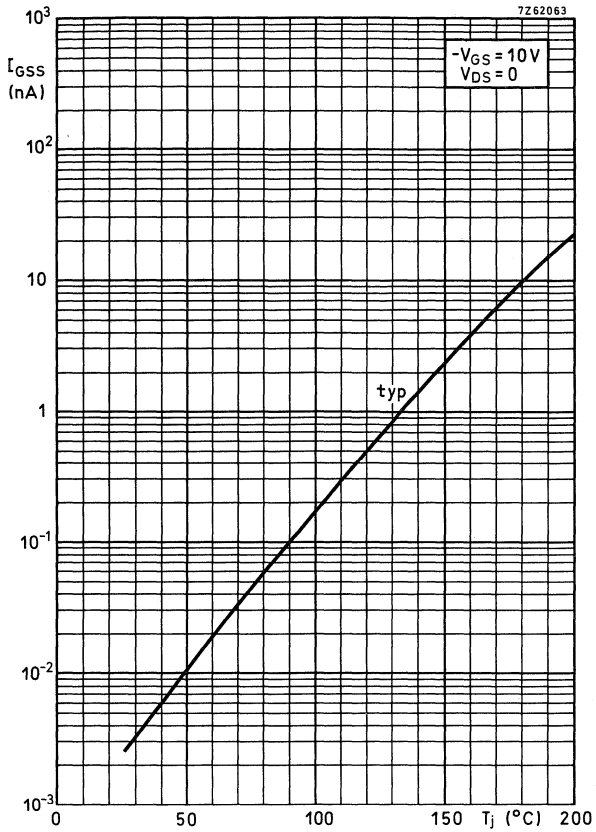

7Z62060
typical values
f=1kHz
T_{amb}=25°C
$|y_{os}|$
(μA/V)
10^4
10^3
10^2
10
1
I_D=1.5mA
0.4mA
BFW12
BFW13
0
10
20
V_{DS} (V)
30


7Z62066
typical values
T_{amb}=25°C
C_{is}
(pF)
6
4
2
0
V_{DS}=5V
V_{DS}=15V
0
2
$-V_{GS}$ (V)
4


7Z62059
typical values
T_{amb}=25°C
$-C_{rs}$
(pF)
1.5
1
0.5
0
V_{DS}=5V
V_{DS}=15V
0
2
$-V_{GS}$ (V)
4


7Z62118.1
10^4
e_n
nV
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2mA
typ
BFW13
BFW12
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62116.1
10^4
i_n
fA
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2mA
BFW13
BFW12
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62063
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10 V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source cut-off voltage I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2.0	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 10 MHz	$\|y_{fs}\|$	>	1.6	mS

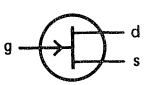
MECHANICAL DATA

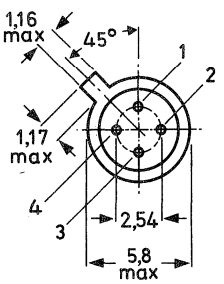
Dimensions in mm

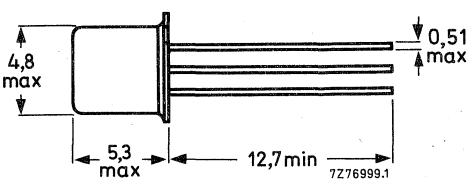
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	1.0	μA
Drain current*				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$		0.5 to 7.5	V
Gate-source cut-off voltage				
I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
y-parameters (common source)				
V_{DS} = 15 V; V_{GS} = 0				
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$		2.0 to 6.5	mS
at f = 10 MHz		>	1.6	mS
Output admittance at f = 1 kHz	$\|y_{os}\|$	<	85	μS
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	2,0	pF

* Measured under pulse conditions.

N-CHANNEL FETS

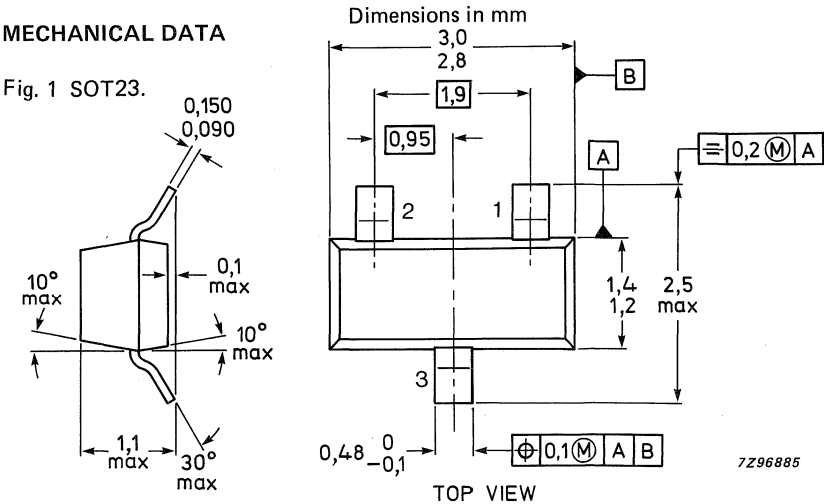
Symmetrical silicon n-channel depletion type junction field-effect transistors in a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power, chopper or switching applications in industrial service.

QUICK REFERENCE DATA

			BSR56	BSR57	BSR58	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250	250	250	mW
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source cut-off voltage						
V_{DS} = 15 V; I_D = 0.5 nA	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rs}	<	5	5	5	pF
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 20 mA; $-V_{GSM}$ = 10 V	t_{off}	<	25	–	–	ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	t_{off}	<	–	50	–	ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	t_{off}	<	–	–	100	ns

MECHANICAL DATA

Fig. 1 SOT23.



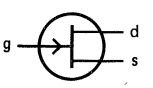
Note: Drain and source are interchangeable.

Marking code

BSR56 = M4p
BSR57 = M5p
BSR58 = M6p

Pinning

1 = drain
2 = source
3 = gate



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Drain-gate voltage	V_{DGO}	max.	40 V
Gate-source voltage	$-V_{GSO}$	max.	40 V
Forward gate current	I_{GF}	max.	50 mA
Total power dissipation up to T_{amb} = 40 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source cut-off current					
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	max.	1.0		nA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	max.	1.0		nA

			BSR56	BSR57	BSR58	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
		<	–	100	80	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	750	–	–	mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	500	–	mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	400	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0; T_a = 25 °C	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0	C_{rss}	<	5	5	5	pF

Notes

1. Mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Switching times

V_{DD} = 10 V; V_{GS} = 0
Conditions I_D and $-V_{GSM}$

			BSR56	BSR57	BSR58	
	I_D	=	20	10	5	mA
	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

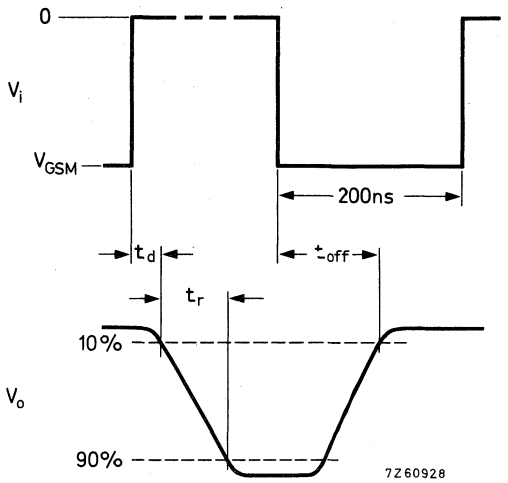


Fig. 2 Switching times waveforms.

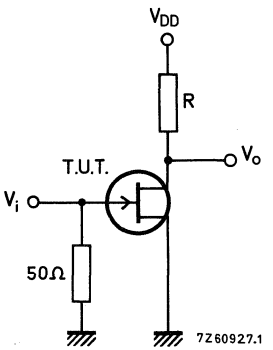


Fig. 3 Test circuit.

BSR56; R = 464 Ω
BSR57; R = 953 Ω
BSR58; R = 1910 Ω

Pulse generator

$t_r = t_f \leqslant 1$ ns
δ = 0.02
Z_o = 50 Ω

Oscilloscope

$t_r \leqslant 0.75$ ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2.5 pF

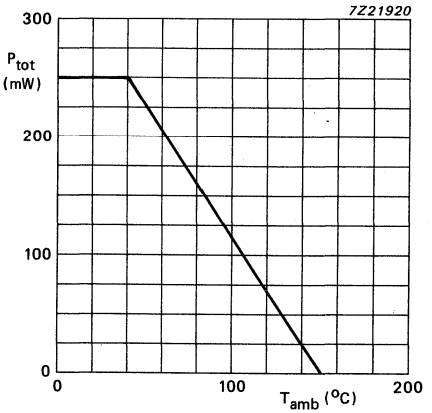


Fig.4 Power derating curve.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		350		mW
			BSV78	**BSV79**	**BSV80**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

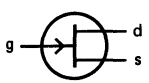
Dimensions in mm

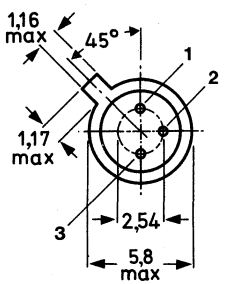
Fig. 1 TO-18.

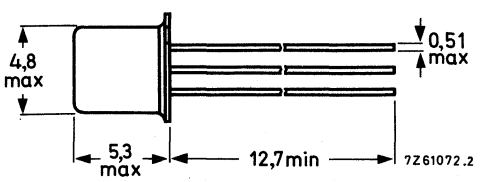
Gate connected to case

Pinning

1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350	mW
Storage temperature range	T_{stg}	−65 to +	175	°C
Operating junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			BSV78	BSV79	BSV80	
Gate cut-off currents						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<		0.25		nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<		0.5		μA
Drain cut-off current						
V_{DS} = 15 V; $-V_{GS}$ = 12 V	I_{DSX}	<		0.25		nA
V_{DS} = 15 V; $-V_{GS}$ = 12 V; T_j = 150 °C	I_{DSX}	<		0.5		μA
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
I_D = 1.5 μA; V_{DS} = 15 V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	500			mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<		400		mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS}$ = 10 V; V_{DS} = 0						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF

Switching times (see Fig. 2)

Turn-on time when switched from

$-V_{GSoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V (**BSV78**)
$-V_{GSoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V (**BSV79**)
$-V_{GSoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V (**BSV80**)

		BSV78	BSV79	BSV80	
delay time	t_d <	5	10	10	ns
rise time	t_r <	5	8	20	ns
turn-on time	t_{on} <	10	18	30	ns

Turn-off time when switched from

I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V (**BSV78**)
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V (**BSV79**)
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V (**BSV80**)

		BSV78	BSV79	BSV80	
fall time	t_f <	6	11	24	ns
storage time	t_s <	4	5	8	ns
turn-off time	t_{off} <	10	16	32	ns

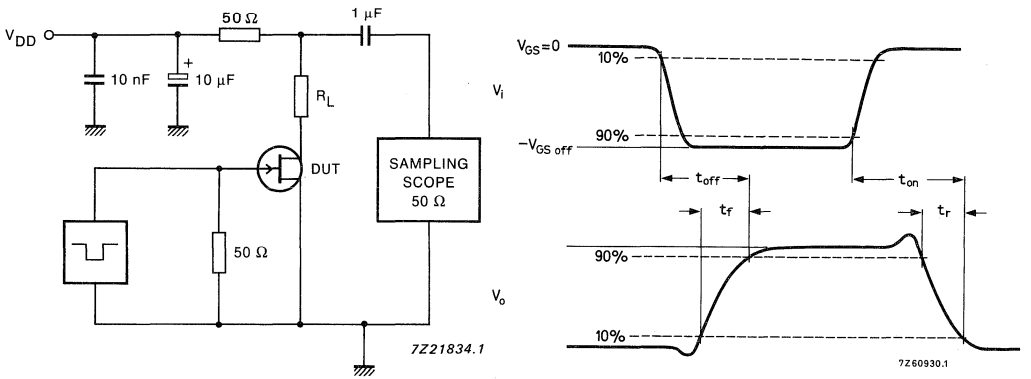


Fig. 2 Switching times test circuit and input and output waveforms.

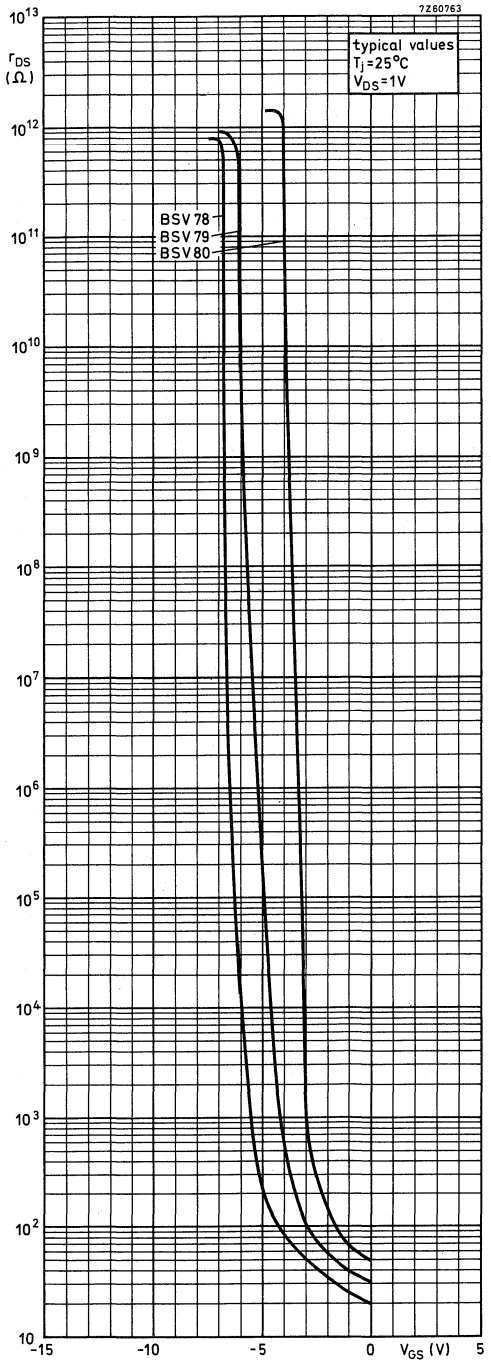
	BSV78	BSV79	BSV80	
R_L =	424	909	1885	Ω

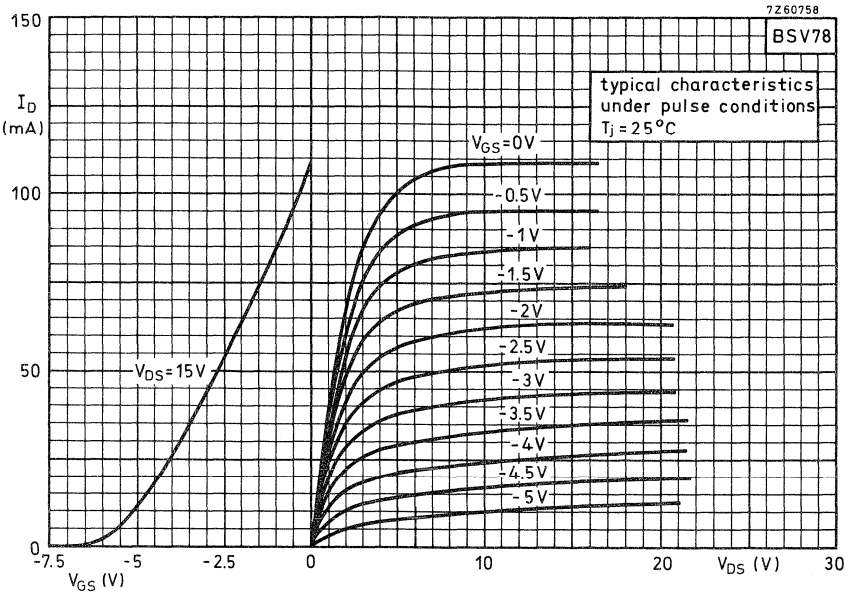
Pulse generator:

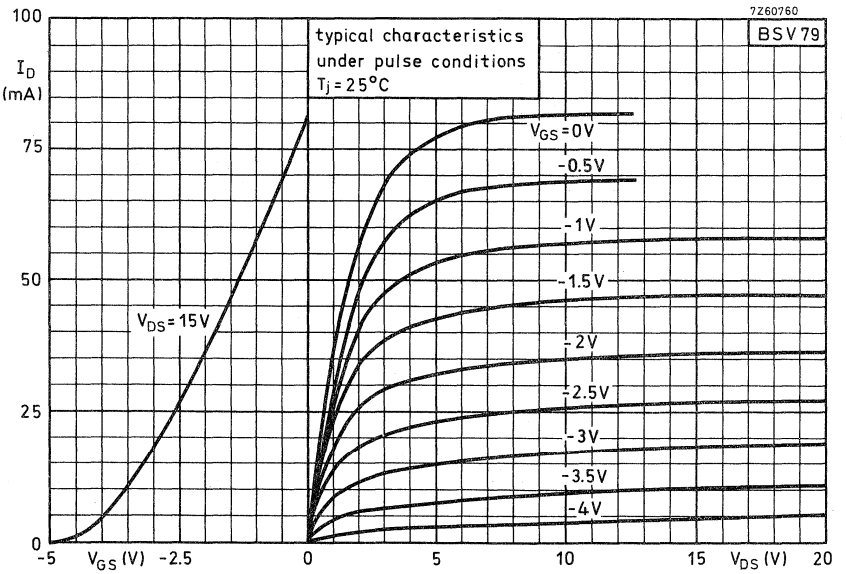
R_i = 50 Ω
t_r < 0.5 ns
t_f < 5 ns

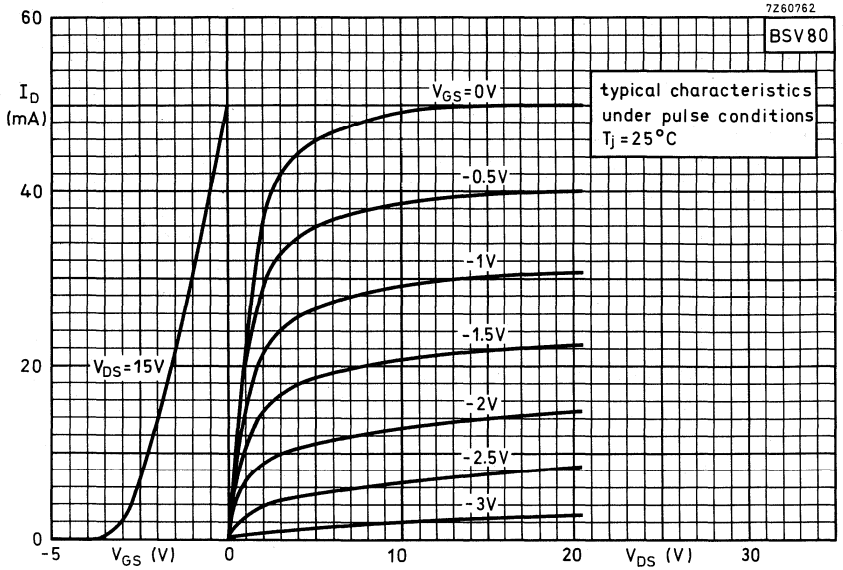
Oscilloscope:

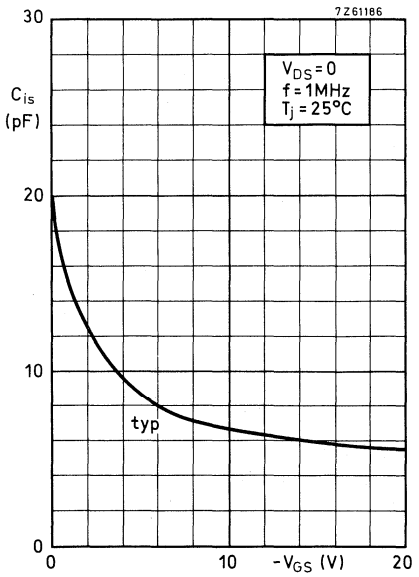
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

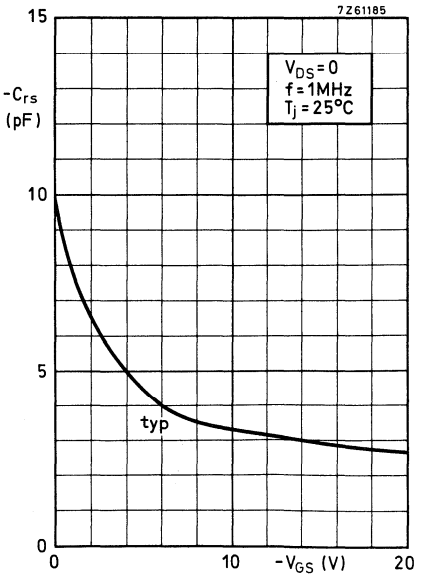

7Z60763
typical values
T_j=25°C
V_{DS}=1V
r_{DS} (Ω)
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
BSV78
BSV79
BSV80
-15
-10
-5
0
V_{GS} (V)
5

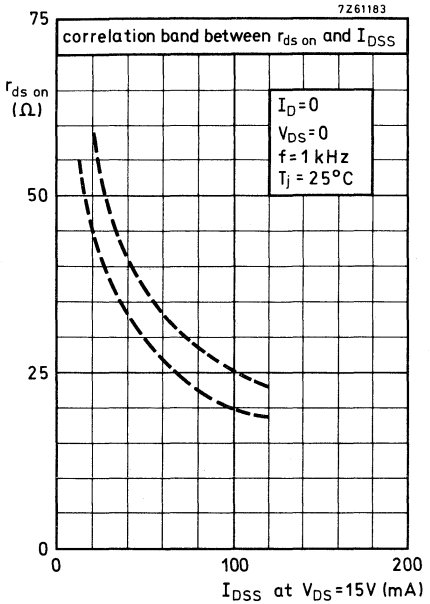

7Z60758
BSV78
typical characteristics
under pulse conditions
Tj = 25°C
ID (mA)
150
100
50
0
VGS=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V
VDS=15V
-7.5
-5
-2.5
VGS (V)
0
10
20
VDS (V)
30

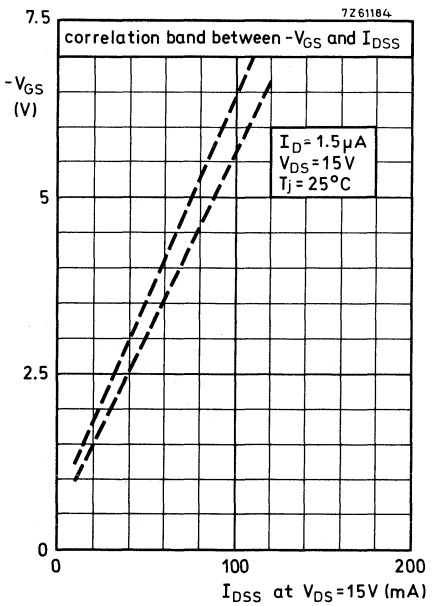

7Z60760
BSV79
typical characteristics
under pulse conditions
Tj = 25°C
ID (mA)
100
75
50
25
0
VGS=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
VDS=15V
-5
VGS (V)
-2.5
0
5
10
15
VDS (V)
20


7Z60762
BSV80
typical characteristics
under pulse conditions
T_j = 25 °C
I_D (mA)
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
V_{DS}=15V
V_{GS} (V)
V_{DS} (V)
60
40
20
0
-5
0
10
20
30


7Z61186
V_{DS} = 0
f = 1MHz
T_j = 25°C
C_{is} (pF)
typ
$-V_{GS}$ (V)
30
20
10
0
0
10
20


7Z61185
V_{DS} = 0
f = 1MHz
T_j = 25°C
$-C_{rs}$ (pF)
typ
$-V_{GS}$ (V)
15
10
5
0
0
10
20


7Z61183
correlation band between $r_{ds\ on}$ and I_{DSS}
$r_{ds\ on}$ (Ω)
75
50
25
0
I_D=0
V_{DS}=0
f=1 kHz
T_j=25°C
0
100
200
I_{DSS} at V_{DS}=15V (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
$-V_{GS}$ (V)
7.5
5
2.5
0
I_D=1.5 μA
V_{DS}=15V
T_j=25°C
0
100
200
I_{DSS} at V_{DS}=15V (mA)

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

J108/J109/J110
N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for J108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT54 envelope. They are intended for use in applications such as analog switches, choppers and commutators.

PINNING - SOT54

PIN	DESCRIPTION
1	gate
2	source
3	drain

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

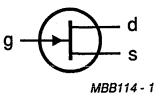


Fig 1. Symbol.

N-channel junction FETs J108/J109/J110

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	-	400	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	J108 J109 J110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 µA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 µA V_{DS} = 5 V	J108 J109 J110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	J108 J109 J110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (J108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (J109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (J110).

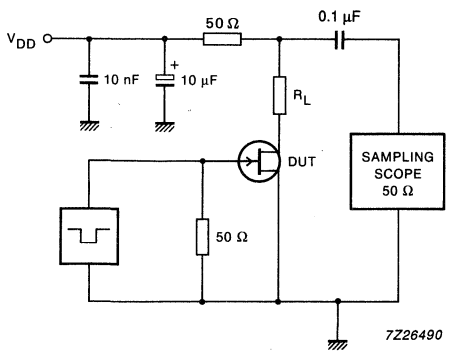


Fig.2 Switching circuit.

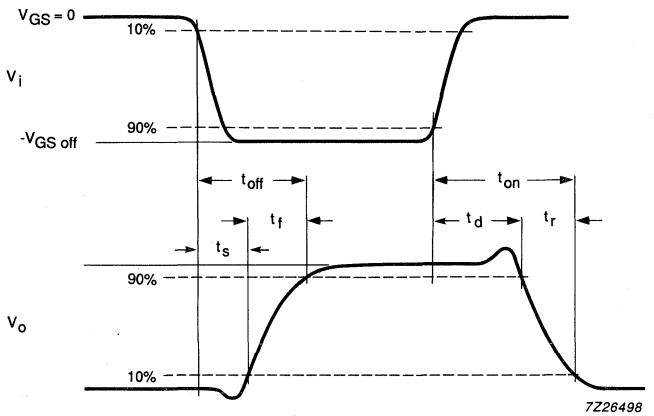


Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Dimensions in mm

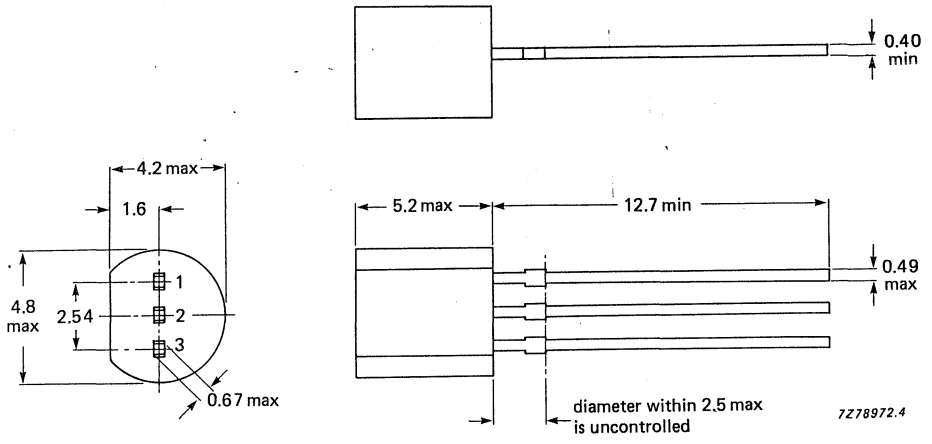


Fig.4 SOT54.

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

Features

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS\ on}$ at zero gate voltage

QUICK REFERENCE DATA

			J111	J112	J113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	400	400	mW
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

MECHANICAL DATA

Fig.1 TO-92.

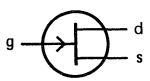
Dimensions in mm

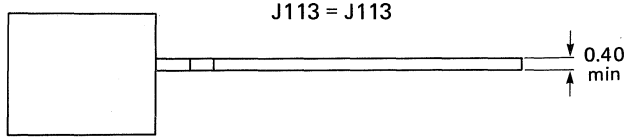
Marking code

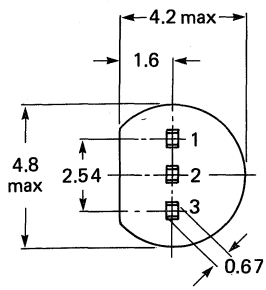
J111 = J111
J112 = J112
J113 = J113

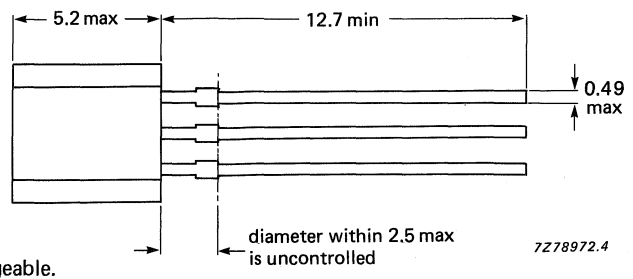
Pinning

1 = Gate
2 = Source
3 = Drain









Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Gate forward current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J111	J112	J113	
Gate reverse current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	1	1	1	nA
Drain cut-off current V_{DS} = 5 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	nA
Drain saturation current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	20	5	2	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage V_{DS} = 5 V; I_D = 1 μA	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance V_{DS} = 0.1 V; V_{GS} = 0	$R_{DS\ on}$	max.	30	50	100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{is}	typ.	6 pF
V_{DS} = $-V_{GS}$ = 0; f = 1 MHz	C_{is}	typ.	22 pF
		max.	28 pF
Feedback capacitance			
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	C_{rs}	typ.	3 pF
Switching times			
test conditions			
V_{DD} = 10 V; V_{GS} = 0 to V_{GSoff}			
$-V_{GS\ off}$ = 12 V; R_L = 750 Ω for J111			
$-V_{GS\ off}$ = 7 V; R_L = 1550 Ω for J112			
$-V_{GS\ off}$ = 5 V; R_L = 3150 Ω for J113			
Rise time	t_r	typ.	6 ns
Turn-on time	t_{on}	typ.	13 ns
Fall time	t_f	typ.	15 ns
Turn-off time	t_{off}	typ.	35 ns

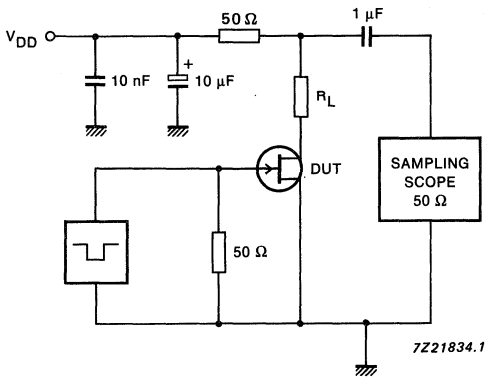


Fig.2 Switching times test circuit.

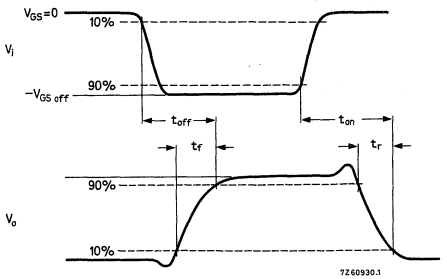


Fig.3 Input and output waveforms.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

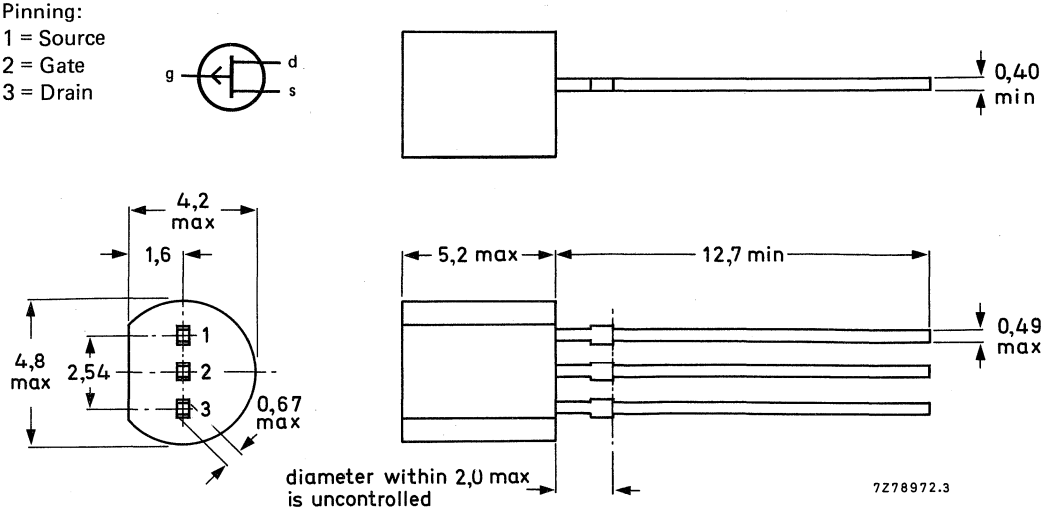
Drain-source voltage	$\pm V_{DS}$	max.	30				V
Gate-source voltage	V_{GSO}	max.	30				V
Gate current	$-I_G$	max.	50				mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400				mW
			J174	**J175**	**J176**	**J177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	85	125	250	300	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.

Pinning:
1 = Source
2 = Gate
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (DC)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.	400	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			J174	J175	J176	J177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	max.	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	min.	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = 15 V	$V_{GS\,off}$	min.	5	3	1	0.8	V
		max.	10	6	4	2.25	V
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	R_{DSon}	max.	85	125	250	300	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)			J174	BSJ175	J176	J177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage time	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

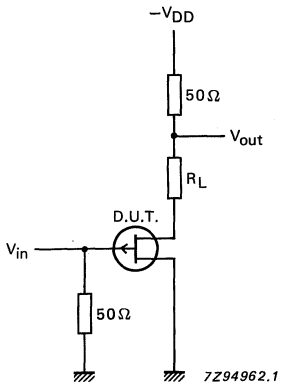


Fig. 2 Switching times test circuit.

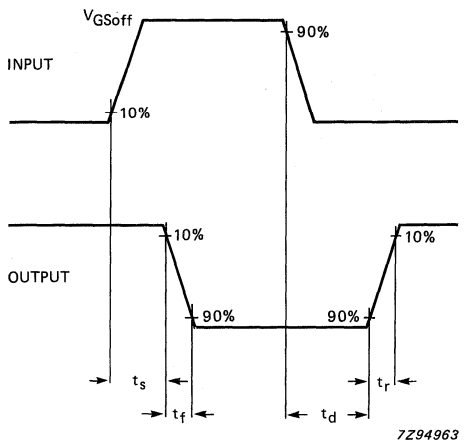


Fig. 3 Input and output waveforms;
$t_d + t_r = t_{on}$
$t_s + t_f = t_{off}$.

N-CHANNEL FETS

Symmetrical silicon n-channel depletion type junction field-effect transistors on a plastic microminiature envelope intended for application in thick and thin-film circuits. The transistors are intended for low-power chopper or switching applications in industry.

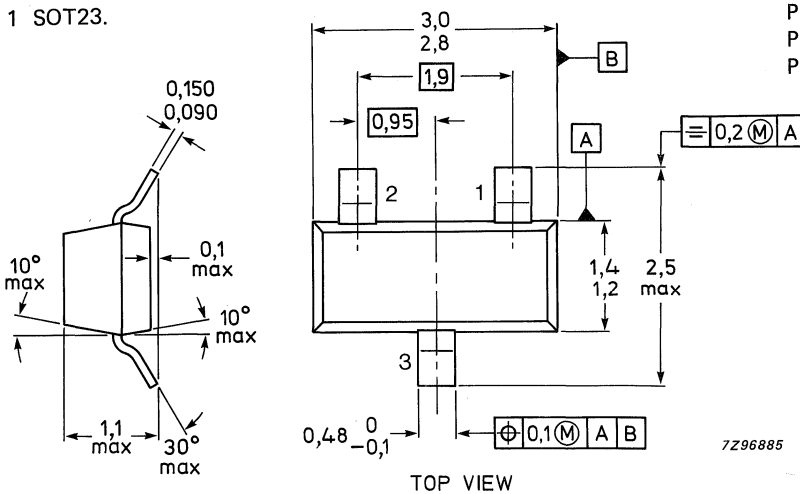
QUICK REFERENCE DATA

			PMBF4391	PMBF4392	PMBF4393	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$R_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz $-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	3.5	3.5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns

MECHANICAL DATA

Fig. 1 SOT23.

Dimensions in mm

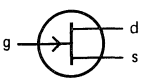


Marking code

PMBF4391 = p6J
PMBF4392 = p6K
PMBF4393 = p6G

Pinning

1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate-source voltage					
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1		V
Gate-source cut-off current					
V_{DS} = 0 V; $-V_{GS}$ = 20 V	$-I_{GSS}$	<	0.1		nA
V_{DS} = 0 V; $-V_{GS}$ = 20 V; T_{amb} = 150 °C	$-I_{GSS}$	<	0.2		μA

			PMBF4391	PMBF4392	PMBF4393	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
		<	150	75	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4	2	0.5	V
		<	10	5	3	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6 mA; V_{GS} = 0	V_{DSon}	<		0.4	–	V
I_D = 3 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 0; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$r_{ds\ on}$	<	30	60	100	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

			PMBF4391	PMBF4392	PMBF4393
Drain cut-off current					
$-V_{GS}$ = 12 V } V_{DS} = 20 V	I_{DSX}	<	0.1	–	– nA
$-V_{GS}$ = 7 V } V_{DS} = 20 V	I_{DSX}	<	–	0.1	– nA
$-V_{GS}$ = 5 V } V_{DS} = 20 V	I_{DSX}	<	–	–	0.1 nA
$-V_{GS}$ = 12 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	0.2	–	– μA
$-V_{GS}$ = 7 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.2	– μA
$-V_{GS}$ = 5 V } V_{DS} = 20 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.2 μA
y-parameters (common source)					
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_{amb} = 25 °C					
Input capacitance	C_{is}	<	14	14	14 pF
Feedback capacitance					
$-V_{GS}$ = 12 V	C_{rs}	<	3.5	–	– pF
$-V_{GS}$ = 7 V	C_{rs}	<	–	3.5	– pF
$-V_{GS}$ = 5 V	C_{rs}	<	–	–	3.5 pF
Switching times					
V_{DD} = 10 V; V_{GS} = 0					
Conditions I_D and $-V_{GSoff}$	I_D	=	12	6	3 mA
	$-V_{GS\,off}$	=	12	7	5 V
	R_L	=	750	1550	3150 Ω
Rise time	t_r	<	5	5	5 ns
Turn on time	t_{on}	<	15	15	15 ns
Fall time	t_f	<	15	20	30 ns
Turn off time	t_{off}	<	20	35	50 ns

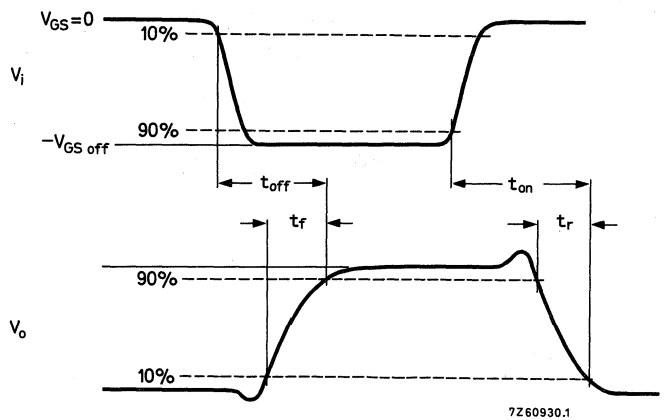
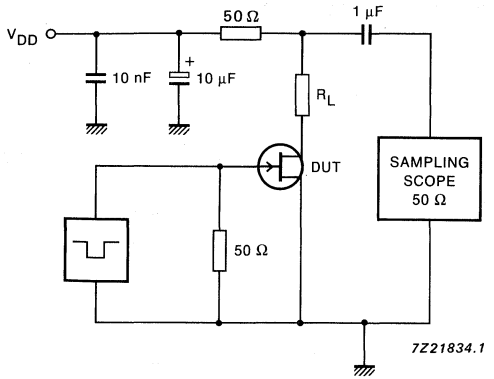


Fig.2 Switching times waveforms.



Pulse generator:

t_r	<	0.5 ns
t_f	<	0.5 ns
t_p	=	100 μs
δ	=	0.01

Oscilloscope:

R_i	=	50 Ω

Fig. 3 Test circuit.

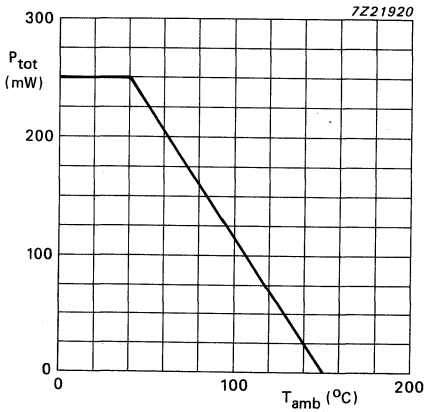


Fig.4 Power derating curve.

Data sheet	
status	Preliminary specification
date of issue	October 1990

PMBFJ108/PMBFJ109/ PMBFJ110

N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for PMBFJ108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in applications such as analog switches, choppers and commutators, and in audio amplifiers.

PIN CONFIGURATION

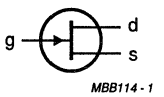


Fig.1 Symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	-	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Notes

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	V_{GS} = −10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	PMBFJ108 PMBFJ109 PMBFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 μA V_{DS} = 5 V	PMBFJ108 PMBFJ109 PMBFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	PMBFJ108 PMBFJ109 PMBFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PMBFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PMBFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PMBFJ110).

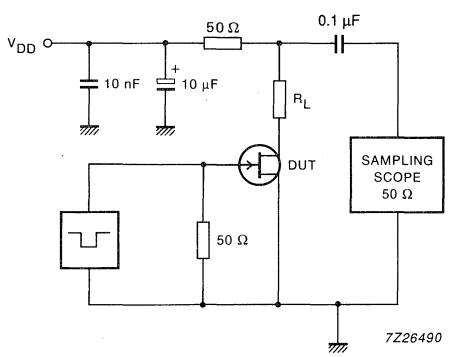


Fig.2 Switching circuit.

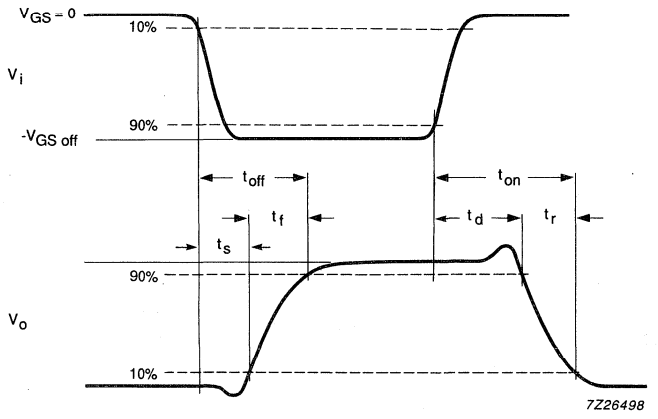
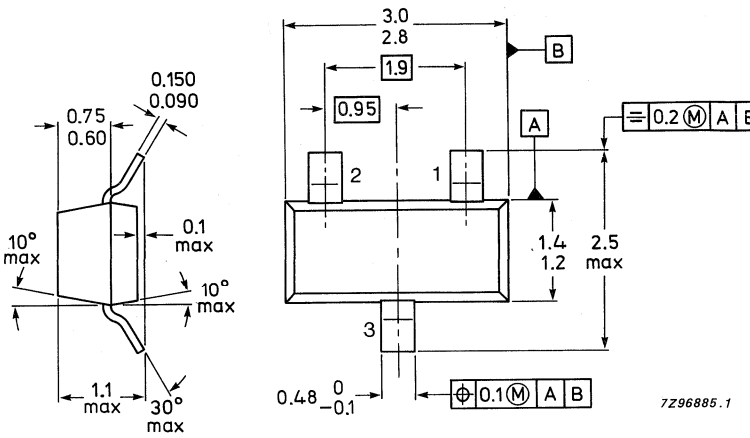


Fig.3 Input and output waveforms.

N-channel junction FETs PMBFJ108/PMBFJ109/PMBFJ110

PACKAGE OUTLINE

Dimensions in mm



TOP VIEW

Marking code:

PMBFJ108 = p08
PMBFJ109 = p09
PMBFJ110 = p10

Fig.4 SOT23.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

PMBFJ111/PMBFJ112/ PMBFJ113

N-channel junction FETs

FEATURES

- High-speed switching
- Low $R_{DS(on)}$ at zero gate voltage (< 30 Ω for PMBFJ111)
- Interchangeability of drain and source connections.

DESCRIPTION

Silicon n-channel junction field-effect transistors in a surface-mount SOT23 envelope. They are intended for use in applications such as analog switches, choppers, commutators, multiplexers and thin and thick film hybrids.

PIN CONFIGURATION

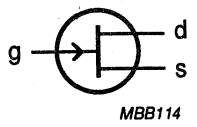


Fig.1 Symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	drain
2	source
3	gate

Note

1. Drain and source are interchangeable.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
$-V_{GSO}$	gate-source voltage		-	40	V
$-V_{GDO}$	gate-drain voltage		-	40	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C note 1	-	300	mW
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL CHARACTERISTICS

$T_j = P(R_{th\ j\text{-}t} + R_{th\ t\text{-}s} + R_{th\ s\text{-}a}) + T_{amb}$

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	430	K/W
$R_{th\ j\text{-}a}$	from junction to ambient (note 2)	500	K/W

Notes

1. Mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Mounted on printed circuit board.

STATIC CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS} = 15$ V $V_{DS} = 0$		-	1	nA
I_{DSS}	drain current	$V_{GS} = 0$ $V_{DS} = 15$ V	PMBFJ111 PMBFJ112 PMBFJ113	20 5 2	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G = 1$ µA $V_{DS} = 0$		40	-	V
$-V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1$ µA $V_{DS} = 5$ V	PMBFJ111 PMBFJ112 PMBFJ113	3 1 0.5	10 5 3	V
$R_{DS(on)}$	drain-source on-resistance	$V_{GS} = 0$ V $V_{DS} = 0.1$ V	PMBFJ111 PMBFJ112 PMBFJ113	- - -	30 50 100	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{iss}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	6	-	pF
		V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	22	28	pF
C_{rss}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	3	-	pF
Switching times (see Fig.2)					
t_r	rise time	note 1	6	-	ns
t_{on}	turn-on time	note 1	13	-	ns
t_f	fall time	note 1	15	-	ns
t_{off}	turn-off time	note 1	35	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 10 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 750 Ω (PMBFJ111);
   $-V_{GS(off)}$ = 7 V, R_L = 1550 Ω (PMBFJ112);
   $-V_{GS(off)}$ = 5 V, R_L = 3150 Ω (PMBFJ113).

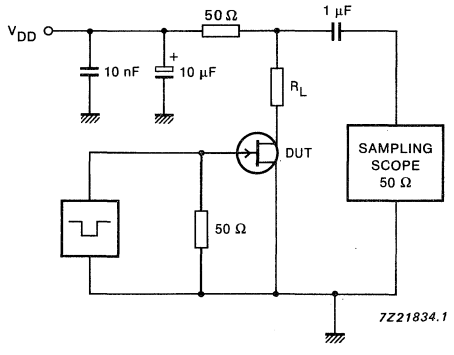


Fig.2 Switching circuit.

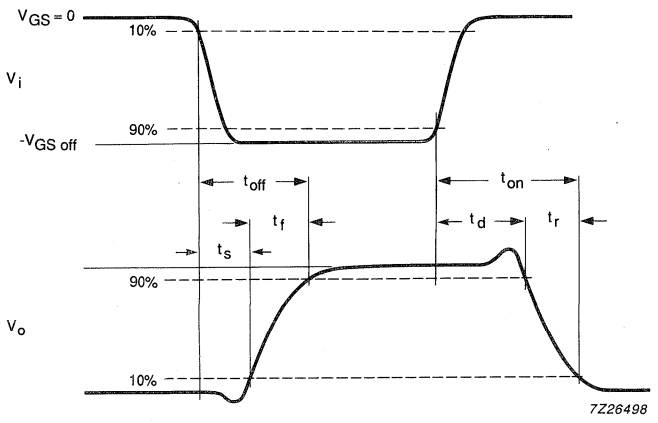


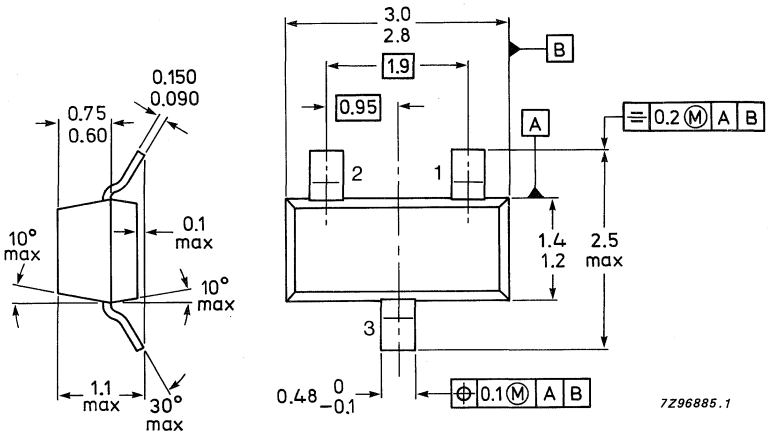
Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Dimensions in mm

Marking code:

PMBFJ111 = p11
PMBFJ112 = p12
PMBFJ113 = p13



TOP VIEW

See also soldering recommendations

Fig.4 SOT23.

P-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Silicon symmetrical p-channel junction FETs in plastic microminiature SOT-23 envelopes.

They are intended for application with analogue switches, choppers, commutators etc. using SMD technology.

A special feature is the interchangeability of the drain and source connections.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		30		V
Gate-source voltage	V_{GSO}	max.		30		V
Gate current	$-I_G$	max.		50		mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		300		mW
		PMBFJ174	**175**	**176**	**177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	> 20	7	2	1,5	mA
		< 135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	< 85	125	250	300	Ω

MECHANICAL DATA

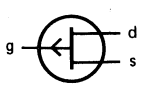
Dimensions in mm

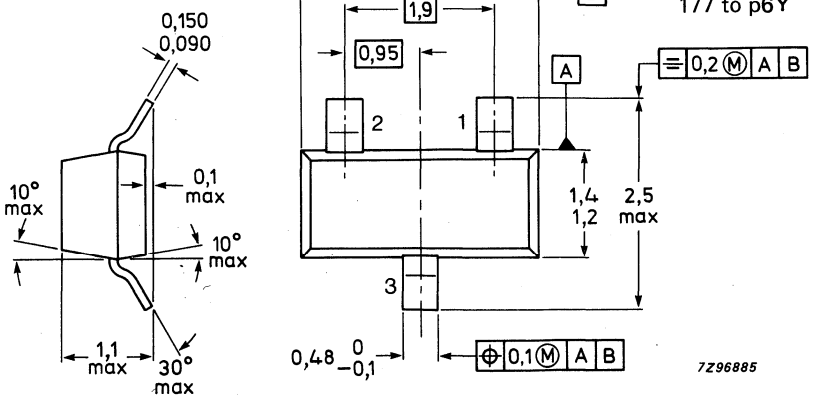
Fig. 1 SOT-23.

Marking codes:

174 to p6X
175 to p6W
176 to p6S
177 to p6Y

Pinning:
1 = Drain
2 = Source
3 = Gate





TOP VIEW

Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	V_{GSO}	max.	30	V
Gate-drain voltage	V_{GDO}	max.	30	V
Gate current (d.c.)	$-I_G$	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PMBFJ174	175	176	177	
Gate cut-off current $-V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	<	1	1	1	1	nA
Drain cut-off current $-V_{DS}$ = 15 V; $-V_{GS}$ = 10 V	$-I_{DSX}$	<	1	1	1	1	nA
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	>	20	7	2	1,5	mA
		<	135	70	35	20	mA
Gate-source breakdown voltage I_G = 1 μA; V_{DS} = 0	$V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source cut-off voltage $-I_D$ = 10 nA; V_{DS} = 15 V	$V_{GS\,off}$	>	5	3	1	0,8	V
		<	10	6	4	2,25	V
Drain-source ON-resistance $-V_{DS}$ = 0,1 V; V_{GS} = 0	$R_{DS\,on}$	<	85	125	250	300	Ω

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Input capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{is}	typ.		8		pF
$-V_{GS}$ = V_{DS} = 0	C_{is}	typ.		30		pF
Feedback capacitance, f = 1 MHz						
$-V_{GS}$ = 10 V; V_{DS} = 0 V	C_{rs}	typ.		4		pF

Switching times (see Fig. 2 + 3)		PMBFJ174		175	176	177	
Delay time	t_d	typ.	2	5	15	20	ns
Rise time	t_r	typ.	5	10	20	25	ns
Turn-on time	t_{on}	typ.	7	15	35	45	ns
Storage temperature	t_s	typ.	5	10	15	20	ns
Fall time	t_f	typ.	10	20	20	25	ns
Turn-off time	t_{off}	typ.	15	30	35	45	ns
Test conditions:	$-V_{DD}$		10	6	6	6	V
	$V_{GS\,off}$		12	8	6	3	V
	R_L		560	1200	2000	2900	Ω
	$V_{GS\,on}$		0	0	0	0	V

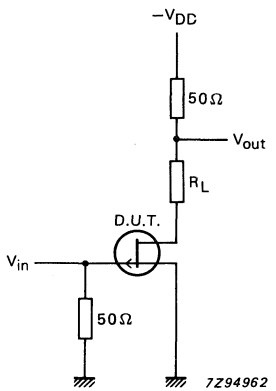


Fig. 2 Switching times test circuit

Rise time input voltage < 1 ns

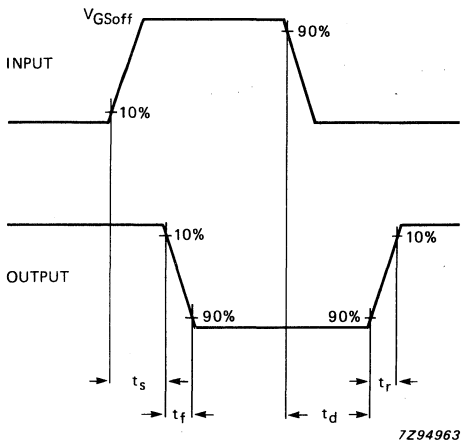


Fig. 3 Input and output waveforms

$t_d + t_r = t_{on}$

$t_s + t_f = t_{off}$

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360		mW
			PN4391	PN4392	PN4393
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5 mA
Gate-source cut-off voltage V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\,off}$	min.	4	2	0.5 V
		max.	10	5	3 V
Drain-source on-resistance I_D = 1 mA; V_{GS} = 0	$R_{DS\,on}$	max.	30	60	100 Ω

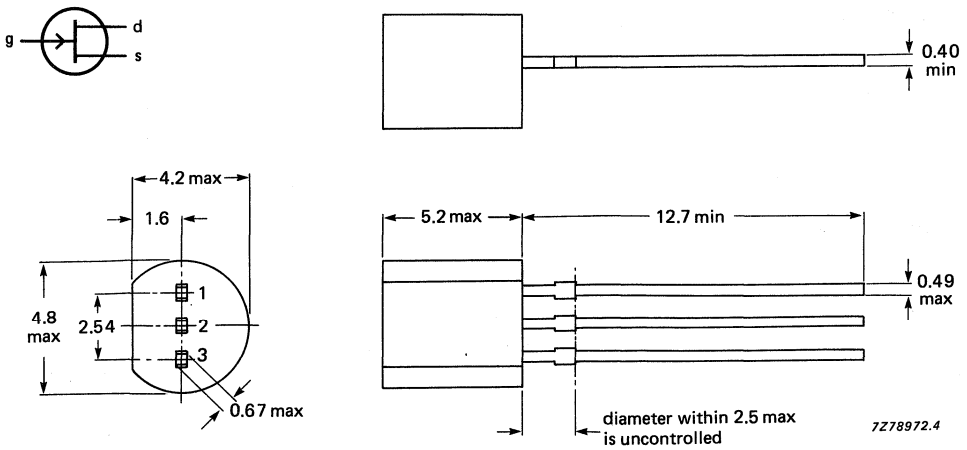
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92.

Pinning

1 = Gate
2 = Source
3 = Drain



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate-drain voltage	$-V_{GDO}$	max.	40	V
Forward gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	350 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Reverse gate current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	1.0	1.0	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 100 °C	$-I_{GSS}$	max.	200	200	200	nA
Drain cut-off current						
$-V_{GS}$ = 12 V; V_{DS} = 20 V	I_{DSX}	max.	1.0			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V	I_{DSX}	max.		1.0		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V	I_{DSX}	max.			1.0	nA
$-V_{GS}$ = 12 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.	200			nA
$-V_{GS}$ = 7 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.		200		nA
$-V_{GS}$ = 5 V; V_{DS} = 20 V; T_{amb} = 100 °C	I_{DSX}	max.			200	nA
Drain saturation current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	min.	50	25	5	mA
		max.	150	100	60	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	40	40	40	V
Gate-source cut-off voltage						
V_{DS} = 20 V; I_D = 1 nA	$-V_{GS\ off}$	min.	4.0	2.0	0.5	V
		max.	10	5.0	3.0	V
Drain-source on-resistance						
I_D = 1 mA; V_{GS} = 0	$R_{DS\ on}$	max.	30	60	100	Ω
Drain-source on-voltage						
V_{GS} = 0; I_D = 12 mA	$V_{DS\ on}$	max.	0.4			V
V_{GS} = 0; I_D = 6 mA	$V_{DS\ on}$	max.		0.4		V
V_{GS} = 0; I_D = 3 mA	$V_{DS\ on}$	max.			0.4	V

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PN4391	PN4392	PN4393	
Drain-source on-resistance						
V_{DS} = 0; V_{GS} = 0; f = 1 kHz; T_a = 25 °C	$R_{DS\,on}$	max.	30	60	100	Ω
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0; f = 1 MHz; T_a = 25 °C	C_{iss}	max.	16	16	16	pF
Feedback capacitance						
V_{DS} = 0; $-V_{GS}$ = 12 V } f = 1 MHz	C_{rss}	max.	5			pF
V_{DS} = 0; $-V_{GS}$ = 7 V } f = 1 MHz	C_{rss}	max.		5		pF
V_{DS} = 0; $-V_{GS}$ = 5 V } f = 1 MHz	C_{rss}	max.			5	pF
Switching times						
test conditions						
V_{DD} = 10 V; V_{GS} = 0 to $V_{GS\,off}$	I_D	=	12	6.0	3.0	mA
	$-V_{GS\,off}$	=	12	7.0	5.0	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	max.	5	5	5	ns
Turn-on time	t_{on}	max.	15	15	15	ns
Fall time	t_f	max.	15	20	30	ns
Turn-off time	t_{off}	max.	20	35	50	ns

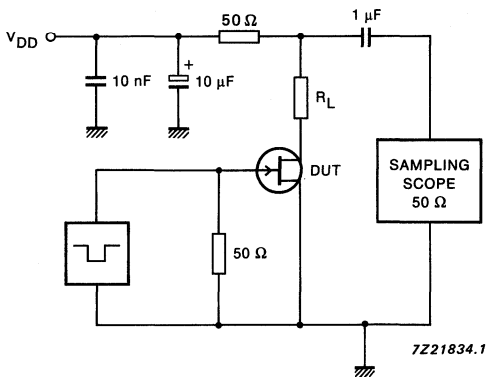


Fig.2 Switching times test circuit.

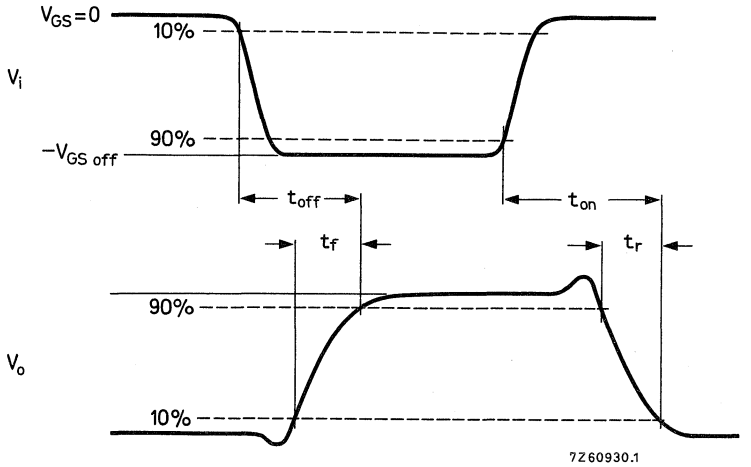


Fig.3 Input and output waveforms.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

PZFJ108/PZFJ109/PZFJ110

N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for PZFJ108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT223 envelope. They are intended for use in applications such as analog switches, choppers and commutators, as well as in audio amplifiers.

PINNING – SOT223

PIN	DESCRIPTION
1	drain
2	gate
3	source
4	gate

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

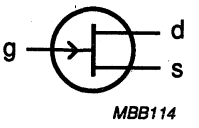


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C (note 1)	-	1.5	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy PCB, 40 mm x 40 mm x 1.5 mm. Mounting pad for the gate lead minimum 6 cm^2.

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	PZFJ108 PZFJ109 PZFJ110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 µA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 µA V_{DS} = 5 V	PZFJ108 PZFJ109 PZFJ110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	PZFJ108 PZFJ109 PZFJ110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Figs. 2 and 3)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (PZFJ108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (PZFJ109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (PZFJ110).

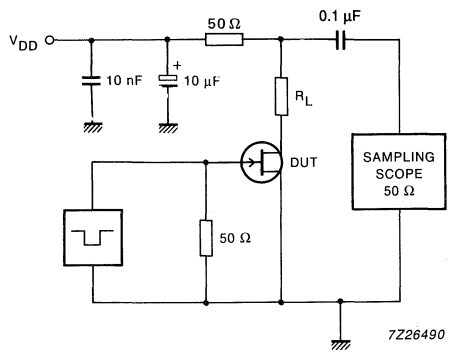


Fig.2 Switching circuit.

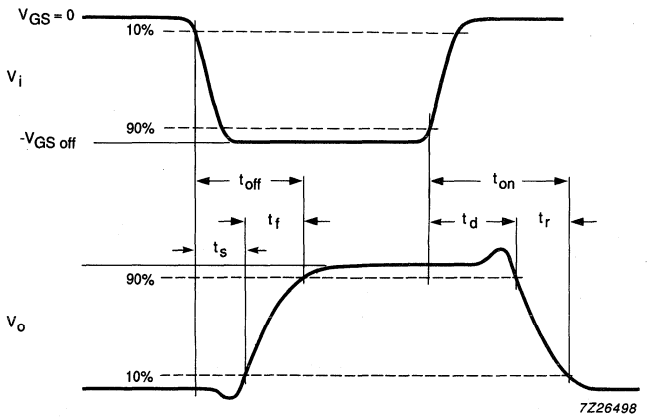
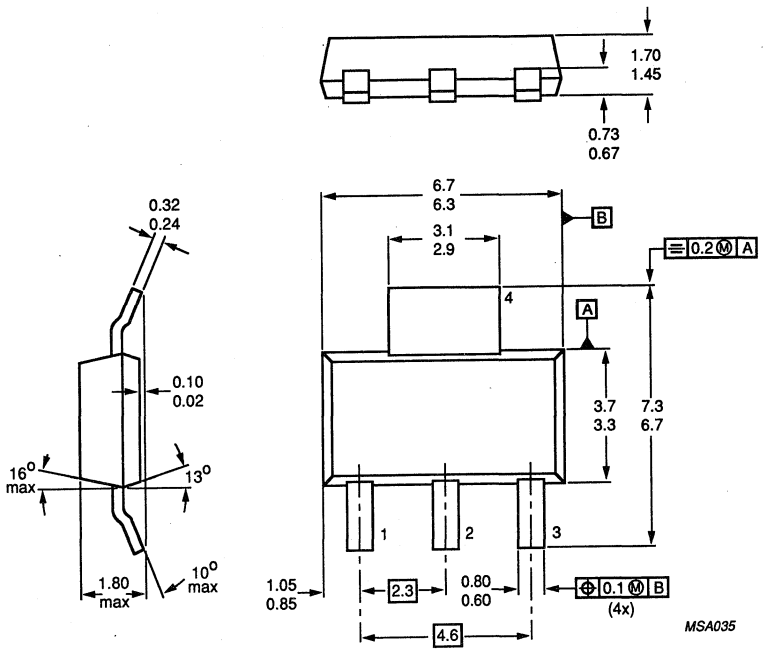


Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Dimensions in mm



Marking code:
PZFJ108 = ZFJ108
PZFJ109 = ZFJ109
PZFJ110 = ZFJ110

Fig.4 SOT223.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N3819
N-channel J-FET

FEATURES

- Low cost
- Specified at 100 MHz
- Automatic insertion package.

DESCRIPTION

N-channel junction field-effect transistor in a plastic TO-92 envelope. It is intended for use in general purpose amplifiers and for analog switching.

PINNING - TO-92

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION

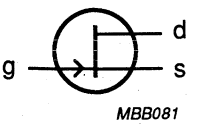


Fig.1 Symbol.

N-channel J-FET 2N3819

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage	open drain $I_D = 0$	-	25	V
V_{DGO}	drain-gate voltage	open source $I_S = 0$	-	25	V
I_G	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	-	360	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	347	K/W

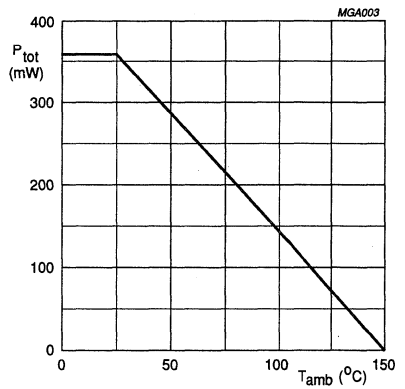


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel J-FET 2N3819

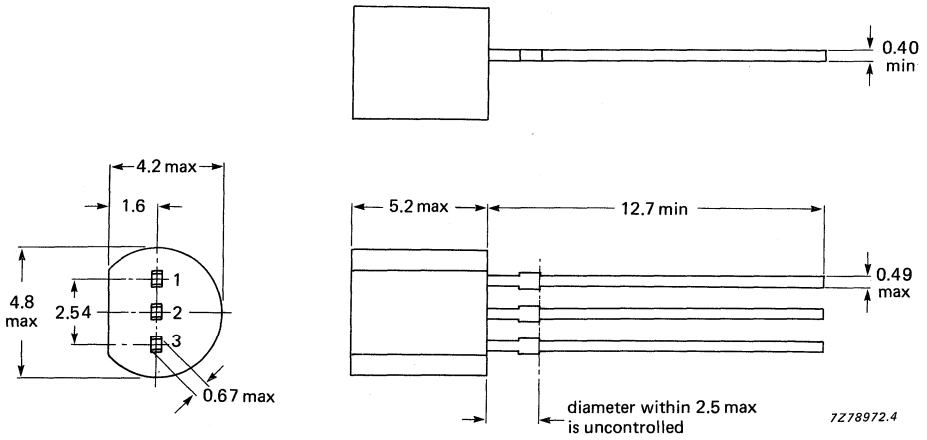
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 $-I_G$ = 1 μA	25	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 15 V V_{DS} = 0	-	2	nA
		$-V_{GS}$ = 15 V V_{DS} = 0 T_{amb} = 100 °C	-	2	μA
I_{DSS}	drain-source current	V_{GS} = 0 V_{DS} = 15 V	2	20	mA
$-V_{GS}$	gate-source voltage	I_D = 200 μA V_{DS} = 15 V	0.5	7.5	V
$-V_{(P)GS}$	gate-source cut-off voltage	I_D = 2 nA V_{DS} = 15 V	-	8	V
$\lvert y_{fs} \rvert$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2	6.5	mS
$\lvert y_{fs} \rvert$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz	1.6	-	mS
$\lvert y_{os} \rvert$	output admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	-	50	μS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	8	pF
C_{rss}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	4	pF

N-channel J-FET 2N3819

PACKAGE OUTLINE



Dimensions in mm

Fig.3 TO-92.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N3820
P-channel J-FET

DESCRIPTION

Silicon p-channel junction field-effect transistor in a plastic TO-92 envelope. It is intended for use in general purpose amplifiers.

PINNING - TO-92

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION

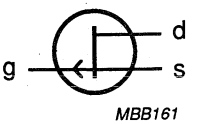


Fig.1 Symbol.

P-channel J-FET 2N3820

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	20	V
$+V_{GS}$	gate-source voltage		-	20	V
$-V_{DG}$	drain-gate voltage		-	20	V
$-I_G$	gate current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	360	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	347	K/W

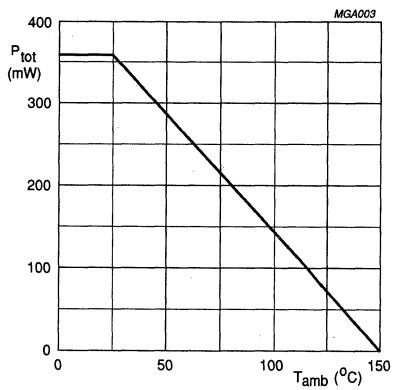


Fig.2 Total power dissipation as a function of ambient temperature.

P-channel J-FET 2N3820

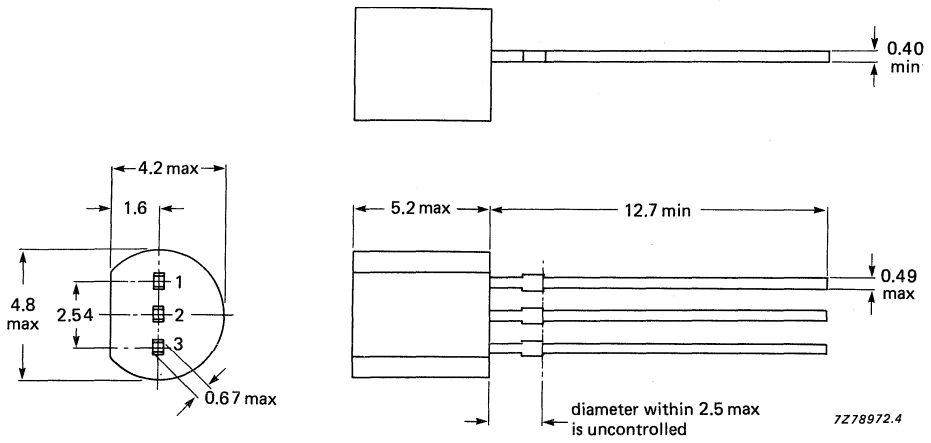
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 I_G = 10 μA	20	-	V
I_{GSS}	gate-source leakage current	V_{GS} = 10 V V_{DS} = 0	-	20	nA
		V_{GS} = 10 V V_{DS} = 0 T_{amb} = 100 °C	-	2	μA
$-I_{DSS}$	drain-source current	V_{GS} = 0 $-V_{DS}$ = 10 V	0.3	15	mA
V_{GS}	gate-source voltage	$-I_D$ = 30 μA $-V_{DS}$ = 10 V	0.3	7.9	V
$V_{(P)GS}$	gate-source cut-off voltage	$-I_D$ = 10 nA $-V_{DS}$ = 10 V	-	8	V
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 10 V V_{GS} = 0 f = 1 kHz	0.8	5	mS
		$-V_{DS}$ = 10 V V_{GS} = 0 f = 10 MHz	0.7	-	mS
$\|y_{os}\|$	output admittance	$-V_{DS}$ = 10 V V_{GS} = 0 f = 1 kHz	-	200	μS
C_{iss}	input capacitance	$-V_{DS}$ = 10 V V_{GS} = 0 f = 1 MHz	-	32	pF
$-C_{rss}$	feedback capacitance	$-V_{DS}$ = 10 V V_{GS} = 0 f = 1 MHz	-	16	pF

P-channel J-FET 2N3820

PACKAGE OUTLINE



Dimensions in mm

Fig.3 TO-92.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Drain current			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10 mA
Transfer admittance			
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$		3,0 to 6,5 mS
V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	$\|y_{fs}\|$	>	3,0 mS

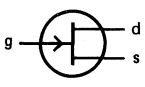
MECHANICAL DATA

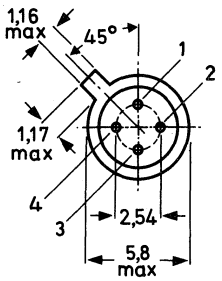
Dimensions in mm

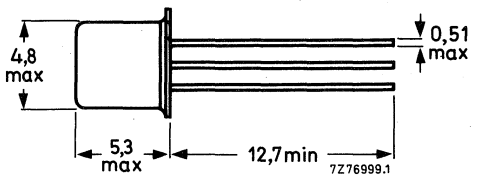
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50 V
Drain-gate voltage	V_{DG}	max.	50 V
Gate-source voltage	$-V_{GS}$	max.	50 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590 K/W

CHARACTERISTICS with source connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 30 V; V_{DS} = 0	$-I_{GSS}$	<	0,1 nA
$-V_{GS}$ = 30 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,1 μA
Drain current *			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10 mA
Gate-source breakdown voltage			
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	50 V
Gate-source voltage			
V_{DS} = 15 V; I_D = 200 μA	$-V_{GS}$		1 to 4 V
Gate-source cut-off voltage			
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	6 V
Small-signal common source characteristics			
V_{DS} = 15 V; V_{GS} = 0			
Transfer admittance *			
f = 1 kHz	$\lvert y_{fs} \rvert$		3,0 to 6,5 mS
f = 100 MHz	$\lvert y_{fs} \rvert$	>	3,0 mS
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	20 μS
Input capacitance at f = 1 MHz	C_{iss}	<	6 pF
Feedback capacitance at f = 1 MHz	C_{rss}	<	3 pF
Noise figure			
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 MΩ			
f = 10 Hz; B = 5 Hz	F	<	5 dB
Equivalent input noise voltage			
V_{DS} = 15 V; V_{GS} = 0			
f = 10 Hz; B = 5 Hz	V_n	<	200 $nV/\sqrt{Hz}$

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

QUICK REFERENCE DATA

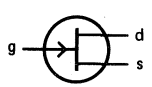
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20 mA
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rss}	<	2 pF
Transfer admittance V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\|y_{fs}\|$	>	3,2 mS
Noise figure at f = 100 MHz V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5 dB

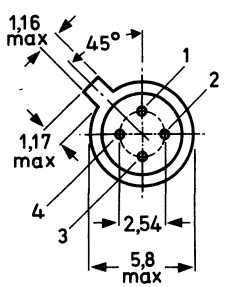
MECHANICAL DATA

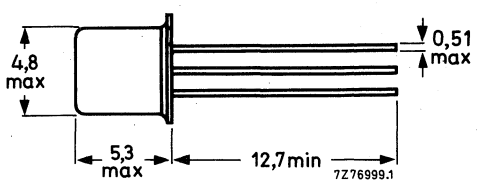
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage	V_{DG}	max.	30 V
Gate-source voltage	$-V_{GS}$	max.	30 V
Gate current (d.c.)	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590 K/W

CHARACTERISTICS with source and shield connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0,5 nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,5 μA
Drain current *			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20 mA
Gate-source breakdown voltage			
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30 V
Gate-source voltage			
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$		1,0 to 7,5 V
Gate-source cut-off voltage			
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	8 V
Small-signal common source characteristics			
V_{DS} = 15 V; V_{GS} = 0			
Transfer admittance *			
f = 1 kHz	$\lvert y_{fs} \rvert$		3,5 to 6,5 mS
f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2 mS
Output admittance at f = 1 kHz *	$\lvert y_{os} \rvert$	<	35 μS
Input capacitance at f = 1 MHz	C_{iss}	<	6 pF
Feedback capacitance at f = 1 MHz	C_{rss}	<	2 pF
Real part of input conductance at f = 200 MHz	$Re(y_{is})$	<	0,8 mS
Real part of output conductance at f = 200 MHz	$Re(y_{os})$	<	0,2 mS
Noise figure at f = 100 MHz			
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5 dB

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL SILICON FET

Symmetrical n-channel, depletion type, planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

QUICK REFERENCE DATA

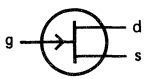
Drain-source voltage	$\pm V_{DS}$	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2 mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6 V
Feedback capacitance at f = 1 MHz V_{DS} = 0; V_{GS} = 7 V	C_{rs}	<	1,5 pF
Drain-source resistance (on) at f = 1 kHz V_{GS} = 0; I_D = 0	R_{DSon}	<	220 Ω

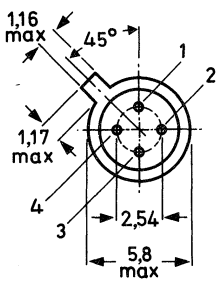
MECHANICAL DATA

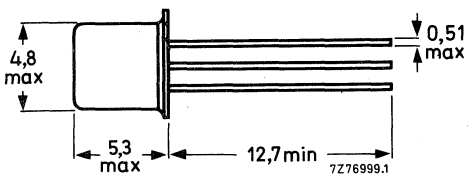
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = source
2 = drain
3 = gate
4 = shield lead connected to case







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250	mW
Storage temperature range	T_{stg}	−55 to +175		°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	590	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	nA
Drain current				
V_{DG} = 20 V; I_S = 0	I_{DGO}	<	0.1	nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<	0.2	μA
Drain current [1])				
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source breakdown voltage				
$-I_G$ = 1.0 μA; V_{DS} = 0	$-V_{(BR)GS}$	>	30	V
Gate-source voltage				
I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Drain-source voltage				
I_D = 1.0 mA; V_{GS} = 0	V_{DS}	<	0.25	V
Drain cut-off current				
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V	I_D	<	1.0	nA
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V; T_{amb} = 150 °C	I_D	<	2.0	μA
Drain-source resistance (on) at f = 1 kHz				
V_{GS} = 0; I_D = 0	R_{DSon}	<	220	Ω
Input capacitance at f = 1 MHz				
V_{DS} = 20 V; V_{GS} = 0	C_{iss}	<	6	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 0; V_{GS} = 7 V	C_{rss}	<	1.5	pF
Switching times				
V_{DD} = 1.5 V; $I_{D\,on}$ = 1.0 mA				
$V_{GS\,on}$ = 0; $-V_{GS\,off}$ = 6 V				
delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

CHARACTERISTICS (continued)

Switching times

V_{DD} = 1.5 V; $I_{D\,on}$ = 1.0 mA

$V_{GS\,on}$ = 0; $-V_{GS\,off}$ = 6 V

delay time	t_d	<	20	ns
rise time	t_r	<	100	ns
turn off time	t_{off}	<	100	ns

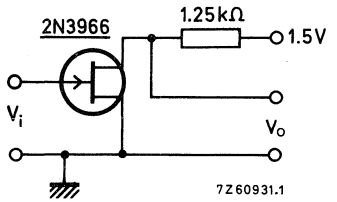


Fig. 2 Test circuit

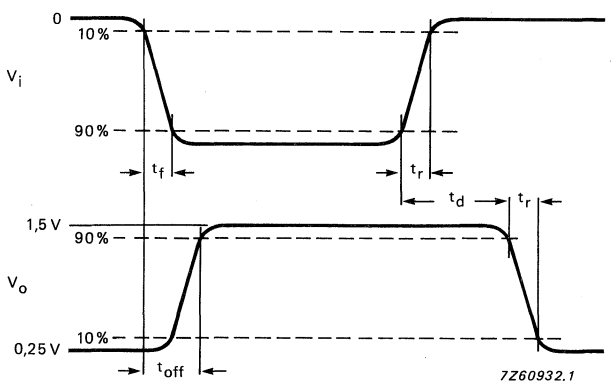


Fig. 3 Waveforms

Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 µs
δ < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max		1.5		W
			2N4091	**2N4092**	**2N4093**	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage		>	5,0	2,0	1,0	V
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	<	10	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω
Feedback capacitance at f = 1 MHz						
V_{DS} = 0; $-V_{GS}$ = 20 V	C_{rs}	<		5,0		pF
Turn-off time						
V_{DD} = 3,0 V; V_{GS} = 0						
I_D = 6,6 mA; $-V_{GSM}$ = 12 V **2N4091**	t_{off}	<		40		ns
I_D = 4,0 mA; $-V_{GSM}$ = 8 V **2N4092**	t_{off}	<		60		ns
I_D = 2,5 mA; $-V_{GSM}$ = 6 V **2N4093**	t_{off}	<		80		ns

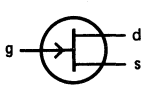
MECHANICAL DATA

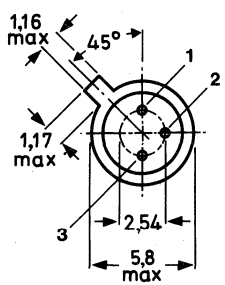
Dimensions in mm

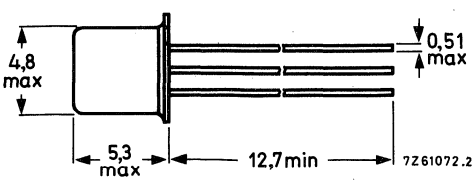
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Current				
Forward gate current (DC)	I_G	max.	10	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−55 to	+175	°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain currents

V_{DG} = 20 V; I_S = 0	I_{DGO}	<		0.2	nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<		0.4	µA

Source current

V_{SG} = 20 V; I_D = 0	I_{SGO}	<		0.2	nA

Drain cut-off current

			2N4091	2N4092	2N4093	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX}	<	0.4	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.4	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.4	µA

Gate-source breakdown voltage

$-I_G$ = 1.0 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V

Drain current [1])

V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA

Gate-source cut-off voltage

I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V

Drain-source voltages (on)

I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V

Drain- source resistance (on)

I_D = 1.0 mA; V_{GS} = 0	R_{DSon}	<	30	50	80	Ω

Drain-source resistance (on) at f = 1 kHz

I_D = 0; V_{GS} = 0	$R_{DS\ on}$	<	30	50	80	Ω

[1]) Measured under pulsed conditions: $t_p \leq 300$ µs; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

Input capacitance

V_{DS} = 20 V ; V_{GS} = 0	C_{is}	<	16	pF

Feedback capacitance

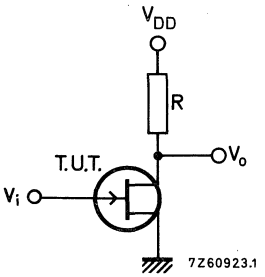
V_{DS} = 0 ; $-V_{GS}$ = 20 V	C_{rs}	<	5	pF

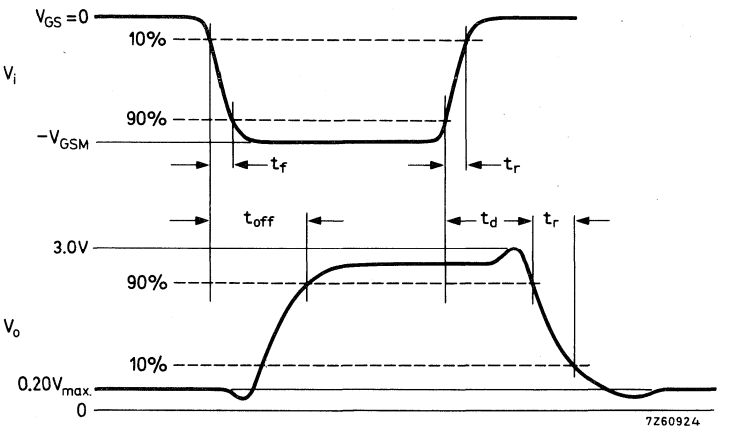
Switching times

V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:





$$R = \frac{2,8}{I_D}$$

Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N4220/4220A/4221/4221A/ 4222/4222A

N-channel J-FETs

FEATURES

- High gain in VHF range
- Low receiver noise figure.

DESCRIPTION

Symmetrical n-channel silicon junction field-effect transistor in a TO-72 envelope. It is intended for use as a VHF amplifier and in oscillators and mixers.

PINNING - TO-72

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	substrate

PIN CONFIGURATION

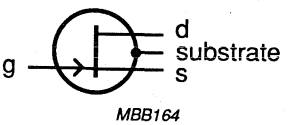


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	30	V
$-V_{GS}$	gate-source voltage		-	30	V
V_{DG}	drain-gate voltage		-	30	V
I_D	drain current		-	15	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		−65	175	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

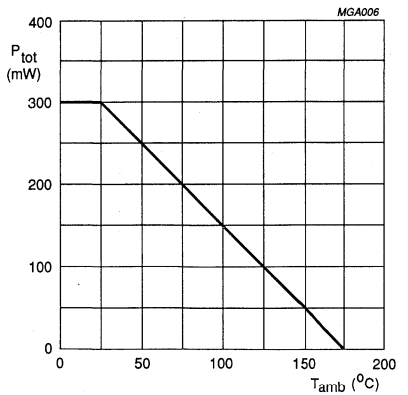


Fig.2 Total power dissipation as a function of ambient temperature.

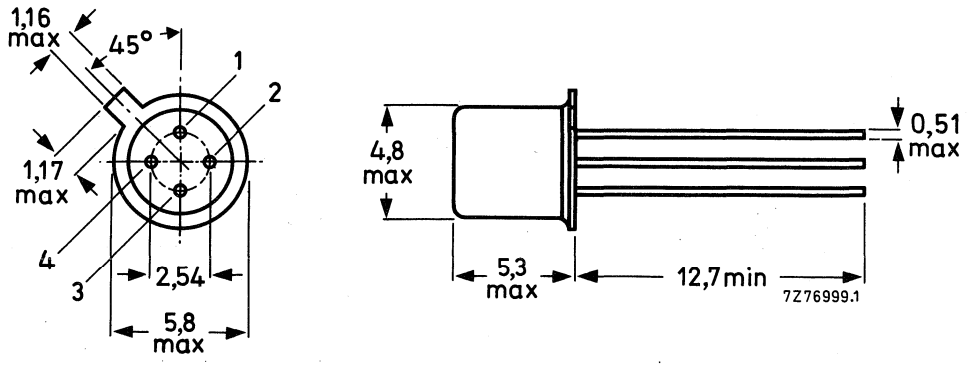
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 10 μA V_{DS} = 0		30	-	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 15 V V_{DS} = 0		-	-	0.1	nA
		$-V_{GS}$ = 15 V V_{DS} = 0 T_{amb} = 150 °C		-	-	100	nA
I_{DSS}	drain-source current	V_{DS} = 15 V V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	0.5 2 5	- - -	3 6 15	mA mA mA
$-V_{GS}$	gate-source voltage	V_{DS} = 15 V I_D = 50 μA	2N4220/A	0.5	-	2.5	V
		V_{DS} = 15 V I_D = 200 μA	2N4221/A	1	-	5	V
		V_{DS} = 15 V I_D = 500 μA	2N4222/A	2	-	6	V
$-V_{P(GS)}$	gate-source cut-off voltage	V_{DS} = 15 V I_D = 0.1 nA	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	4 6 8	V V V
$\|g_{fs}\|$	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	1 2 2.5	- - -	4 5 6	mS mS mS
$\|y_{fs}\|$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz		750	-	-	μS
$\|y_{os}\|$	output admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N4220/A 2N4221/A 2N4222/A	- - -	- - -	10 20 40	μS μS μS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	4.5	6	pF
$-C_{rss}$	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	1.2	2	pF
C_{oss}	output capacitance	V_{DS} = 15 V V_{GS} = 0 f = 30 MHz		-	1.5	-	pF
$R_{DS(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0	2N4220/A 2N4221/A 2N4222/A	- - -	500 400 300	- - -	Ω Ω Ω
F	noise figure	V_{DS} = 15 V V_{GS} = 0 R_S = 1 MΩ f = 100 Hz	2N4220A 2N4221A 2N4222A	-	-	2.5	dB

PACKAGE OUTLINE

Substrate connected to case.
Drain and source connections can be interchanged.



Dimensions in mm

Fig.3 TO-72.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N4340
N-channel J-FET

FEATURES

- Low noise, noise figure < 1 dB
- High off isolation.

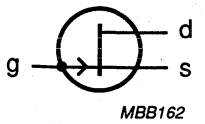
DESCRIPTION

Symmetrical n-channel silicon junction field-effect transistor in a TO-18 metal envelope. It is intended for use in small-signal audio amplifiers, as a switch in choppers, and as a voltage-controlled resistor.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	drain
3	gate, substrate

PIN CONFIGURATION



MBB162

Fig.1 Symbol.

N-channel J-FET 2N4340

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{GD}$	gate-drain voltage		-	50	V
$-V_{GS}$	gate-source voltage		-	50	V
I_G	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	300	mW
T_{stg}	storage temperature range		–65	200	°C
T_j	junction temperature		-	175	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

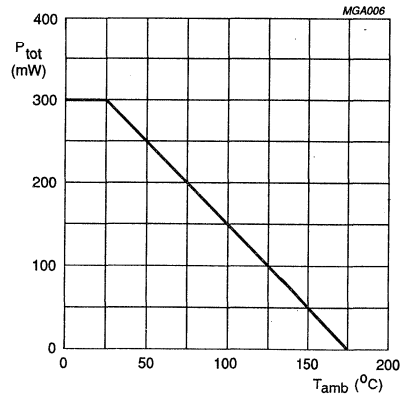


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel J-FET 2N4340

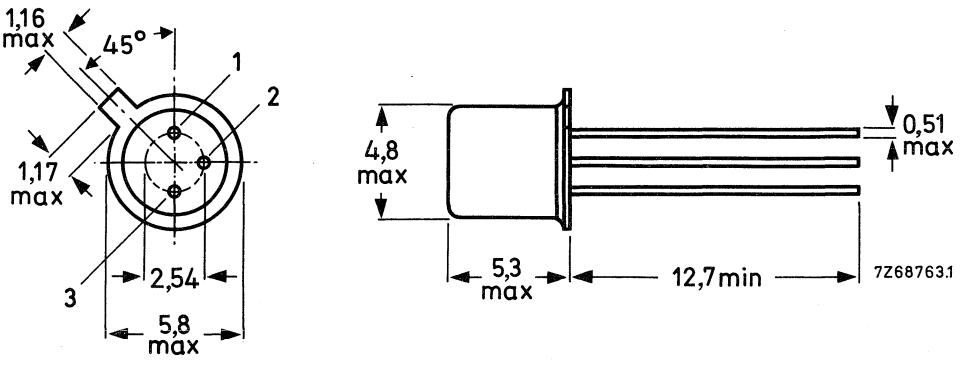
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 $-I_G$ = 1 µA	50	-	-	V
I_{DSS}	drain-source current	V_{GS} = 0 V_{DS} = 15 V	1.2	-	3.6	mA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 5 V V_{DS} = 15 V	-	-	0.05	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V	-	-	0.1	nA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 30 V T_{amb} = 150 °C	-	-	0.1	µA
$-V_{P(GS)}$	gate-source cut-off voltage	I_D = 0.1 µA V_{DS} = 15 V	1	-	3	V
$r_{ds(on)}$	drain-source on resistance	V_{DS} = 0 V_{GS} = 0 f = 1 kHz	-	-	1.5	kΩ
g_{fs}	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	1.3	-	3	mS
g_{os}	output conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	-	-	30	µS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	7	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	-	-	3	pF
F	noise figure	V_{GS} = 0 V_{DS} = 15 V R_G = 1 MΩ f = 1 kHz B = 200 Hz	-	-	1	dB

N-channel J-FET 2N4340

PACKAGE OUTLINE



Gate connected to case.

Dimensions in mm

Fig.3 TO-18.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1.5		W
			2N4391	**2N4392**	**2N4393**	
Drain current						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage		>	4,0	2,0	0,5	V
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz						
V_{DS} = 0; $-V_{GS}$ = 12 V **2N4391**						
V_{DS} = 0; $-V_{GS}$ = 7 V **2N4392**	C_{rs}	<	3,5	3,5	3,5	pF
V_{DS} = 0; $-V_{GS}$ = 5 V **2N4393**						
Turn-off time						
V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSoff}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSoff}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSoff}$ = 5 V	t_{off}	<	–	–	50	ns

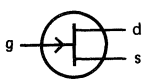
MECHANICAL DATA

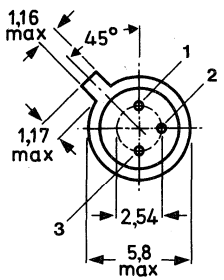
Dimensions in mm

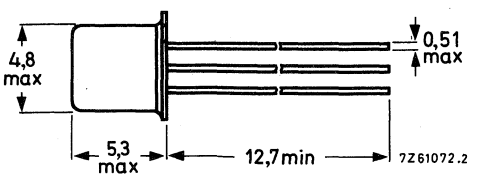
Fig. 1 TO-18.

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Note: Drain and source are interchangeable.

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Gate current (DC)	I_G	max.	50	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65	to +175	°C
Junction temperature	T_j	max.	175	°C
From junction to case in free air	$R_{th\ j\text{-}c}$	=	100	K/W

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off current

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$ <	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$ <	0.2	µA

Drain cut-off current

		2N4391	2N4392	2N4393	
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX} <	0.1	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 7 V	I_{DSX} <	–	0.1	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 5 V	I_{DSX} <	–	–	0.1	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX} <	0.2	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 7 V; T_{amb} = 150 °C	I_{DSX} <	–	0.2	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 5 V; T_{amb} = 150 °C	I_{DSX} <	–	–	0.2	µA

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain currents (note 1)						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	R_{DSon}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

Note

1. measured under pulsed conditions: t_p = 100 μs; δ = 0.01

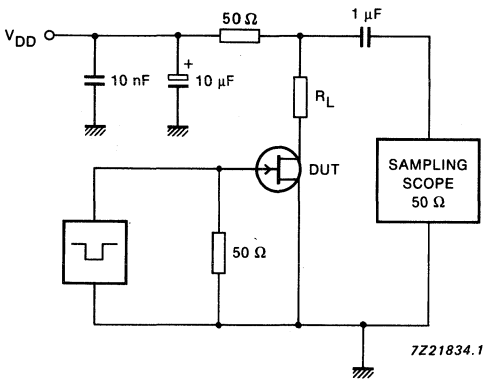
CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

Switching times

V_{DD} = 10 V; V_{GS} = 0

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSoff}$	=	12	7	5	V
	R_L	=	750	1550	3150	Ω
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:

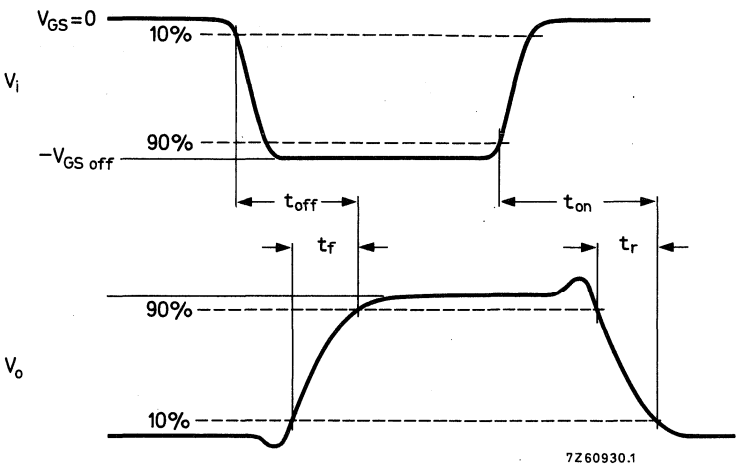


Pulse generator:

t_r	< 0.5	ns
t_f	< 0.5	ns
t_p	= 100	µs
δ	= 0.01	

Oscilloscope:

R_i = 50 Ω



Data sheet	
status	Product specification
date of issue	October 1990

2N4416/2N4416A
N-channel J-FETs

PINNING - TO-72

PIN	DESCRIPTION
1	source
2	drain
3	gate
4	substrate

PIN CONFIGURATION

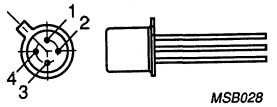


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
V_{DG}	drain-gate voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
$-V_{GS}$	gate-source voltage				
	2N4416		–	30	V
	2N4416A		–	35	V
I_G	gate current		–	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	300	mW
		$T_{case} \leq 25$ °C	–	450	mW
T_{stg}	storage temperature range		−65	200	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	590	K/W
$R_{th\ j\text{-}c}$	from junction to case	390	K/W

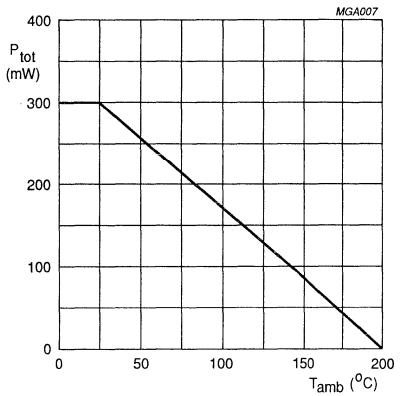


Fig.2 Power derating curve.

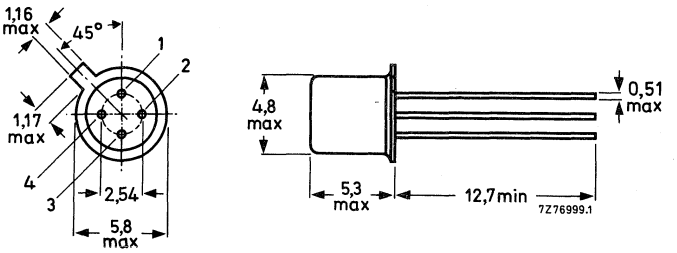
N-channel J-FETs 2N4416/2N4416A

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DSS}	drain-source current	V_{DS} = 15 V V_{GS} = 0	5	15	mA
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0	–	0.1	nA
		$-V_{GS}$ = 20 V V_{DS} = 0 T_{amb} = 150 °C	–	0.1	µA
$-V_{GS}$	gate-source voltage	I_D = 0.5 mA V_{DS} = 15 V	1	5.5	V
$-V_{P(GS)}$	gate-source cut-off voltage 2N4416 2N4416A	I_D = 1 nA V_{DS} = 15 V	 – 2.5	 6 6	 V V
$\|y_{fs}\|$	transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	4.5	7.5	mS
$\|y_{os}\|$	output admittance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	–	50	µS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	–	4	pF
C_{oss}	output capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	–	0.8	pF
C_{rss}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz	–	2	pF

PACKAGE OUTLINE



Dimensions in mm

Substrate connected to case.

Fig.3 TO-72.

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

Drain-source voltage	**2N4856 to 2N4858**	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
				2N4856 2N4859	**2N4857 2N4860**	**2N4858 2N4861**	
Drain current							
V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage			>	4	2	0,8	V
I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz							
I_D = 0; V_{GS} = 0		$R_{DS\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz							
V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time							
V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

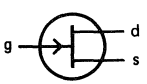
MECHANICAL DATA

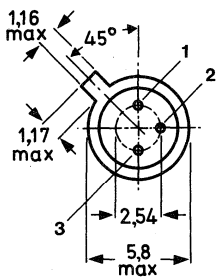
Dimensions in mm

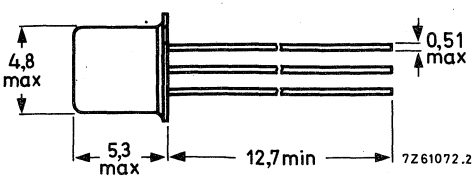
Fig. 1 TO-18

Gate connected to case

Pinning
1 = source
2 = drain
3 = gate







Accessories: 56246 (distance disc).

Note: Drain and source are interchangeable.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Gate current (d.c.)	I_G	max.	50		mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	300		mW
Storage temperature range	T_{stg}	−65 to	+175		^oC
Junction temperature	T_j	max.	175		^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	490	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off currents					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	µA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	µA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	µA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1])						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage					
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$R_{DS\,on}$	<	25	40	60	Ω

[1]) measured under pulsed conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)
V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz

Input capacitance	C_{is}	< 18 pF
Feedback capacitance	C_{rs}	< 8 pF

Switching times (see Figs 2 and 3)
V_{DD} = 10 V; V_{GS} = 0

		2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	= 20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	= 10	6	4	V
Delay time	t_d	< 6	6	10	ns
Rise time	t_r	< 3	4	10	ns
Turn-off time	t_{off}	< 25	50	100	ns

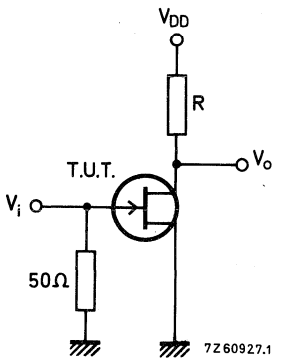


Fig. 2 Switching times test circuit.

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
R =	464	953	1910	Ω

Pulse generator:
$t_r \leqslant$ 1 ns
$t_f \leqslant$ 1 ns
δ = 0,02
Z_o = 50 Ω

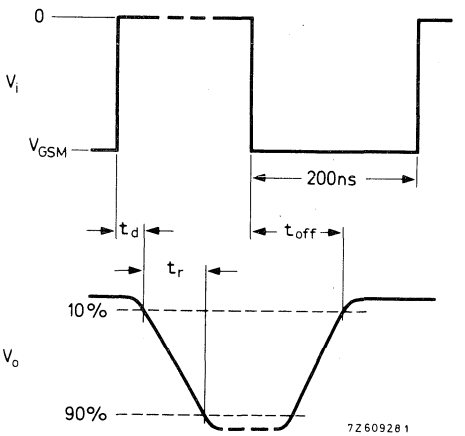


Fig. 3 Input and output waveforms.

Oscilloscope:
$t_r \leqslant$ 0,75 ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N5116
P-channel J-FET

FEATURES

- P-channel complement of 2N4393
- Short sample and hold aperture time.

DESCRIPTION

P-channel silicon junction field-effect transistor in a TO-18 metal envelope. It is intended for applications as an analog switch, on commutators and choppers, and as an integrator reset switch.

PINNING - TO-18

PIN	DESCRIPTION
1	source
2	gate
3	drain

PIN CONFIGURATION

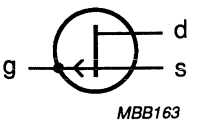


Fig.1 Symbol.

P-channel J-FET 2N5116

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{GD}	gate-drain voltage		-	30	V
V_{GS}	gate-source voltage		-	30	V
$-I_G$	gate current		-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	500	mW
T_{stg}	storage temperature range		–65	200	°C
T_j	junction temperature		-	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

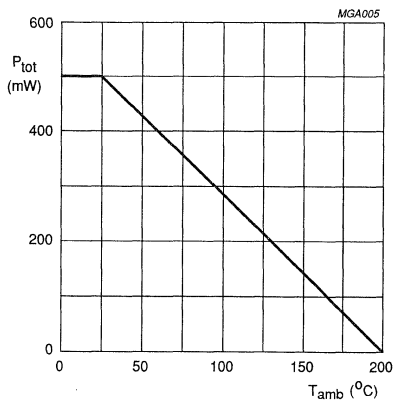


Fig.2 Total power dissipation as a function of ambient temperature.

P-channel J-FET 2N5116

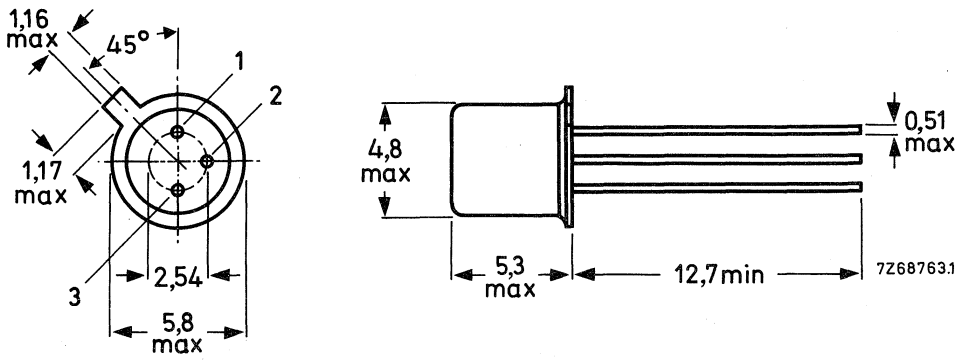
CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0 I_G = 1 µA	30	-	V
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0	-	0.5	nA
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0 T_{amb} = 150 °C	-	1	µA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V	-	0.5	nA
$-I_{DSX}$	drain cut-off current	V_{GS} = 5 V $-V_{DS}$ = 15 V T_{amb} = 150 °C	-	1	µA
$-I_{DSS}$	drain current	V_{GS} = 0 $-V_{DS}$ = 15 V	5	25	mA
$-V_{GS}$	gate-source voltage	$-I_G$ = 1 mA V_{DS} = 0	-	1	V
$V_{P(GS)}$	gate-source cut-off voltage	$-V_{DS}$ = 15 V $-I_D$ = 1 nA	1	4	V
$-V_{(DS)on}$	drain-source on voltage	V_{GS} = 0 $-I_D$ = 3 mA	-	0.6	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 0 $-I_D$ = 1 mA	-	150	Ω
$r_{ds(on)}$	drain-source on resistance	V_{GS} = 0 I_D = 0 f = 1 kHz	-	150	Ω
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz	-	27	pF
C_{rss}	feedback capacitance	V_{DS} = 0 V_{GS} = 5 V f = 1 MHz	-	7	pF
Switching times					
t_d	delay time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	12	ns
t_r	rise time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	30	ns
t_{off}	turn-off time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	10	ns
t_f	fall time	$-V_{batD}$ = 6 V V_{batG} = 8 V R_L = 2 kΩ R_G = 390 Ω $-I_D$ = 3 mA	-	50	ns

P-channel J-FET 2N5116

PACKAGE OUTLINE



Dimensions in mm

Fig.3 TO-18.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N5460/5461/5462
P-channel J-FETs

DESCRIPTION

P-channel silicon junction field-effect transistor in a TO-92 plastic envelope. It is intended for use as an analog switch and an amplifier.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	drain
3	source

PIN CONFIGURATION

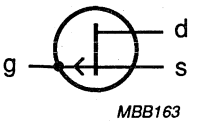


Fig.1 Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	40	V
V_{GS}	gate-source voltage		-	40	V
$-I_G$	gate current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 40$ °C	-	310	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	355	K/W

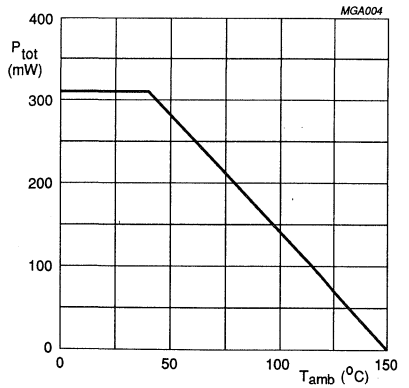


Fig.2 Total power dissipation as a function of ambient temperature.

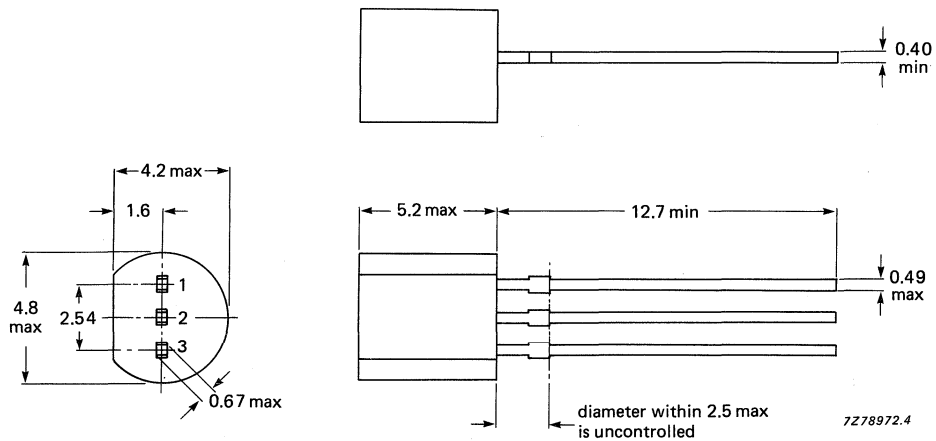
P-channel J-FETs | 2N5460/5461/5462

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{GSS}	gate-source leakage current	V_{GS} = 20 V V_{DS} = 0		-	5	nA
		V_{GS} = 20 V V_{DS} = 0 T_{amb} = 100 °C		-	1	µA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 15 V V_{GS} = 0	2N5460 2N5461 2N5462	1 2 4	5 9 16	mA mA mA
V_{GS}	gate-source voltage	$-I_D$ = 0.1 mA $-V_{DS}$ = 15 V	2N5460	0.5	4	V
V_{GS}	gate-source voltage	$-I_D$ = 0.2 mA $-V_{DS}$ = 15 V	2N5461	0.8	4.5	V
V_{GS}	gate-source voltage	$-I_D$ = 0.4 mA $-V_{DS}$ = 15 V	2N5462	1.5	6	V
$V_{P(GS)}$	gate-source cut-off voltage	$-I_D$ = 1 µA $-V_{DS}$ = 15 V	2N5460 2N5461 2N5462	0.75 1 1.8	6 7.5 9	V V V
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz	2N5460 2N5461 2N5462	1 1.5 2	4 5 6	mS mS mS
$\|y_{os}\|$	output admittance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 kHz		-	75	µS
C_{iss}	input capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	7	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 15 V V_{GS} = 0 f = 1 MHz		-	2	pF
NF	noise figure	$-V_{DS}$ = 15 V V_{GS} = 0 f = 100 Hz B = 1 Hz		-	2.5	dB

PACKAGE OUTLINE



Dimensions in mm

Fig.3 TO-92.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

2N5484/5485/5486
N-channel J-FETs

FEATURES

- No gate-drive current required
- Very low parasitic capacitances
- High gain
- Specified for 100/400 MHz operation

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION

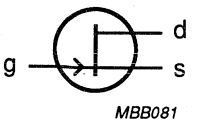


Fig.1 Symbol.

DESCRIPTION

N-channel silicon junction field-effect transistor in a plastic TO-92 envelope. It is intended for use as a VHF/UHF amplifier equipment such as mixers and oscillators.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DG}	drain-gate voltage		-	25	V
$-V_{GS}$	gate-source voltage		-	25	V
$I_{G(F)}$	forward gate current		-	10	mA
P_{tot}	total power dissipation	T_{case} = 25 °C	-	310	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		-	150	°C

N-channel J-FETs 2N5484/5485/5486

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

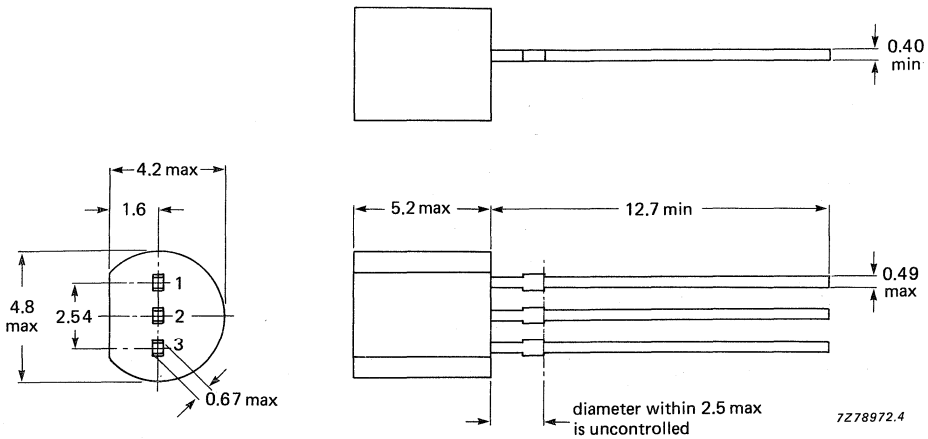
SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 µA V_{DS} = 0		25	-	V
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0 $-V_{GS}$ = 20 V V_{DS} = 0 T_{amb} = 100 °C		- -	1 0.2	nA µA
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 10 nA V_{DS} = 15 V	2N5484 2N5485 2N5486	0.3 0.5 2	3 4 6	V V V
I_{DSS}	drain-source current	V_{DS} = 15 V V_{GS} = 0	2N5484 2N5485 2N5486	1 4 8	5 10 20	mA mA mA
g_{fs}	transfer conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N5484 2N5485 2N5486	3 3.5 4	6 7 8	mS mS mS
$Re(y_{is})$	common source input admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz	2N5484	-	0.1	mS
$\|y_{is}\|$	input admittance	V_{DS} = 15 V V_{GS} = 0 f = 400 MHz	2N5485 2N5486	- -	1 1	mS mS
g_{os}	output conductance	V_{DS} = 15 V V_{GS} = 0 f = 1 kHz	2N5484 2N5485 2N5486	- - -	50 60 75	µS µS µS
$Re(g_{os})$	common source output conductance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz	2N5484	-	0.075	mS
$Re(y_{os})$	common source output admittance	V_{DS} = 15 V V_{GS} = 0 f = 400 MHz	2N5485 2N5486	- -	0.1 0.1	mS mS
$Re(y_{fs})$	common source transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 100 MHz	2N5484	2.5	-	mS
$Re(y_{fs})$	common source transfer admittance	V_{DS} = 15 V V_{GS} = 0 f = 400 MHz	2N5485 2N5486	3 3.5	- -	mS mS
C_{iss}	input capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	5	pF
C_{rss}	feedback capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	1	pF
C_{oss}	output capacitance	V_{DS} = 15 V V_{GS} = 0 f = 1 MHz		-	2	pF
NF	noise figure	V_{DS} = 15 V V_{GS} = 0 R_G = 1 MΩ f = 1 kHz		-	2.5	dB

CHARACTERISTICS (continued)

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
NF	noise figure	V_{DS} = 15 V I_D = 1 mA R_G = 1 kΩ f = 100 MHz	2N5484	-	3	dB
NF	noise figure	V_{DS} = 15 V I_D = 4 mA R_G = 1 kΩ f = 100 MHz	2N5485 2N5486	- -	2 2	dB dB
F	noise figure	V_{DS} = 15 V I_D = 4 mA R_G = 1 kΩ f = 400 MHz	2N5485 2N5486	- -	4 4	dB dB
G_{ps}	common source power gain	V_{DS} = 15 V I_D = 1 mA f = 100 MHz	2N5484	16	25	dB
G_{ps}	common source power gain	V_{DS} = 15 V I_D = 4 mA f = 100 MHz	2N5485 2N5486	18 18	30 30	dB dB
G_{ps}	common source power gain	V_{DS} = 15 V I_D = 4 mA f = 400 MHz	2N5485 2N5486	10 10	20 20	dB dB

PACKAGE OUTLINE



Dimensions in mm

Fig.2 TO-92.

DEVICE DATA
MOS-FETs
single gate

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		10 to 40 mA
Transfer admittance I_D = 5 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	6 mS
Feedback capacitance I_D = 5 mA; V_{DS} = 15 V; f = 1 MHz	C_{rs}	<	0,7 pF
Noise figure at f = 200 MHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C G_S = 1 mS; $B_S = B_{Sopt}$	F	<	5 dB
Equivalent noise voltage at f = 1 kHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C	$V_n\sqrt{B}$	typ.	100 $nV\sqrt{Hz}$

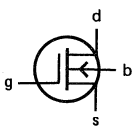
MECHANICAL DATA

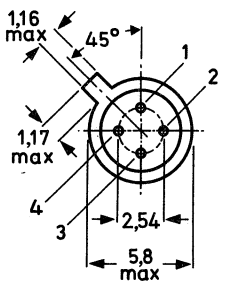
Dimensions in mm

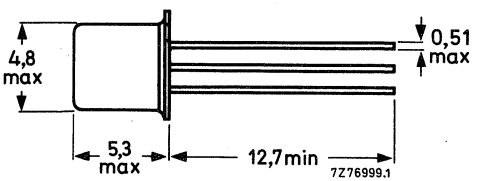
Fig. 1 TO-72.

Pinning

1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

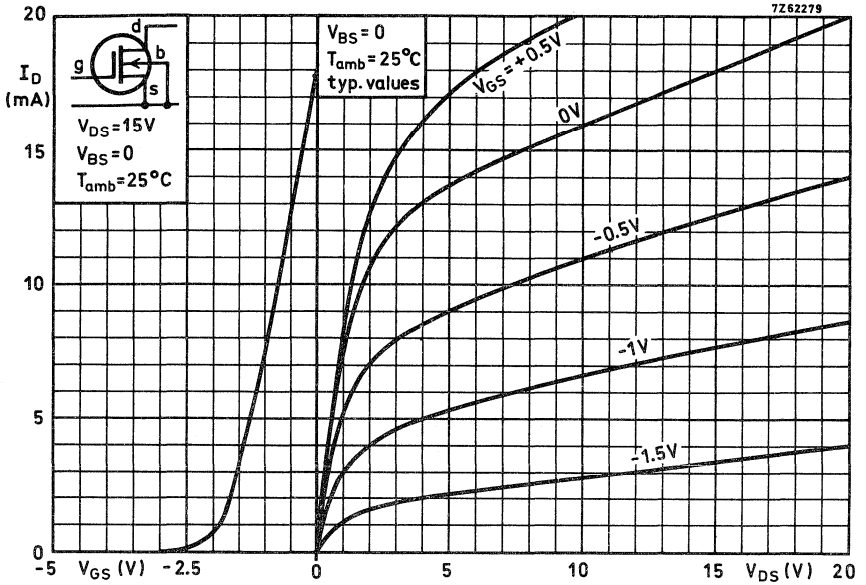
Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 V −15 V
Drain current (d.c.)	I_D	max.	20 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature	T_{stg}	−65 to +	125 °C
Junction temperature	T_j	max.	125 °C

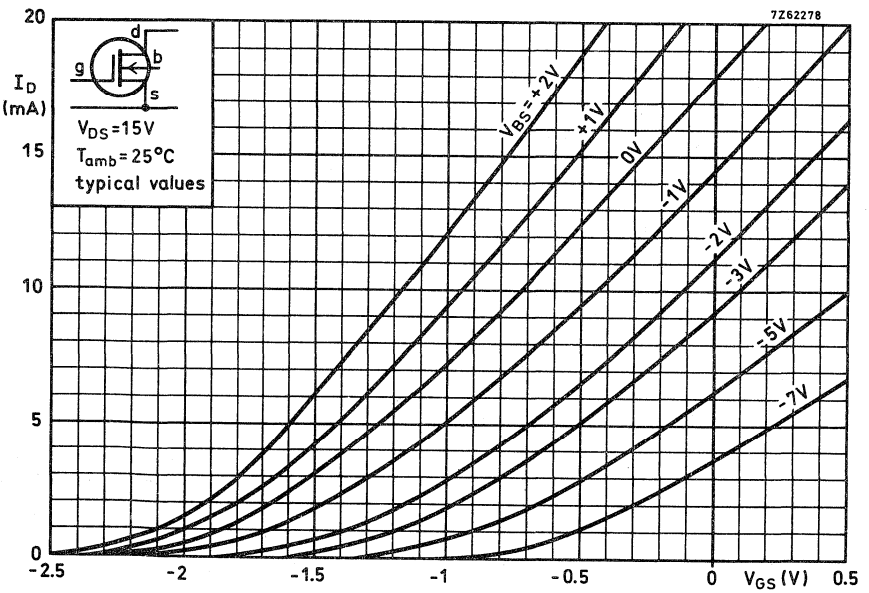
THERMAL RESISTANCE

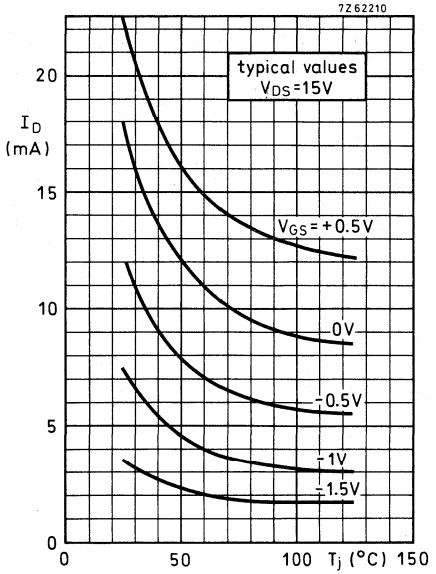
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

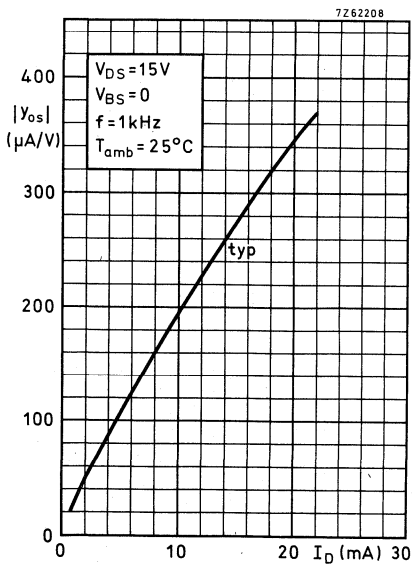
CHARACTERISTICS $T_j = 25\ ^oC$ unless otherwise specified

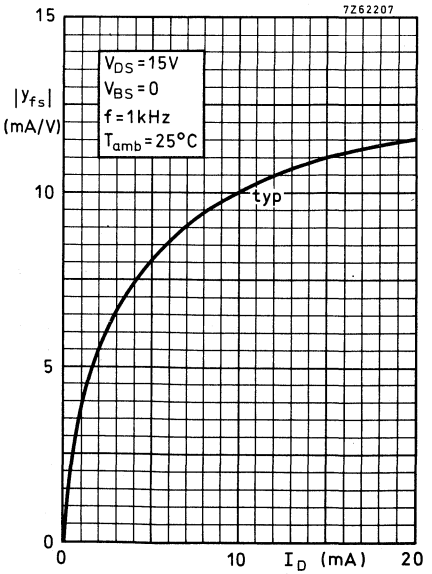
Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	I_{GSS}	<	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	μA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	μA
Drain current				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	10 to	40	mA
Gate-source voltage				
$I_D = 100$ nA; $V_{DS} = 15$ V	$-V_{GS}$	0.5 to	3.5	V
Gate-source cut-off voltage				
$I_D = 100$ nA ; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	4	V
y parameters				
$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\ ^oC$				
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	6	mS
Output admittance at f = 1 kHz	$\|y_{os}\|$	<	0.4	mS
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF
Noise figure at f = 200 MHz				
$I_D = 5$ mA; $V_{DS} = 15$ V; $T_{amb} = 25\ ^oC$				
$G_S = 1$ mS; $B_S = B_{Sopt}$	F	<	5	dB
Equivalent noise voltage $T_{amb} = 25\ ^oC$				
$I_D = 5$ mA; $V_{DS} = 15$ V; f = 120 Hz	$V_n/\sqrt{B}$	typ.	300	nV/$\sqrt{Hz}$
$T_{amb} = 25\ ^oC$ f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	nV/$\sqrt{Hz}$
f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	nV/$\sqrt{Hz}$

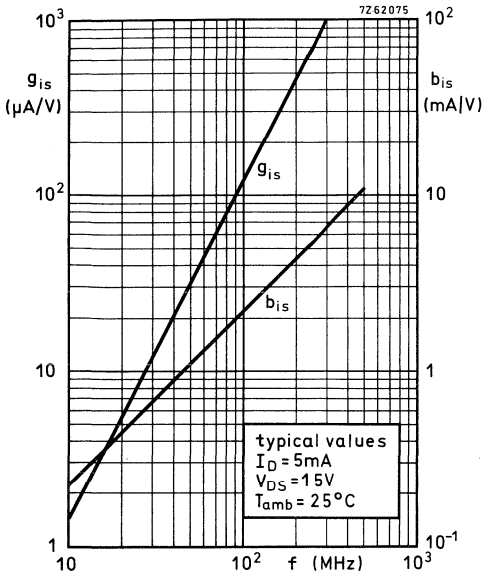

7Z62279
I_D (mA)
20
15
10
5
0
d
g
b
s
V_{DS}=15V
V_{BS}=0
T_{amb}=25°C
V_{BS} = 0
T_{amb} = 25°C
typ. values
V_{GS} = +0.5V
0V
-0.5V
-1V
-1.5V
-5
V_{GS} (V)
-2.5
0
5
10
15
V_{DS} (V)
20

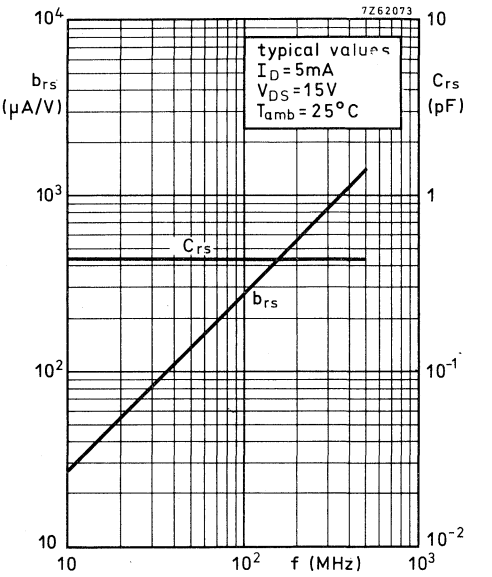

7Z62278
I_D (mA)
20
15
10
5
0
d
g
b
s
V_{DS}=15V
T_{amb}=25°C
typical values
V_{BS} = +2V
+1V
0V
-1V
-2V
-3V
-5V
-7V
-2.5
-2
-1.5
-1
-0.5
0
V_{GS} (V)
0.5

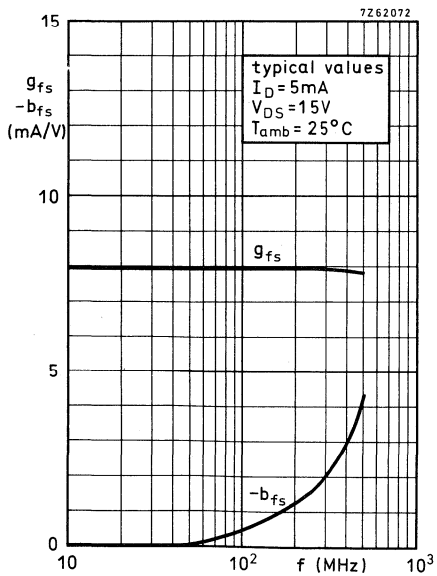

7Z62210
typical values
V_{DS}=15V
I_D
(mA)
20
15
10
5
0
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
0
50
100
T_j (°C)
150

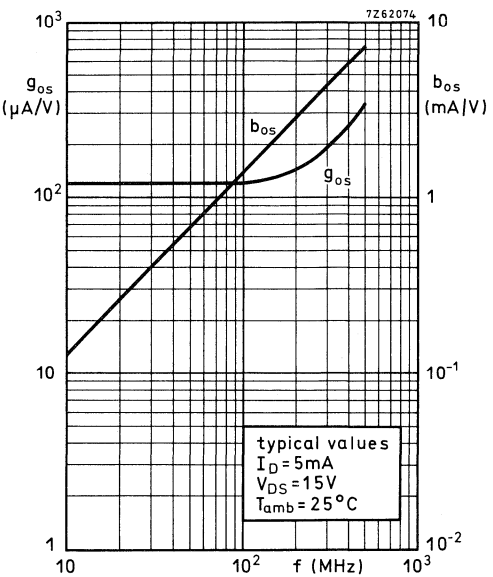

7Z62208
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{os}|$
(μA/V)
400
300
200
100
0
typ
0
10
20
I_D(mA)
30

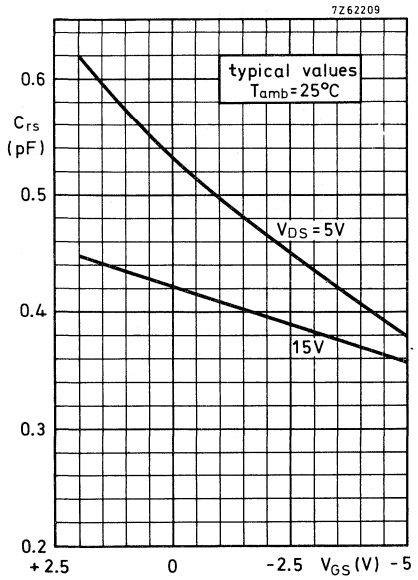

7Z62207
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{fs}|$
(mA/V)
15
10
5
0
typ
0
10
I_D (mA)
20

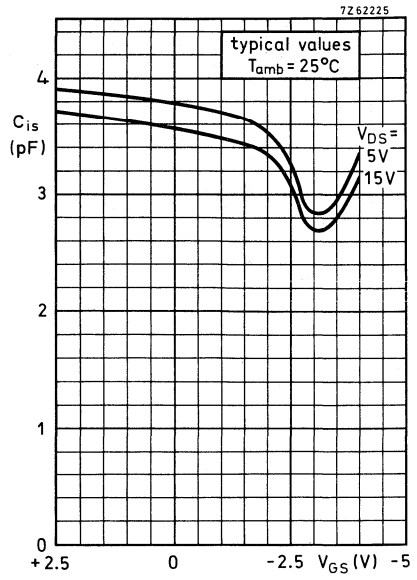

7Z62075
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62073
b_{rs} (μA/V)
C_{rs} (pF)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
C_{rs}
b_{rs}
f (MHz)


7Z62072
g_{fs} $-b_{fs}$ (mA/V)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
f (MHz)


7Z62074
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62209
typical values
Tamb = 25°C
Crs
(pF)
0.6
0.5
0.4
0.3
0.2
VDS = 5V
15V
+2.5
0
-2.5
VGS (V)
-5


7Z62225
typical values
Tamb = 25°C
Cis
(pF)
4
3
2
1
0
VDS =
5V
15V
+2.5
0
-2.5
VGS (V)
-5

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.

The transistor is sealed in a TO-72 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.	275	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feedback capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

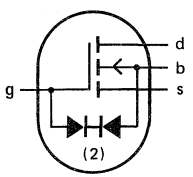
MECHANICAL DATA

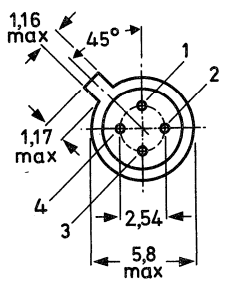
Dimensions in mm

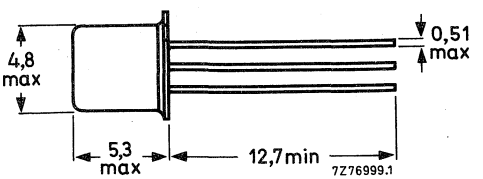
Fig. 1 TO-72.

Pinning

1 = source
2 = drain
3 = gate
4 = substrate (b) connected to case







Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	+ 15 −15	V V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C in free air	P_{tot}	max.	275	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA
Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_S = 20 mA	g_{fs}	min. typ.	10 15	mS mS

Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0 V_{GS} = 5 V	r_{DSon}	typ. max.	25 Ω 50 Ω
V_{GS} = 10 V	r_{DSon}	typ. max.	15 Ω 30 Ω
Capacitances at f = 1 MHz (see Fig. 2) V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	2.3 pF
Output capacitance	C_{oss}	typ.	1.9 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 to + 5 V	t_{on}	typ.	1.0 ns
	t_{off}	typ.	5.0 ns

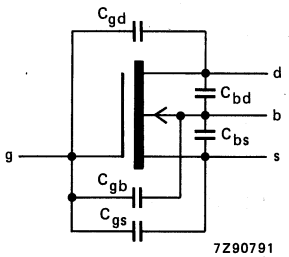
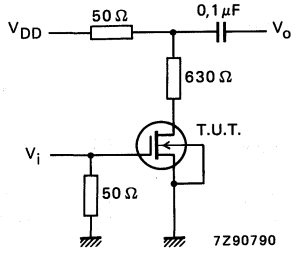


Fig. 2 Capacitances model.
$C_{iss} = C_{gs} + C_{gd} + C_{gb}$
$C_{oss} = C_{gd} + C_{bd}$
$C_{rss} = C_{gd}$



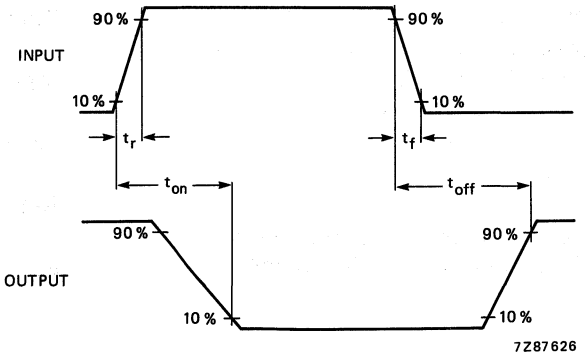


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; $t_r < 0.5$ ns; $t_f < 1.0$ ns; t_p = 20 ns; $\delta < 0.01$.

MOSFET N-CHANNEL DEPLETION SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type.

The transistor is sealed in a SOT-143 envelope and features a low ON-resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver
- convertor
- chopper

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230	mW
Junction temperature	T_j	max.	125	°C
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 1 mA	R_{DSon}	max.	30	Ω
Feed-back capacitance V_{GS} = V_{BS} = −5 V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6	pF

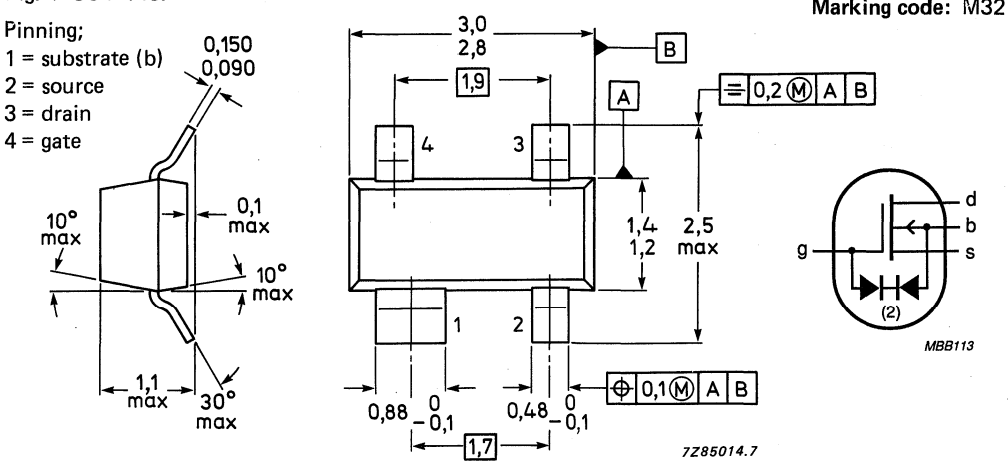
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-143.

Marking code: M32

Pinning;
1 = substrate (b)
2 = source
3 = drain
4 = gate



TOP VIEW

Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Source-drain voltage	V_{SD}	max.	20	V
Drain-substrate voltage	V_{DB}	max.	25	V
Source-substrate voltage	V_{SB}	max.	25	V
Gate-substrate voltage	V_{GB}	max.	± 25	V
Gate-source voltage	V_{GS}	max.	+ 15 −40	V V
Drain current (DC)	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current $V_{GS} = V_{BS} = -5$ V; V_{DS} = 10V	I_{DSoff}	typ.	1.0	nA
Source-drain leakage current $V_{GD} = V_{BD}$ = 5 V; V_{SD} = 10V	I_{SDoff}	typ.	1.0	nA
Gate-substrate leakage current $V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	max.	10	nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

Forward transconductance at f = 1 kHz V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	min. typ.	10 mS 15 mS
Gate-source cut-off voltage V_{DS} = 10 V; V_{SB} = 0; I I_D = 10 μA	$-V_{(P)GS}$	max.	2.0 V
Drain-source ON-resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 5 V	R_{DSon}	typ. max.	25 Ω 50 Ω
V_{GS} = 10 V	R_{DSon}	typ. max.	15 Ω 30 Ω
Capacitances at f = 1 MHz V_{GS} = V_{BS} = −5V; V_{DS} = 10 V			
Feed-back capacitance	C_{rss}	typ.	0.6 pF
Input capacitance	C_{iss}	typ.	1.5 pF
Output capacitance	C_{oss}	typ.	1.0 pF
Switching times (see Fig. 3) V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on} t_{off}	typ. typ.	1.0 ns 5.0 ns

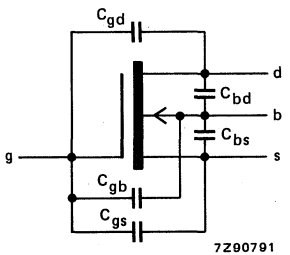
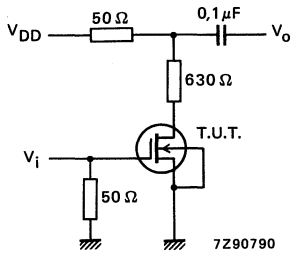


Fig. 2 Capacitances model.

$C_{iss} = C_{gs} + C_{gd} + C_{gb}$

$C_{oss} = C_{gd} + C_{bd}$

$C_{rss} = C_{gd}$



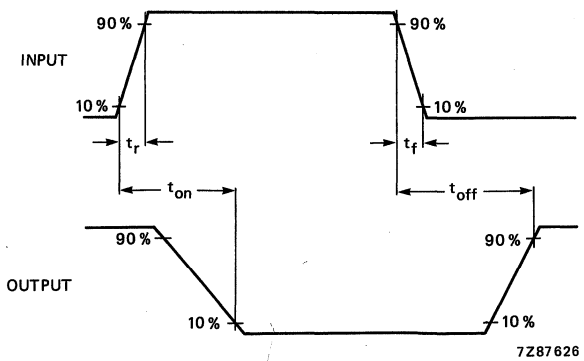


Fig. 3 Switching times and input and output waveforms;
R_i = 50 Ω; $t_r < 0.5$ ns; $t_f < 1.0$ ns; t_p = 20 ns; $\delta < 0.01$.

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTORS

Symmetrical insulated gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

These transistors are hermetically sealed in a TO-72 envelope and feature a low ON-resistance, high switching speed and low capacitances.

The types BSD213 and BSD215 are protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analogue and/or digital switch
- switch driver
- converters
- choppers

QUICK REFERENCE DATA

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Drain-source resistance I_D = 1 mA; V_{SB} = 0; V_{GS} = 15 V	$R_{DS(on)}$	typ.		25			Ω
Feedback capacitance $V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.		0,6			pF
Junction temperature	T_j	max.		125			°C

MECHANICAL DATA

See next page.

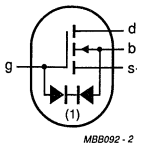
MECHANICAL DATA

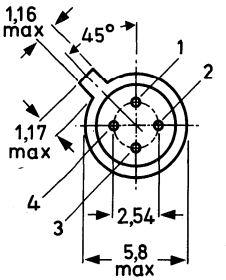
Dimensions in mm

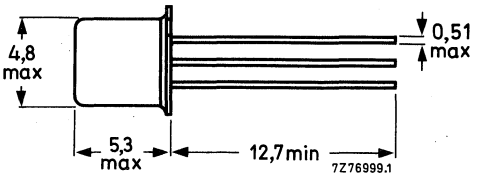
Fig. 1 TO-72.

Pinning

1 = drain
2 = source
3 = gate
4 = substrate (b)
connected to case







(1) Diode protection on types BSD213 and BSD215 only.
BSD212 and BSD214 have no protection diode.
To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BSD212	BSD213	BSD214	BSD215	
Drain-source voltage	V_{DS}	max.	10	10	20	20	V
Source-drain voltage	V_{SD}	max.	10	10	20	20	V
Drain-substrate voltage	V_{DB}	max.	15	15	25	25	V
Source-substrate voltage	V_{SB}	max.	15	15	25	25	V
Gate-substrate voltage	V_{GB}	max.	± 40	± 15	± 40	± 15	V
Gate-source voltage	V_{GS}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Gate-drain voltage	V_{GD}	max.	± 40	+ 15 −30	± 40	+ 15 −40	V
Drain current (DC)	I_D	max.		50			mA
Total power dissipation up to T_{amb} = 25 °C (free air)	P_{tot}	max.		275			mW
Storage temperature range	T_{stg}			−65 to + 175			°C
Junction temperature	T_j	max.		125			°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	360	K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			BSD212	BSD213	BSD214	BSD215	
Drain-source breakdown voltage							
$V_{GS} = V_{BS} = -5$ V; I_S = 10 nA	$V_{(BR)DSX}$	>	10	10	20	20	V
Source-drain breakdown voltage							
$V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10	10	20	20	V
Drain-substrate breakdown voltage							
V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15	15	25	25	V
Source-substrate breakdown voltage							
V_{GB} = 0; I_S = 10 nA; open drain	$V_{(BR)SBO}$	>	15	15	25	25	V
Drain-source leakage current							
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 10 V	I_{DSoff}	typ.	1,0	1,0	–	–	nA
$V_{GS} = V_{BS} = -5$ V; V_{DS} = 20 V	I_{DSoff}	typ.	–	–	1,0	1,0	nA
Source-drain leakage current							
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 10 V	I_{SDoff}	typ.	1,0	1,0	–	–	nA
$V_{GD} = V_{BD} = -5$ V; V_{SD} = 20 V	I_{SDoff}	typ.	–	–	1,0	1,0	nA
Gate-substrate leakage current							
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 40 V	I_{GBS}	<	0,1	–	0,1	–	nA
$V_{DB} = V_{SB}$ = 0; V_{GB} = ± 15 V	I_{GBS}	<	–	10	–	10	nA
Threshold voltage							
$V_{DS} = V_{GS} = V_{GS(th)}$; V_{SB} = 0; I_S = 1 μA	$V_{GS(th)}$		0,1 to 2,0				V

			BSD212	BSD213	BSD214	BSD215	
Drain-source resistance							
I_D = 1,0 mA; V_{SB} = 0;							
V_{GS} = 5 V	$R_{DS(on)}$	typ.	30	30	30	30	Ω
		<	70	70	70	70	Ω
V_{GS} = 10 V	$R_{DS(on)}$	typ.	20	20	20	20	Ω
		<	45	45	45	45	
V_{GS} = 15 V	$R_{DS(on)}$	typ.	15	15	15	15	Ω
V_{GS} = 25 V	$R_{DS(on)}$	typ.	12		12		Ω

DYNAMIC CHARACTERISTICS

Forward transconductance at f = 1 kHz				
V_{DS} = 10 V; V_{SB} = 0; I_D = 20 mA	g_{fs}	typ.	15	mS
		>	10	
Capacitance at f = 1 MHz (see Fig. 2)				
$V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V				
Feed-back capacitance	C_{rss}	typ.	0,6	pF
Input capacitance	C_{iss}	typ.	2,3	pF
Output capacitance	C_{oss}	typ.	1,9	pF

DYNAMIC CHARACTERISTICS (continued)

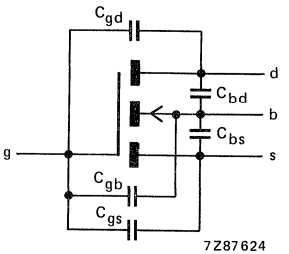


Fig. 2 Capacitances model.

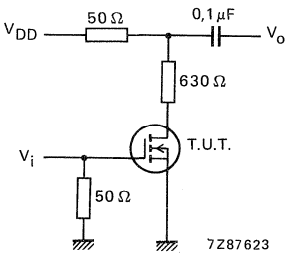
$C_{iss} = C_{GS} + C_{GD} + C_{GB}$

$C_{oss} = C_{GD} + C_{BD}$

$C_{rss} = C_{GD}$

Switching times (see Fig. 3)

V_{DD} = 10 V; V_i = −5 V to +5 V	t_{on}	typ.	1,0	ns
	t_{off}	typ.	5,0	ns



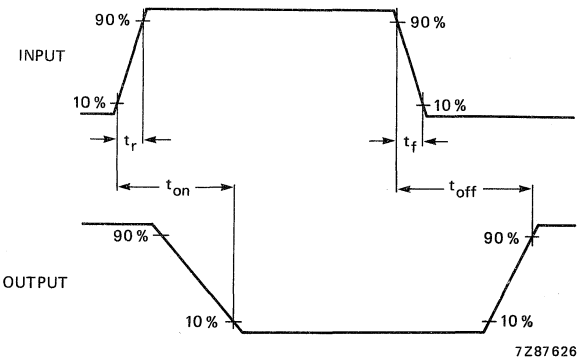


Fig. 3 Switching times test circuit and input and output waveforms.

Pulse generator:

R_i = 50 Ω

t_r < 0,5 ns

t_f < 1,0 ns

t_p = 20 ns

δ < 0,01

MOSFET N-CHANNEL ENHANCEMENT SWITCHING TRANSISTOR

Symmetrical insulated-gate silicon MOS field-effect transistor of the N-channel enhancement mode type.

The transistor is sealed in a SOT143 envelope and features a low ON resistance and low capacitances.

The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

Applications:

- analog and/or digital switch
- switch driver

QUICK REFERENCE DATA

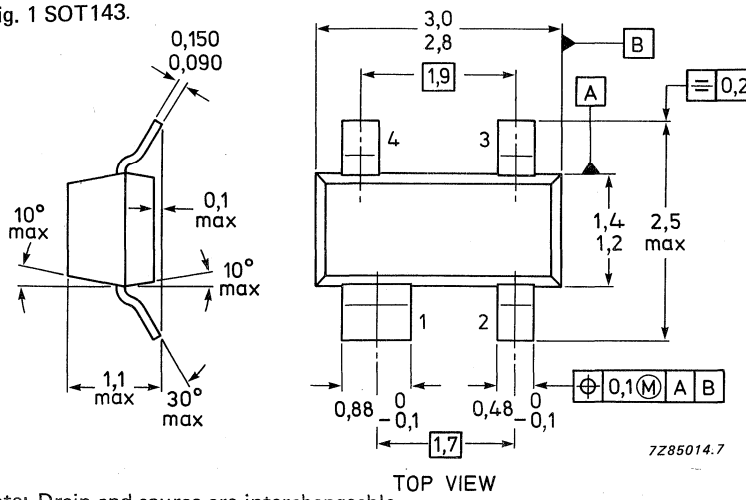
Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	230 mW
Gate-source threshold voltage $V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu A$	$V_{GS(th)}$	$>$ $<$	0.1 V 2.0 V
Drain-source ON-resistance V_{GS} = 10 V; V_{SB} = 0; I_D = 0.1 mA	R_{DSon}	$<$	45 Ω
Feed-back capacitance $V_{GS} = V_{BS} = -15$ V; V_{DS} = 10 V; f = 1 MHz	C_{rss}	typ.	0.6 pF

MECHANICAL DATA

SOT143 (see Fig. 1).

See also *Soldering recommendations*.

Fig. 1 SOT143.



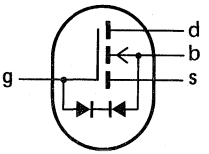
Dimensions in mm

Marking code:

BSS83 = M74

Pinning;

1 = substrate (b)
2 = source
3 = drain
4 = gate



Note: Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	10 V
Source-drain voltage	V_{SD}	max.	10 V
Drain-substrate voltage	V_{DB}	max.	15 V
Source-substrate voltage	V_{SB}	max.	15 V
Drain current (DC)	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	230 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	125 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

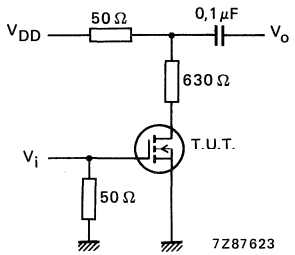
Drain-source breakdown voltage $V_{GS} = V_{BS} = -5$ V; I_D = 10 nA	$V_{(BR)DSX}$	>	10 V
Source-drain breakdown voltage $V_{GD} = V_{BD} = -5$ V; I_D = 10 nA	$V_{(BR)SDX}$	>	10 V
Drain-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open source	$V_{(BR)DBO}$	>	15 V
Source-substrate breakdown voltage V_{GB} = 0; I_D = 10 nA; open drain	$V_{(BR)SBO}$	>	15 V
Drain-source leakage current $V_{GS} = V_{BS} = -2$ V; V_{DS} = 6,6 V	I_{DSoff}	<	10 nA

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Source-drain leakage current			
$V_{GD} = V_{BD} = -2$ V; $V_{SD} = 6{,}6$ V	I_{SDoff}	<	10 nA
Forward transconductance at f = 1 kHz			
$V_{DS} = 10$ V; $V_{SB} = 0$; $I_D = 20$ mA	g_{fs}	>	10 mS
		typ.	15 mS
Gate-source threshold voltage			
$V_{DS} = V_{GS}$; $V_{SB} = 0$; $I_D = 1\ \mu$A	$V_{GS(th)}$	>	0,1 V
		<	2,0 V
Drain-source ON-resistance			
$I_D = 0{,}1$ mA;			
$V_{GS} = 5$ V; $V_{SB} = 0$	R_{DSon}	<	70 Ω
$V_{GS} = 10$ V; $V_{SB} = 0$	R_{DSon}	<	45 Ω
$V_{GS} = 3{,}2$ V; $V_{SB} = 6{,}8$ V (see Fig. 4)	R_{DSon}	typ.	80 Ω
		<	120 Ω
Gate-substrate zener voltages			
$V_{DB} = V_{SB} = 0$; $-I_G = 10\ \mu$A	$V_{Z(1)}$	>	12,5 V
$V_{DB} = V_{SB} = 0$; $+I_G = 10\ \mu$A	$V_{Z(2)}$	>	12,5 V
Capacitances at f = 1 MHz			
$V_{GS} = V_{BS} = -15$ V; $V_{DS} = 10$ V			
Feed-back capacitance	C_{rss}	typ.	0,6 pF
Input capacitance	C_{iss}	typ.	1,5 pF
Output capacitance	C_{oss}	typ.	1,0 pF
Switching times (see Fig. 2)			
$V_{DD} = 10$ V; $V_i = 5$ V	t_{on}	typ.	1,0 ns
	t_{off}	typ.	5,0 ns

Pulse generator:

$R_i = 50\ \Omega$
$t_r < 0{,}5$ ns
$t_f < 1{,}0$ ns
$t_p = 20$ ns
$\delta < 0{,}01$



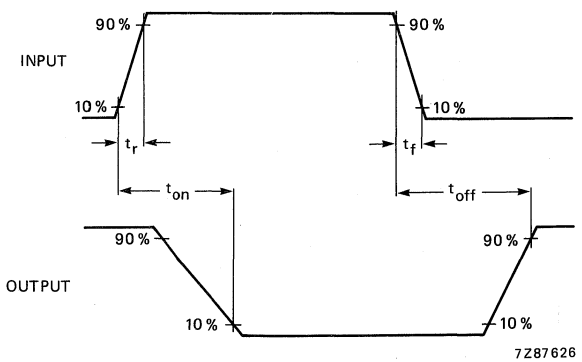


Fig. 2 Switching times test circuit and input and output waveforms.

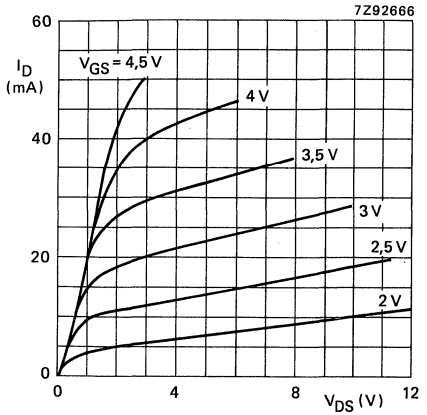


Fig. 3 V_{SB} = 0; typical values.

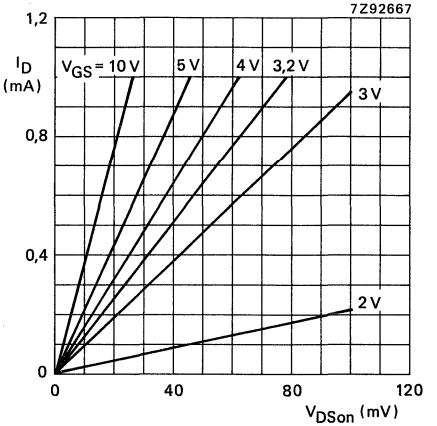


Fig. 4 V_{SB} = 6,8 V; typical values.

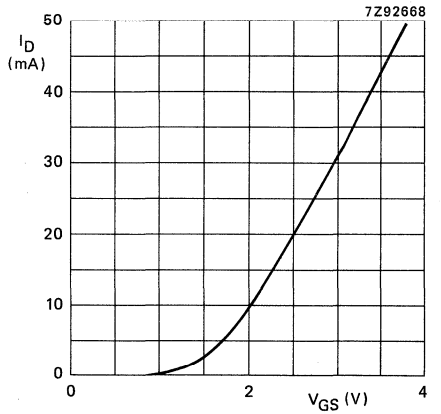


Fig. 5 V_{DS} = 10 V; V_{BS} = 0; typical values.

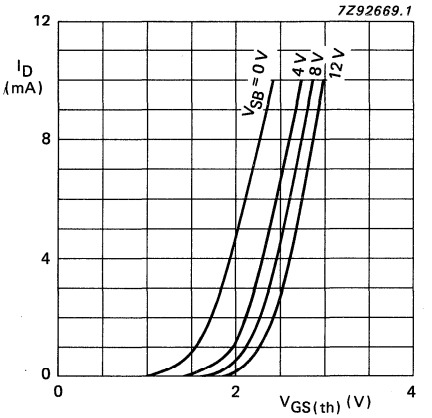


Fig. 6 $V_{DS} = V_{GS} = V_{GS(th)}$.

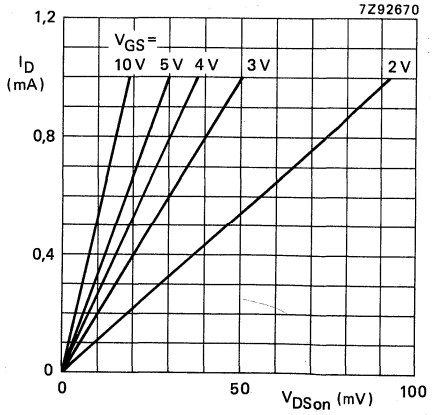


Fig. 7 V_{SB} = 0; typical values.

Conditions for Figs 3, 4, 5, 6 and 7:
T_j = 25 °C.

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

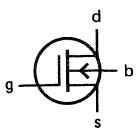
Drain-source resistance (on) at f = 1 kHz			
V_{DS} = 0; V_{GS} = 5 V; V_{BS} = 0	$R_{ds\ on}$	max.	50 Ω
Drain-source resistance (off)			
V_{DS} = 10 V; $-V_{GS}$ = 5 V; V_{BS} = 0	$R_{DS\ off}$	min.	10 GΩ
Feedback capacitance at f = 1 MHz			
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	typ.	0.5 pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	typ.	0.5 pF

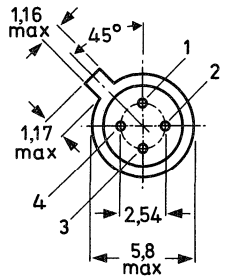
MECHANICAL DATA

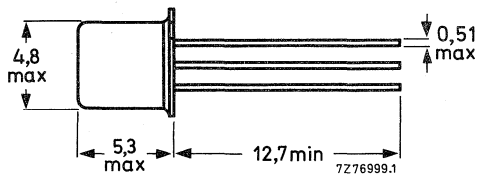
Dimensions in mm

Fig. 1 TO-72.

Pinning
1 = drain
2 = source
3 = gate
4 = substrate (b) connected to case







Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	V_{GB}	max. min.	10 V −10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 V −15 V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	V_{G-N}	max. min.	50 V −50 V
Drain current (DC)	I_D	max.	25 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{DM}	max.	50 mA
Source current (peak value) $t_p = 20$ ms; $\delta = 0.1$	I_{SM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 125 °C
Junction temperature	T_j	max.	125 °C

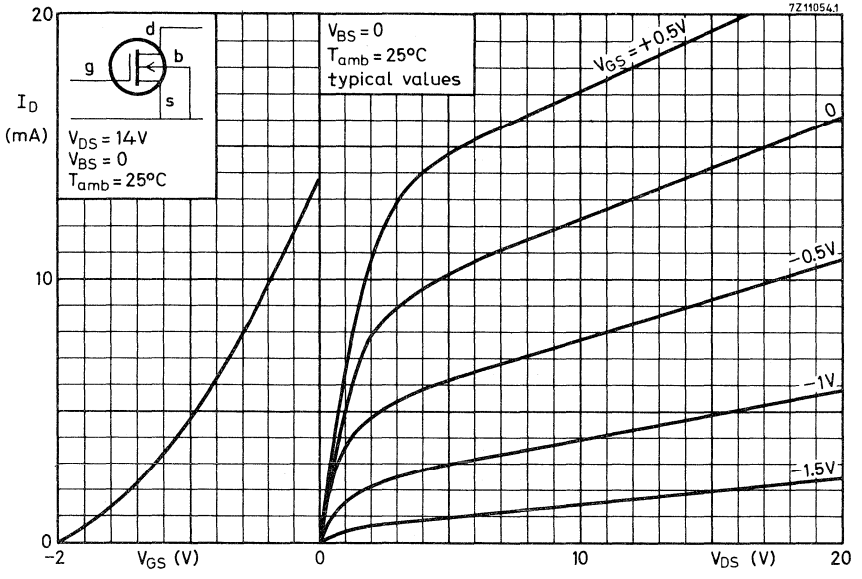
THERMAL RESISTANCE

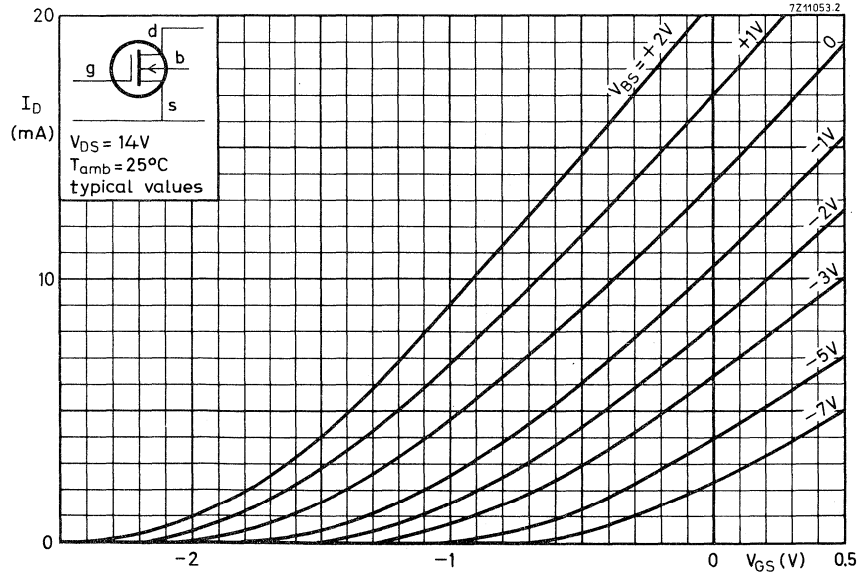
From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W

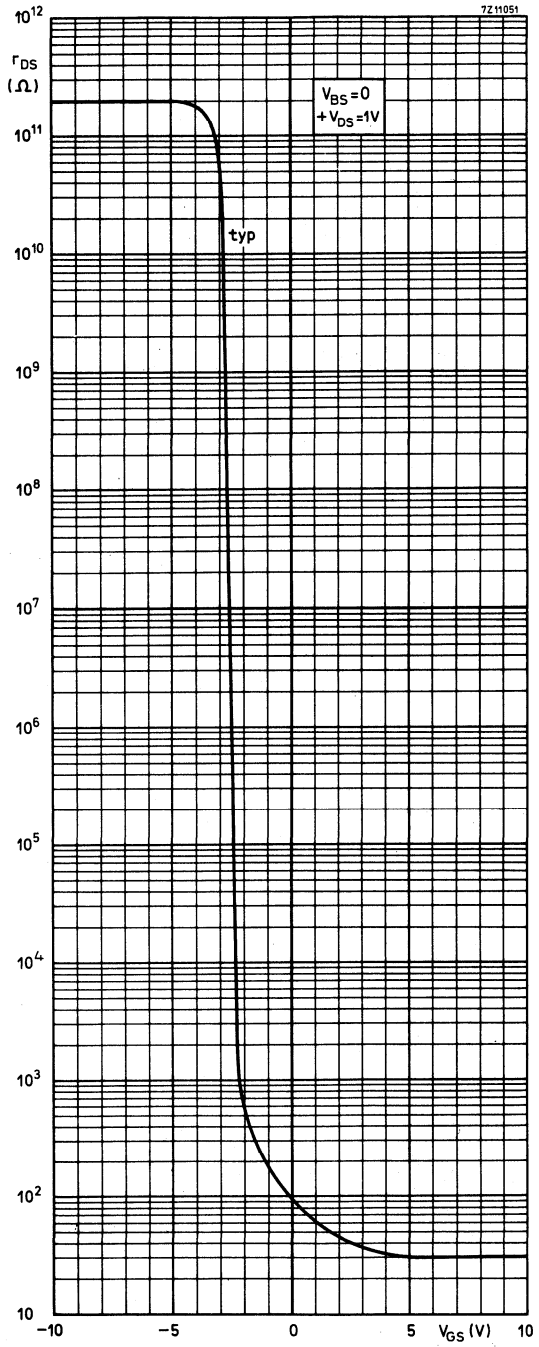
CHARACTERISTICS

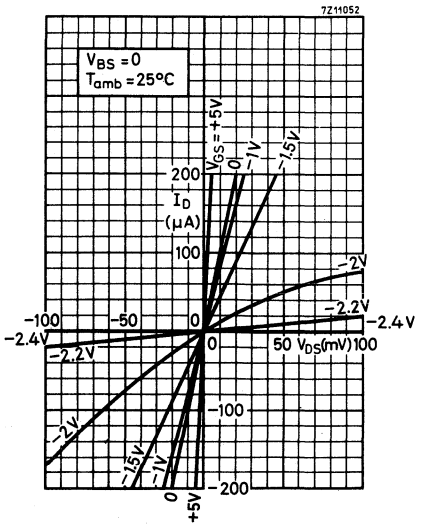
T_j = 25 °C unless otherwise specified

Drain cut-off currents; V_{BS} = 0				
V_{DS} = 10 V; $-V_{GS}$ = 5 V	I_{DSX}	<	1	nA
V_{DS} = 10 V; $-V_{GS}$ = 5 V; T_j = 125 °C	I_{DSX}	<	1	µA
Source cut-off currents; V_{BD} = 0				
V_{SD} = 10 V; $-V_{GD}$ = 5 V	I_{SDX}	<	1	nA
V_{SD} = 10 V; $-V_{GD}$ = 5 V; T_j = 125 °C	I_{SDX}	<	1	µA
Gate currents; V_{BS} = 0				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 °C	I_{GSS}	<	200	pA
Bulk currents; V_{GB} = 0				
$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	µA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	µA
Drain-source resistance (on) at f = 1 kHz; V_{BS} = 0				
V_{GS} = 0 ; V_{DS} = 0	$R_{ds\ on}$	<	100	Ω
V_{GS} = 0 ; V_{DS} = 0; T_j = 125 °C	$R_{ds\ on}$	<	150	Ω
$+V_{GS}$ = 5 V; V_{DS} = 0	$R_{ds\ on}$	<	50	Ω
Drain-source resistance (off)				
$-V_{GS}$ = 5 V; V_{DS} = 10 V; V_{BS} = 0	$R_{DS\ off}$	>	10	GΩ
Feedback capacitances at f = 1 MHz				
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	typ.	0.5	pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	typ.	0.5	pF
Gate to all other terminals capacitance at f = 1 MHz				
$-V_{GB}$ = 5 V; V_{SB} = V_{DB} = 0	C_{g-n}	<	6	pF


7Z11054.1
d
g
b
s
V_{BS} = 0
T_{amb} = 25°C
typical values
V_{DS} = 14V
V_{BS} = 0
T_{amb} = 25°C
I_D
(mA)
V_{GS} = +0.5V
0
−0.5V
−1V
−1.5V
20
10
0
−2
V_{GS} (V)
0
10
V_{DS} (V)
20


7Z11053.2
d
g
b
s
V_{DS} = 14V
T_{amb} = 25°C
typical values
I_D
(mA)
V_{BS} = +2V
+1V
0
−1V
−2V
−3V
−5V
−7V
20
10
0
−2
−1
0
V_{GS} (V)
0.5


7Z11051
10^{12}
r_{DS} (Ω)
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
V_{BS} = 0
+V_{DS} = 1V
typ
−10
−5
0
5
V_{GS} (V)
10


7Z11052
V_{BS} = 0
T_{amb} = 25°C
I_D (μA)
200
100
−100
−50
0
50
100
V_{DS}(mV)
V_{GS} = +5V
0
−1V
−1.5V
−2V
−2.2V
−2.4V
−100
−200
+5V

DEVICE DATA
MOS-FETs
dual gate

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8 dB

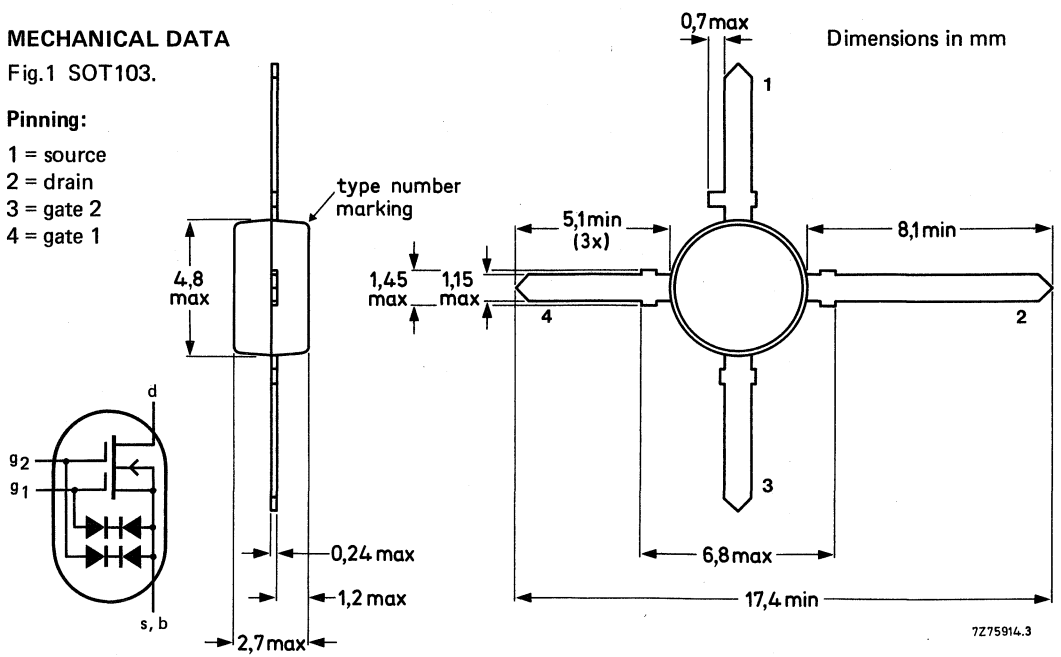
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

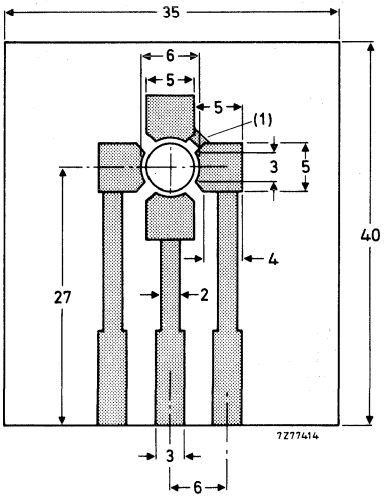
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S}$ = V_{DS} = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.7 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.7 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5 mS
		typ.	12 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	1.8 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9 pF
Noise figure at G_S = 2 mS; B_S = B_S opt			
f = 200 MHz	F	typ.	1.6 dB
f = 800 MHz	F	typ.	2.8 dB
Power gain at G_S = 2 mS; B_S = B_S opt			
G_L = 0.5 mS; B_L = B_L opt; f = 200 MHz	G_p	typ.	23 dB
G_L = 1 mS; B_L = B_L opt; f = 800 MHz	G_p	typ.	16.5 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications in television tuners. The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

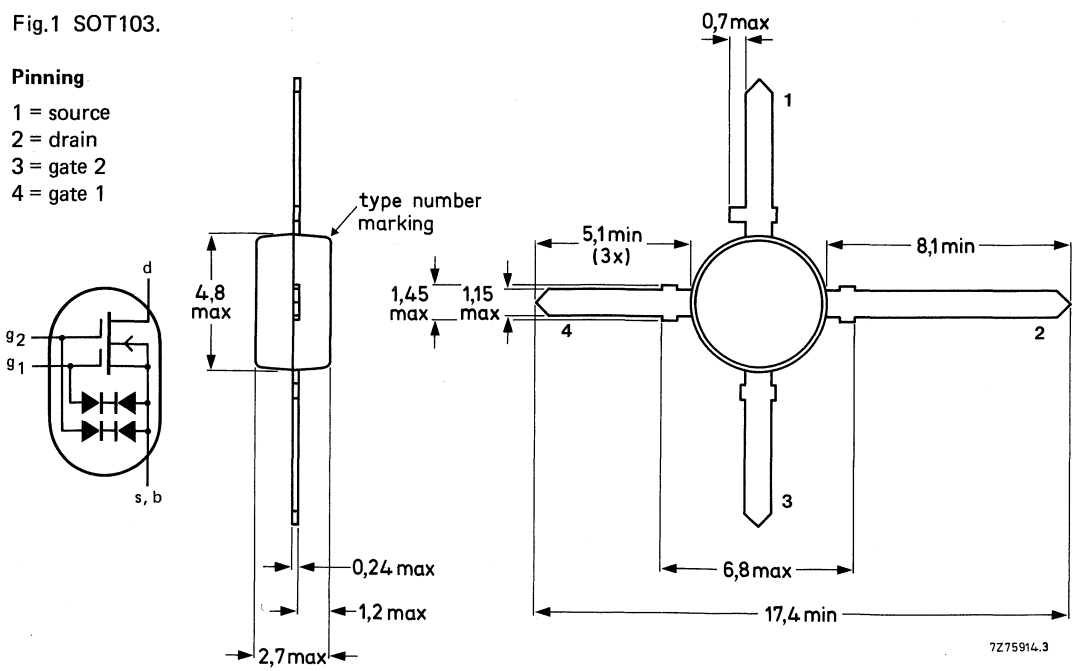
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

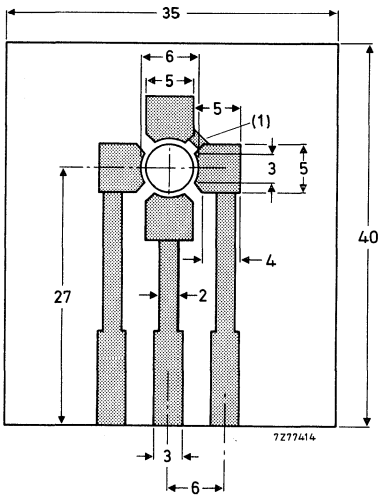
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	6.0 to 20 V	
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	6.0 to 20 V	
Drain current			
V_{DS} = 15 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}	4 to 20 mA	
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.5 pF
		max.	3.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at G_S = 2 mS ; $B_S = B_S$ opt f = 200 MHz	F	typ.	1.0 dB
Power gain at G_S = 2 mS ; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

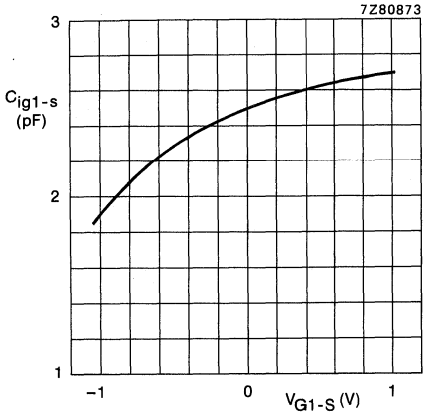


Fig. 3 V_{G2-S} = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

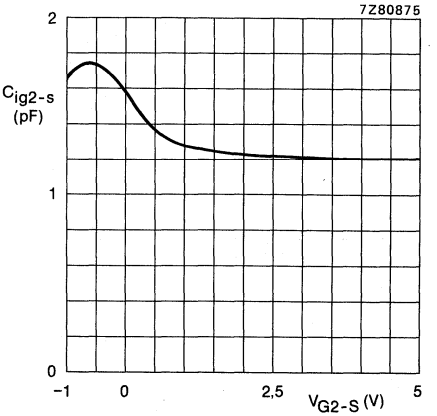


Fig. 4 V_{G1-S} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

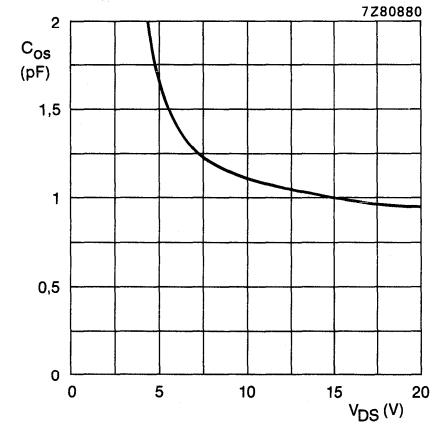


Fig. 5 V_{G2-S} = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

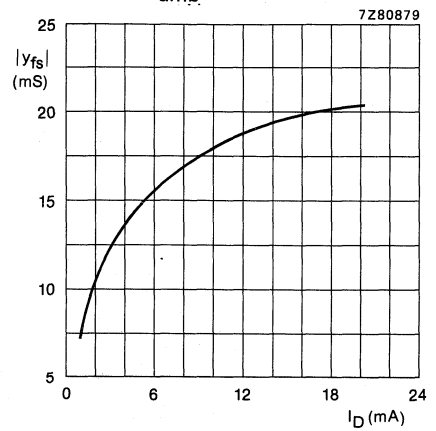


Fig. 6 V_{G2-S} = 4; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

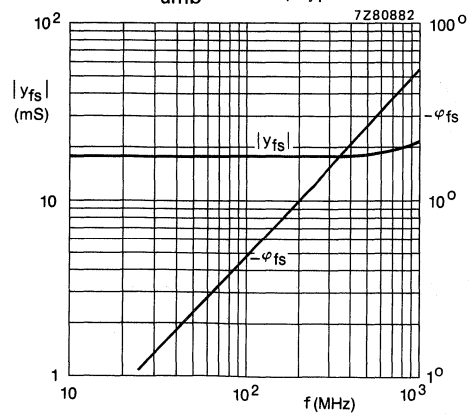


Fig. 7 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

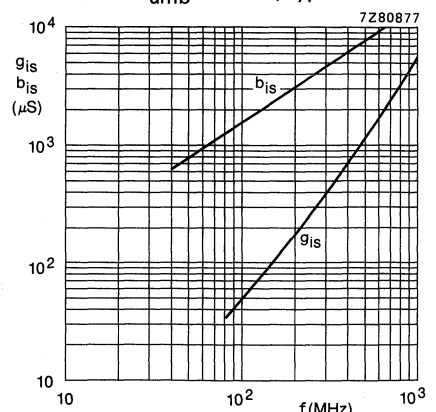


Fig. 8 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

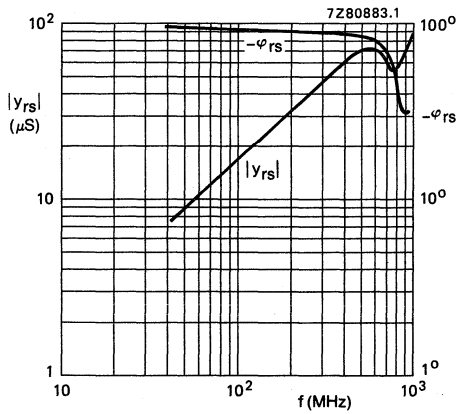


Fig. 9 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

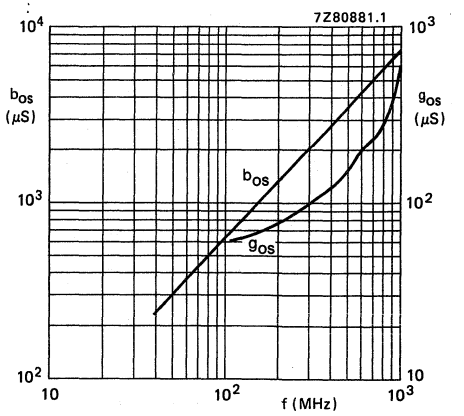


Fig. 10 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

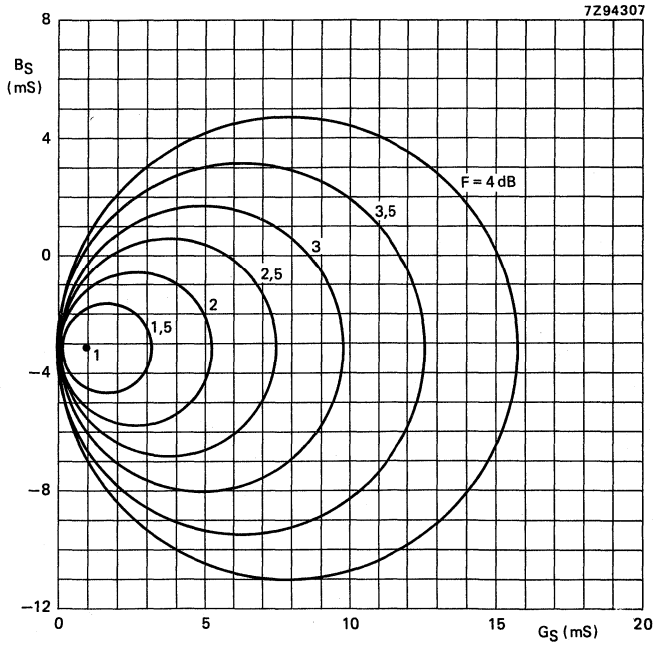


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with large tuning ranges up to 500 MHz.

QUICK REFERENCE DATA

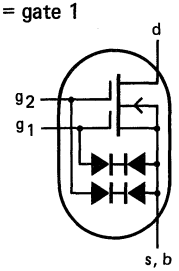
Drain-source voltage	V_{DS}	max.	20 V
Drain-current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2,5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_{Sopt} I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1,0 dB

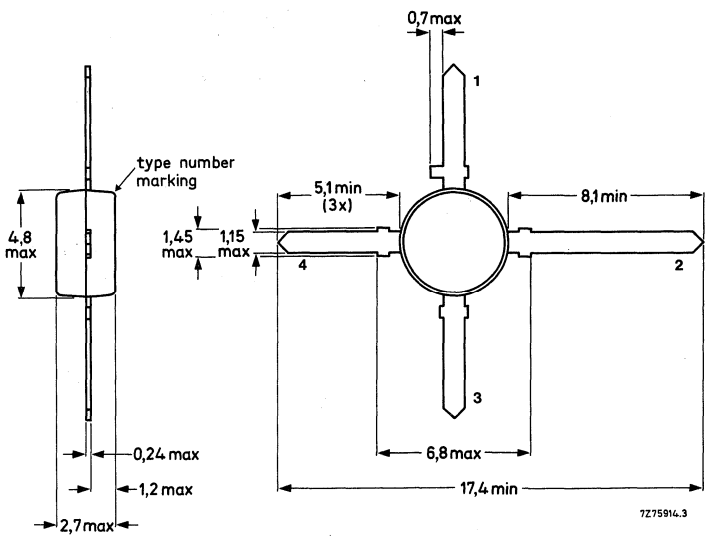
MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT103.

Pinning
1 = source
2 = drain
3 = gate 2
4 = gate 1





RATINGS

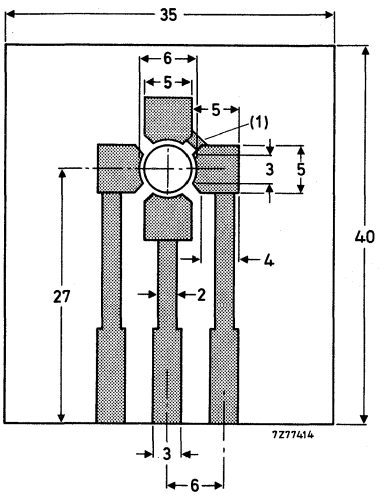
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain-current (DC or average)	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on a printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless stated otherwise

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	<	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	<	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6,0 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6,0 to 20 V
Drain current			
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; $V_{G2\text{-}S}$ = 4 V	I_{DSS}		2,0 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	<	2,5 V
I_D = 20 μA; V_{DS} = 15 V; + $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	<	2,0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source); I_D = 10 mA; V_{DS} = 15 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	15 mS
		typ.	18 mS
Input capacitance at gate 1 at f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2,5 pF
Input capacitance at gate 2 at f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1,2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,0 pF
Noise figure at G_S = 2 mS; $B_S = B_{Sopt}$ and f = 200 MHz	F	typ.	1,0 dB
Power gain at G_S = 2 mS; $B_S = B_{Sopt}$ G_L = 0,5 mS; $B_L = B_{Lopt}$; f = 200 MHz	G_P	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 3.3 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	1.8 dB

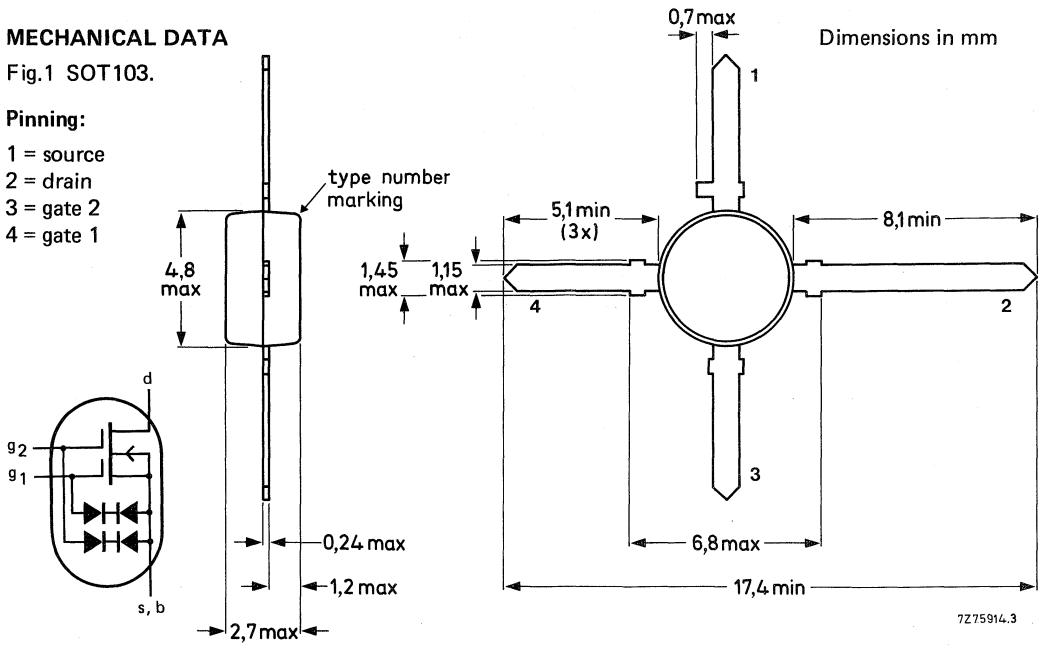
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



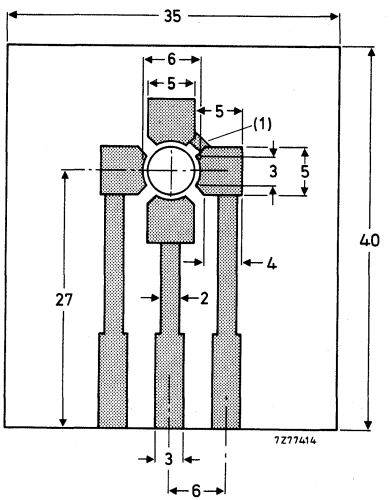
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335 K/W



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	50 nA
$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		6 to 20 V
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0; + $V_{G2\text{-}S}$ = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ.	2.3 pF
		max.	2.6 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.1 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
f = 800 MHz; G_S = 3.3 mS; $B_S = B_S$ opt	F	typ.	1.8 dB
Power gain			
f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS; B_S = opt; B_L = opt	G_p	typ.	25 dB
f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS; B_S = opt; B_L = opt	G_p	typ.	18 dB

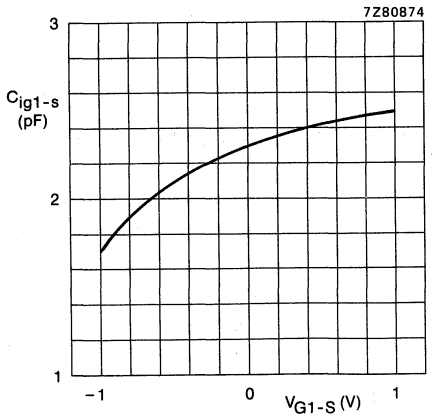


Fig.3 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

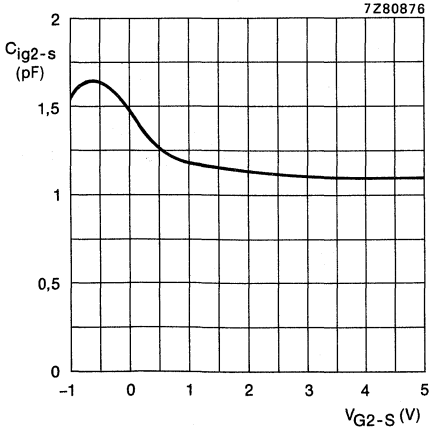


Fig.4 $V_{G1\text{-}S}$ = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{amb} = 25 °C; typical values.

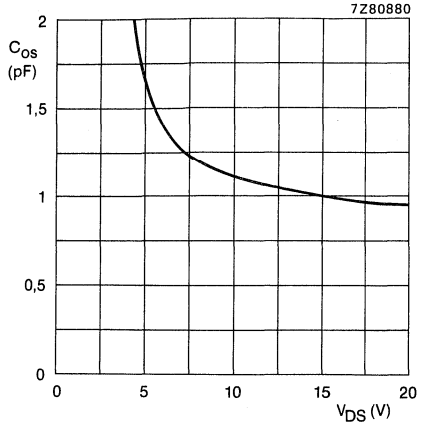


Fig. 5 V_{G2-S} = 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C; typical values.

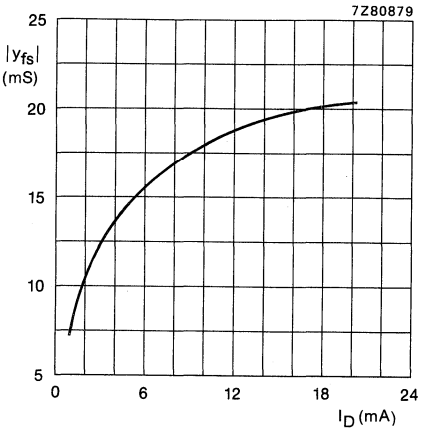


Fig. 6 V_{G2-S} = 4 V; V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

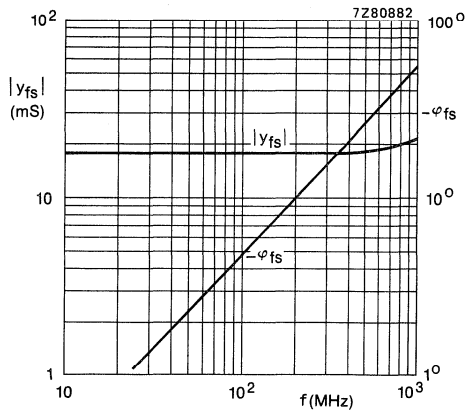


Fig. 7 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

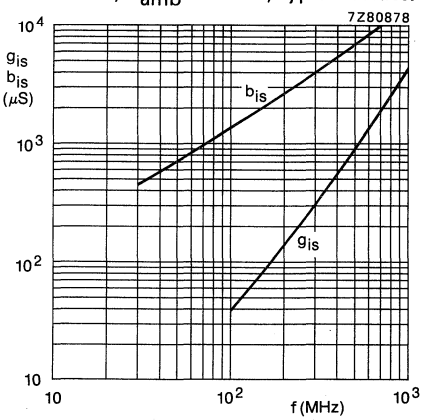


Fig. 8 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

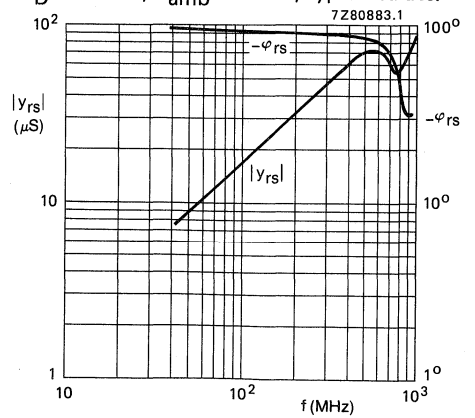


Fig. 9 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

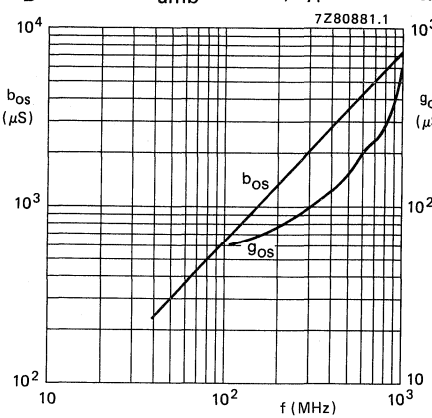


Fig. 10 V_{G2-S} = 4 V; V_{DS} = 15 V; I_D = 10 mA; T_{amb} = 25 °C; typical values.

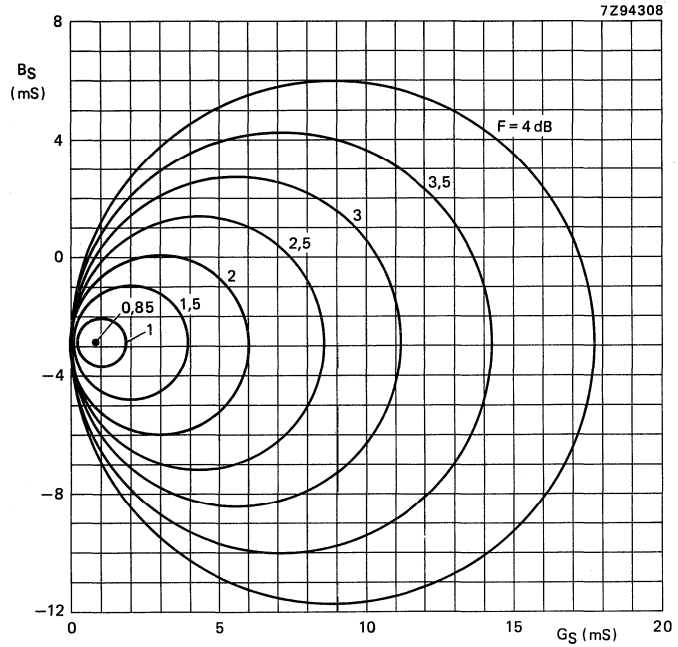


Fig. 11 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA;
f = 200 MHz; T_{amb} = 25 °C; typical values.

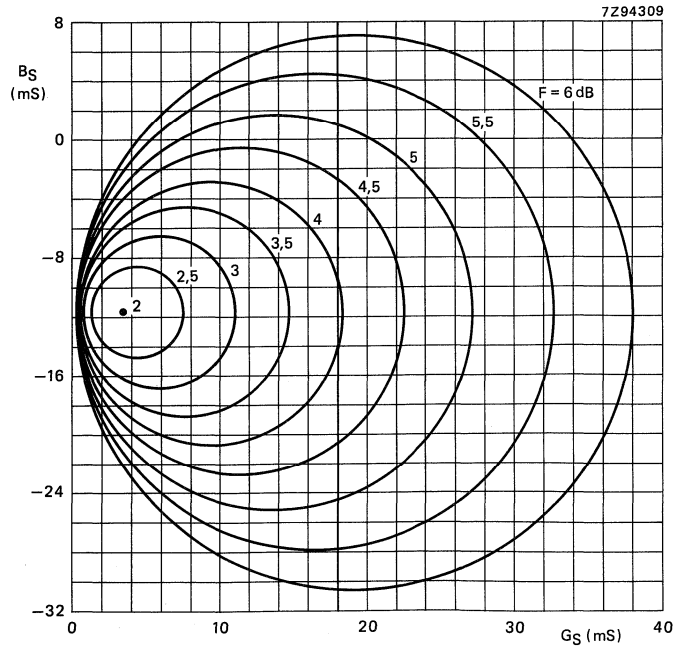


Fig. 12 $V_{G2\text{-}S}$ = 4 V; V_{DS} = 15 V; I_D = 10 mA;
f = 800 MHz; T_{amb} = 25 °C; typical values.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected. Intended for UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment.
This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current (DC)	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 5 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0 dB

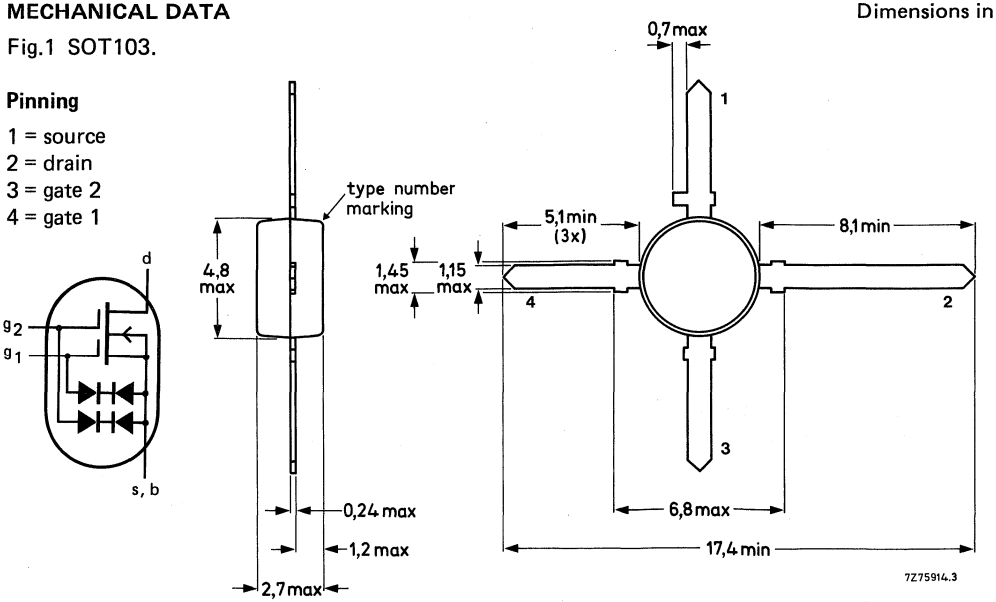
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

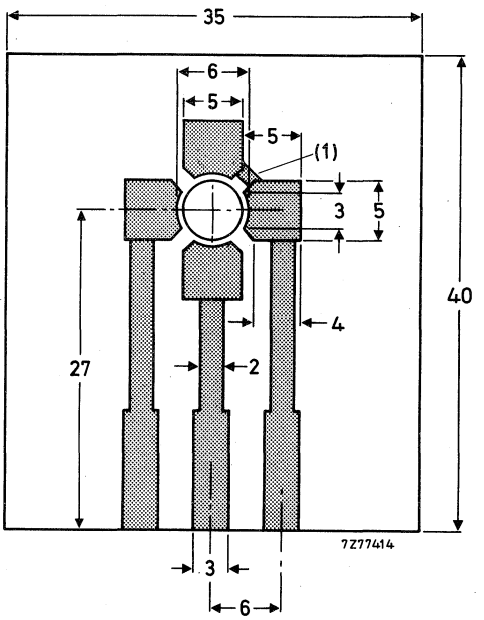
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig.2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 7 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	25 nA
± V_{G2-S} = 7 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	25 nA
Gate-source breakdown voltages			
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		8 to 20 V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	min.	0.2 V
		max.	1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	min.	0.2 V
		max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	18 mS
		typ.	19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.6 pF
		max.	3.0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
		max.	35 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.1 pF
Noise figure at f = 800 MHz; G_S = 5 mS; B_S = B_S opt	F	typ.	2.0 dB
		max.	3.0 dB

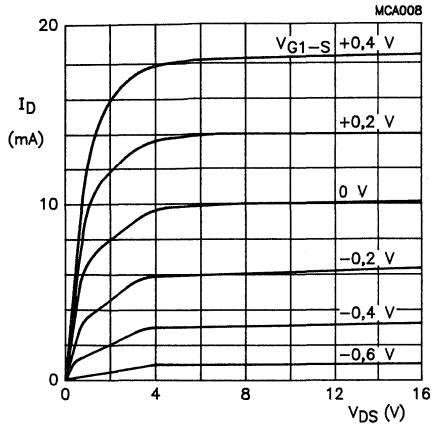


Fig.3 Output characteristics.
$V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

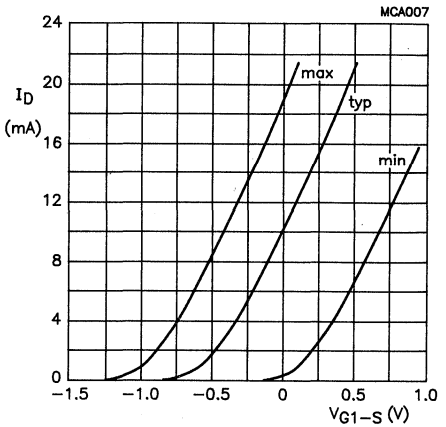


Fig.4 Transfer characteristics.
V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

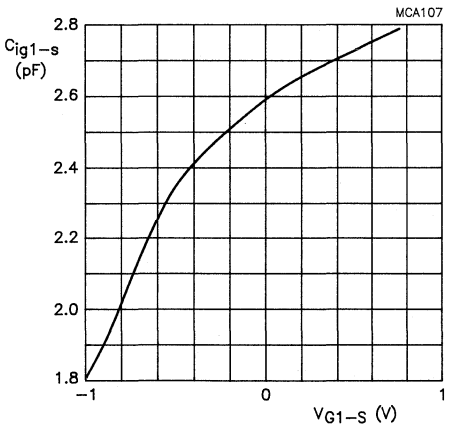


Fig.5 Gate 1 input capacitance as a function of gate 1 source voltage;
f = 1 MHz; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

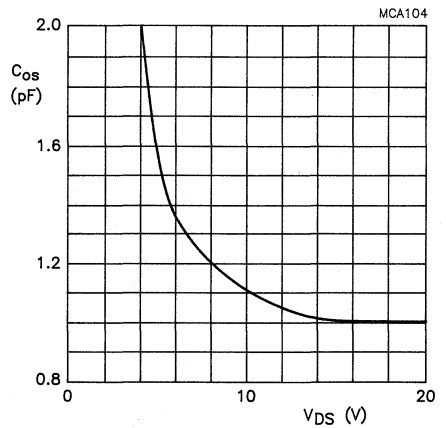


Fig.6 Output capacitance as a function of drain voltage; f = 1 MHz;
I_D = 10 mA; $V_{G2\text{-}S}$ = 4 V;
T_{amb} = 25 °C.

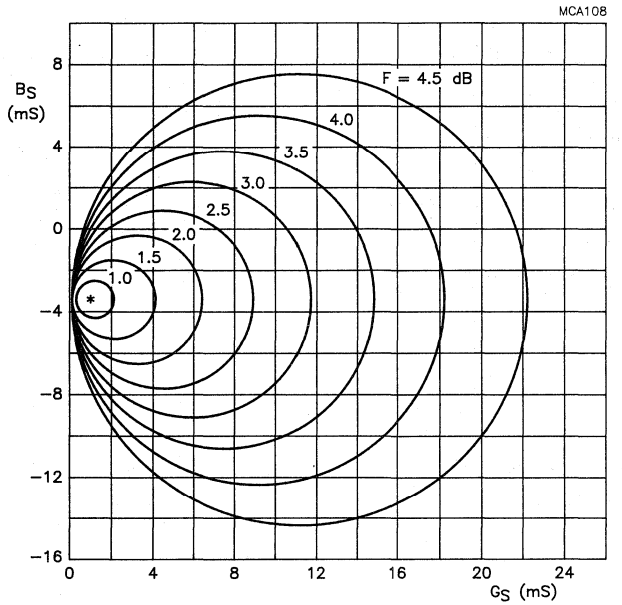


Fig.7 Circles of constant noise figures; f = 200 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

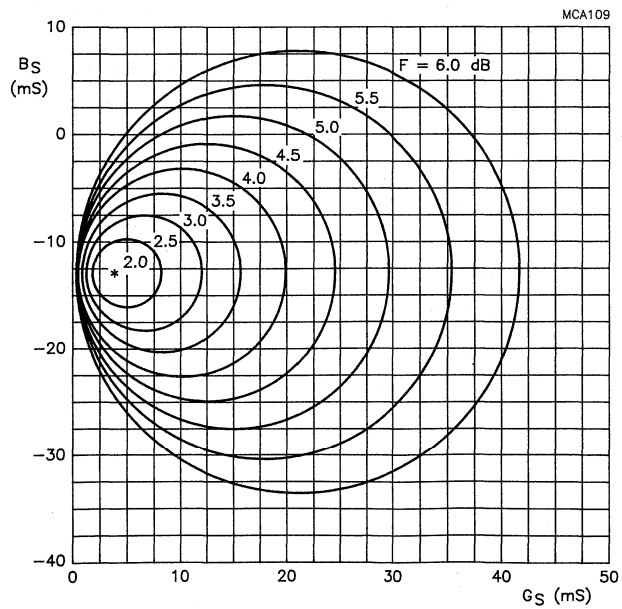


Fig.8 Circles of constant noise figures; f = 800 MHz; T_{amb} = 25 °C; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA.

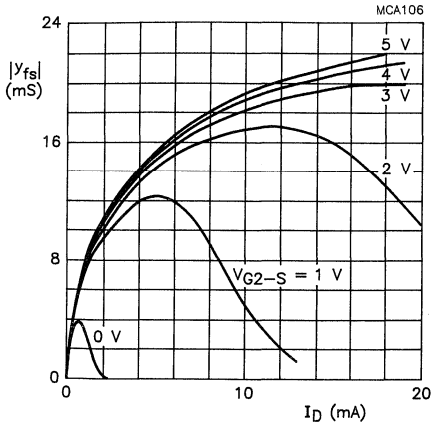


Fig.9 Forward transfer admittance as a function of drain current; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

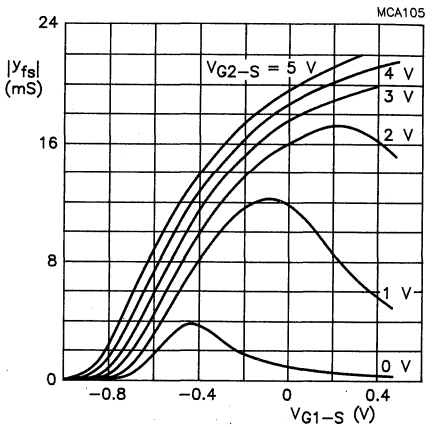


Fig.10 Forward transfer admittance as a function of gate 1 source voltage; f = 1 kHz; V_{DS} = 10 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	14 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	2.1 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	0.7 dB

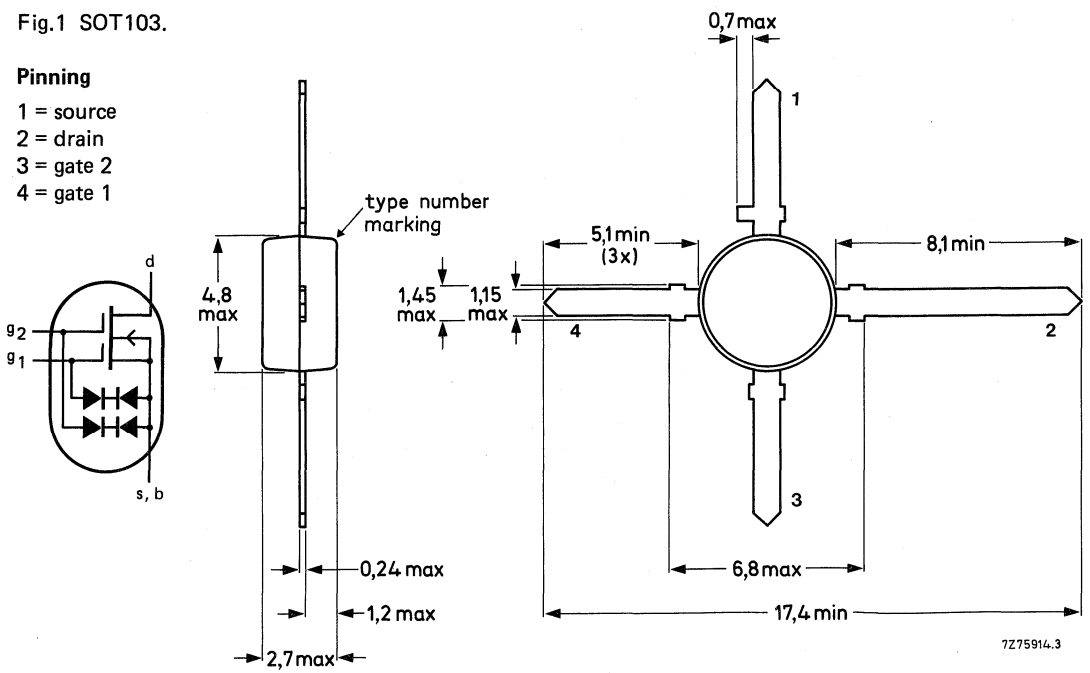
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



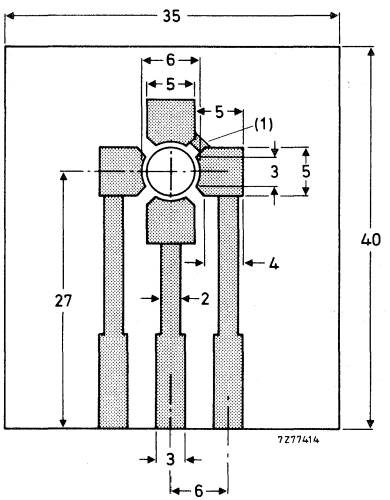
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	20	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig.2)	$R_{th\ j-a}$	=	335	K/W



Dimensions in mm

(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	<	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	6 to 20	V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	6 to 20	V
Drain current			
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}	4 to 25	mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	< 2.5	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	< 2.5	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	> 10 typ. 14	mS mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. 2.1	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ. 1.0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. 20	fF
Output capacitance at f = 1 MHz	C_{os}	typ. 1.1	pF
Noise figure at f = 100 MHz; G_S = 1 mS; $B_S = B_S$ opt	F	typ. 0.7 < 1.7	dB dB
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ. 1.0 < 2.0	dB dB
Transducer gain at f = 100 MHz; G_S = 1 mS; $B_S = B_S$ opt; G_L = 0.5 mS; $B_L = B_L$ opt	G_{tr}	typ. 29	dB
Transducer gain at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt; G_L = 0.5 mS; $B_L = B_L$ opt	G_{tr}	typ. 26	dB

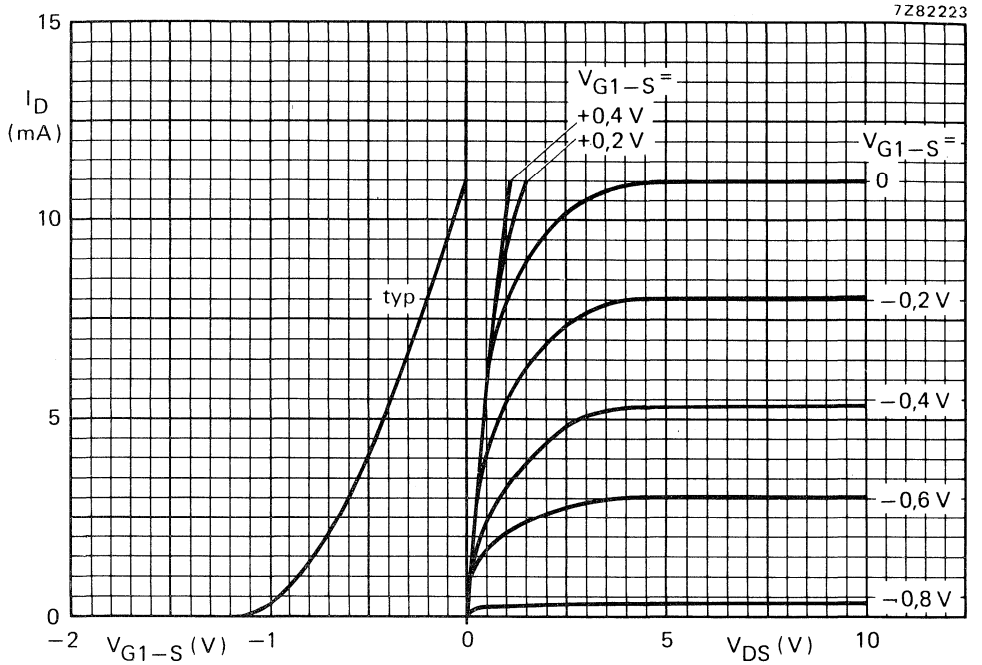


Fig. 3 **Left-hand graph:** V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C. **Right-hand graph:** V_{G2-S} = + 4 V; T_{amb} = 25 °C.

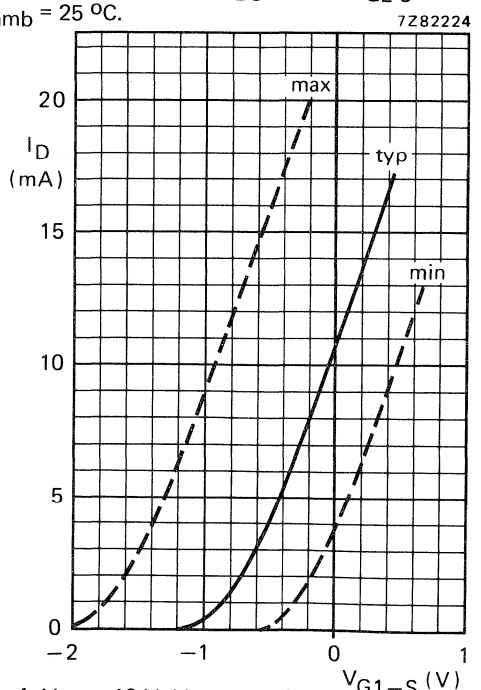


Fig. 4 V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

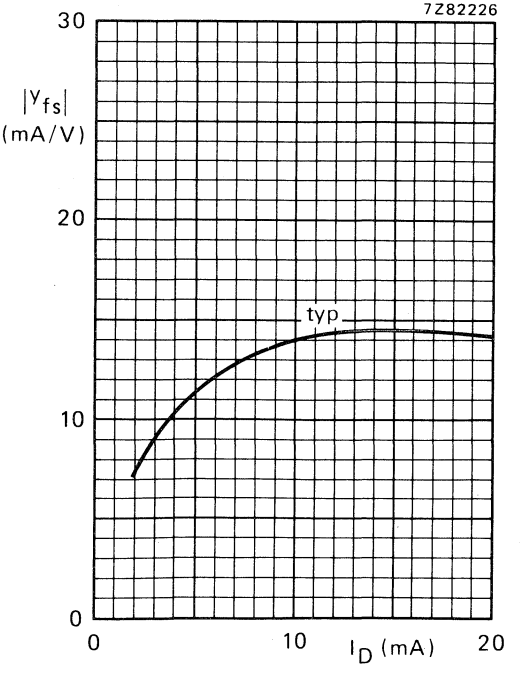


Fig. 5 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 kHz; T_{amb} = 25 °C.

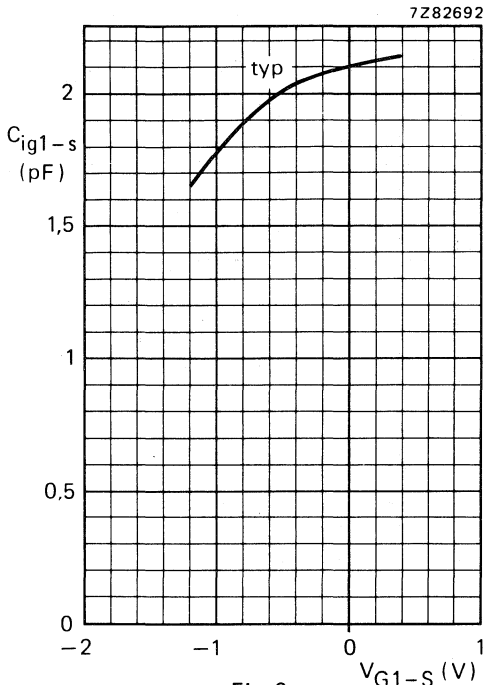


Fig. 6.

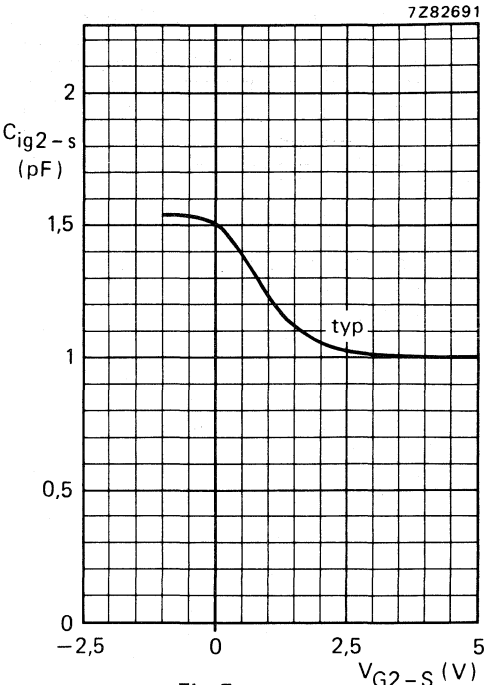


Fig. 7.

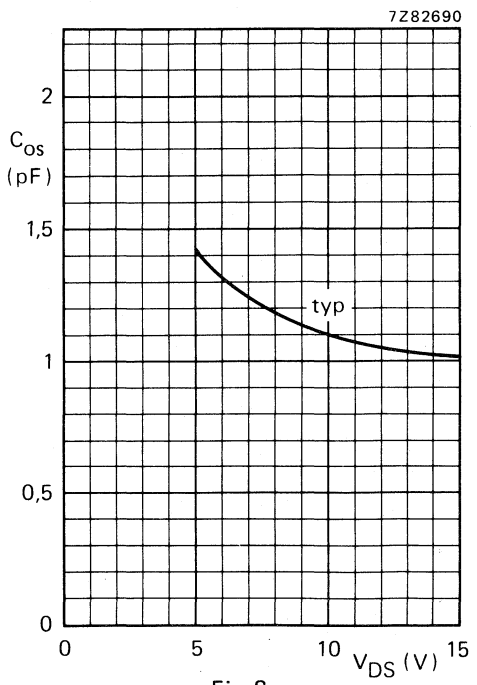


Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 V_{G2-S} = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

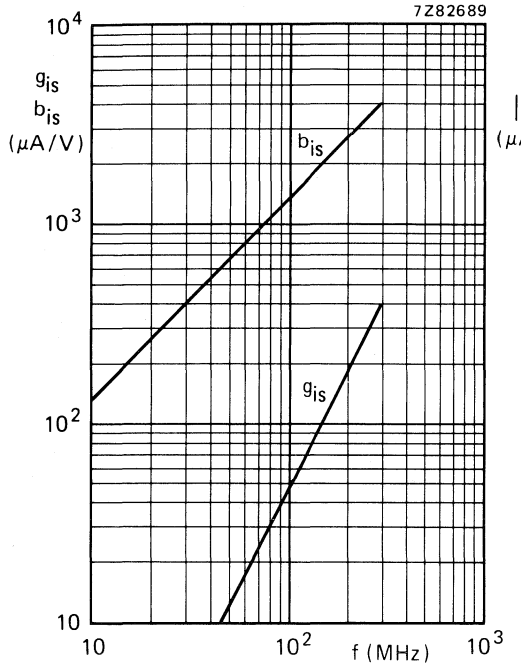


Fig. 9.

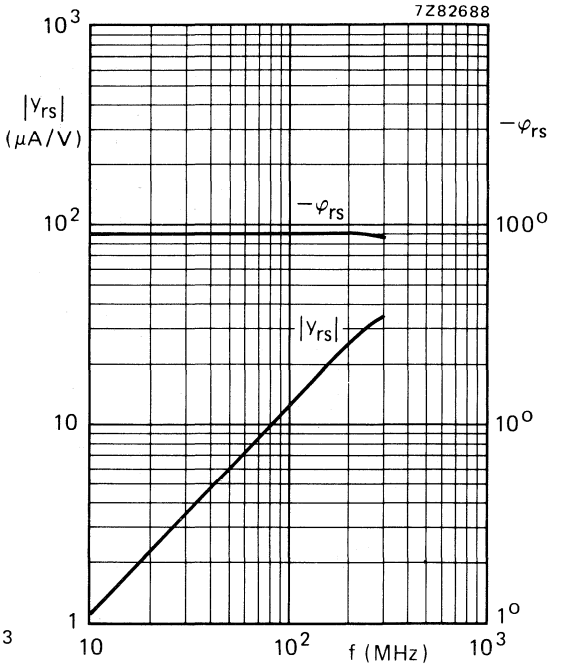


Fig. 10.

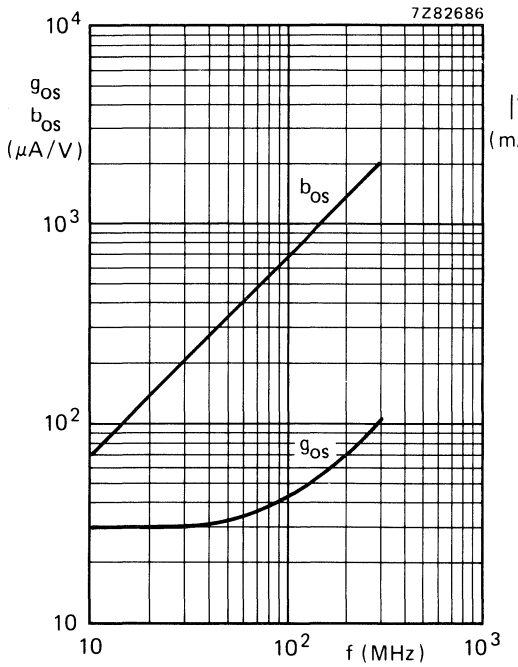


Fig. 11.

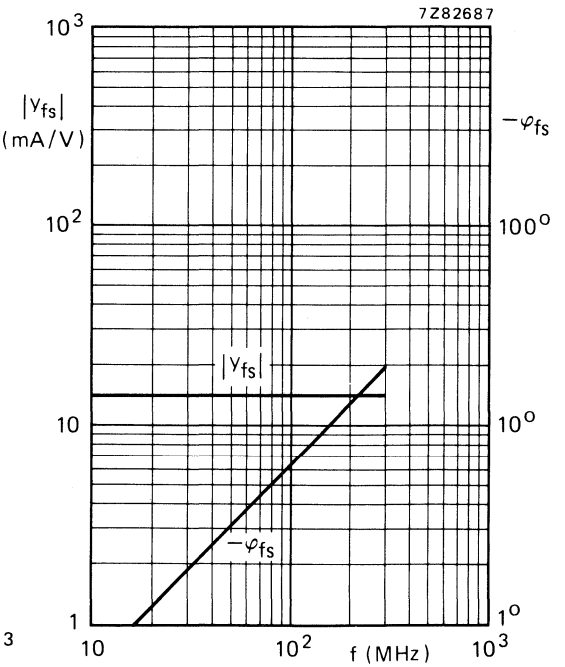


Fig. 12.

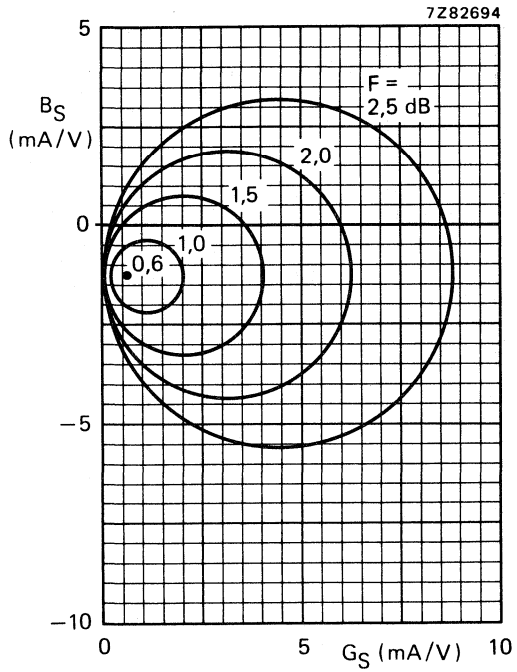


Fig. 13 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 100 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

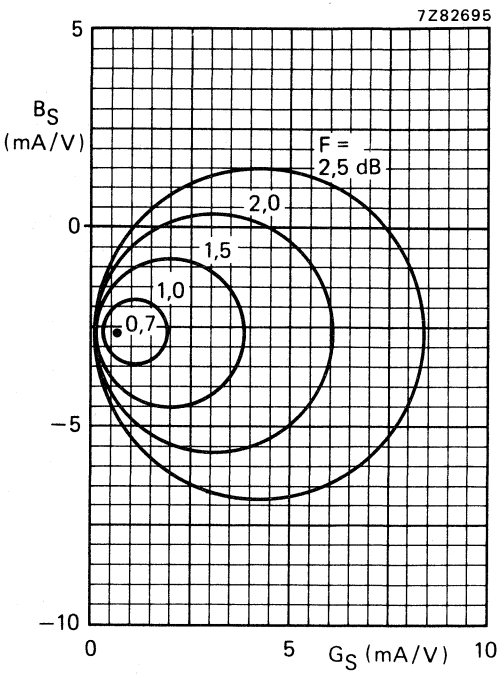


Fig. 14 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

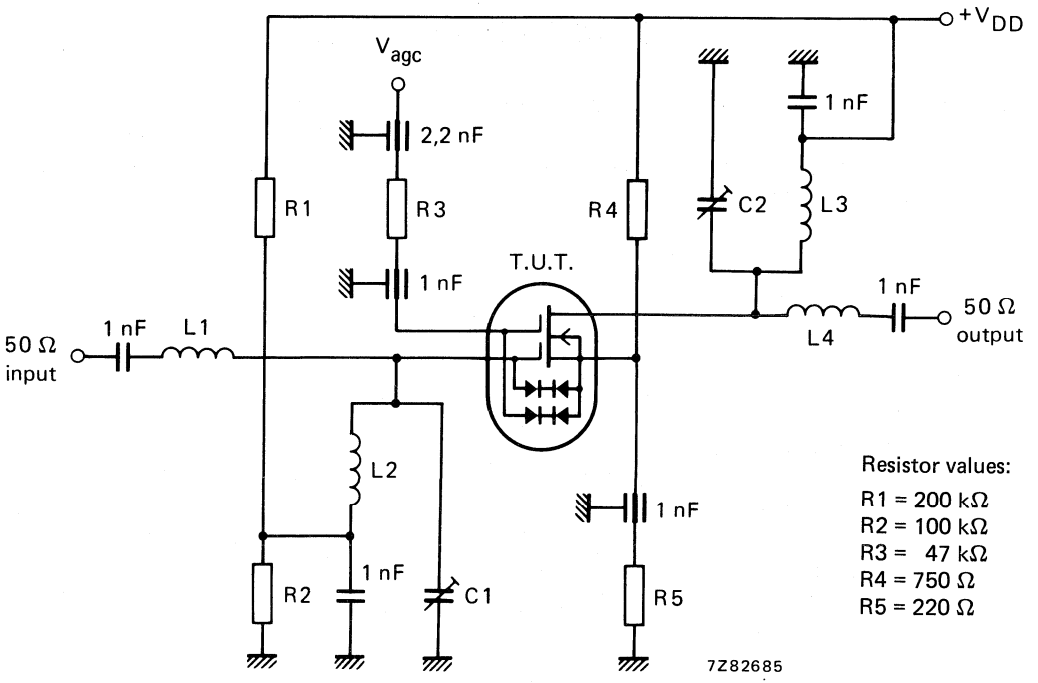


Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

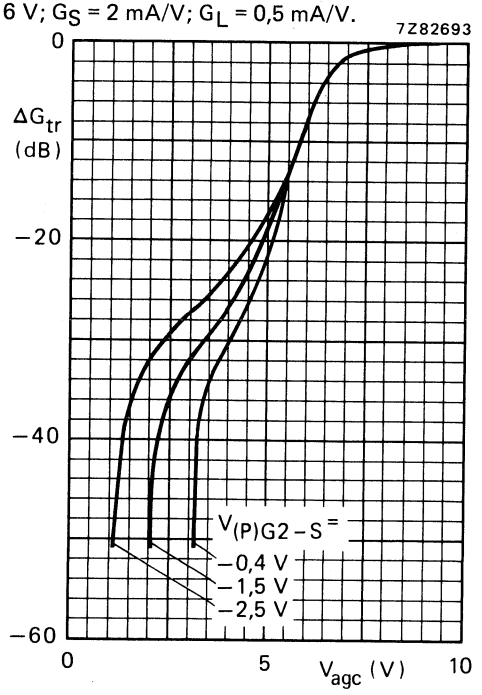


Fig. 16 V_{DD} = 16 V; f = 200 MHz; T_{amb} = 25 °C; typical values; see also Fig. 15.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF applications, such as VHF television tuners, FM tuners, with 12 V supply voltage.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4.0 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

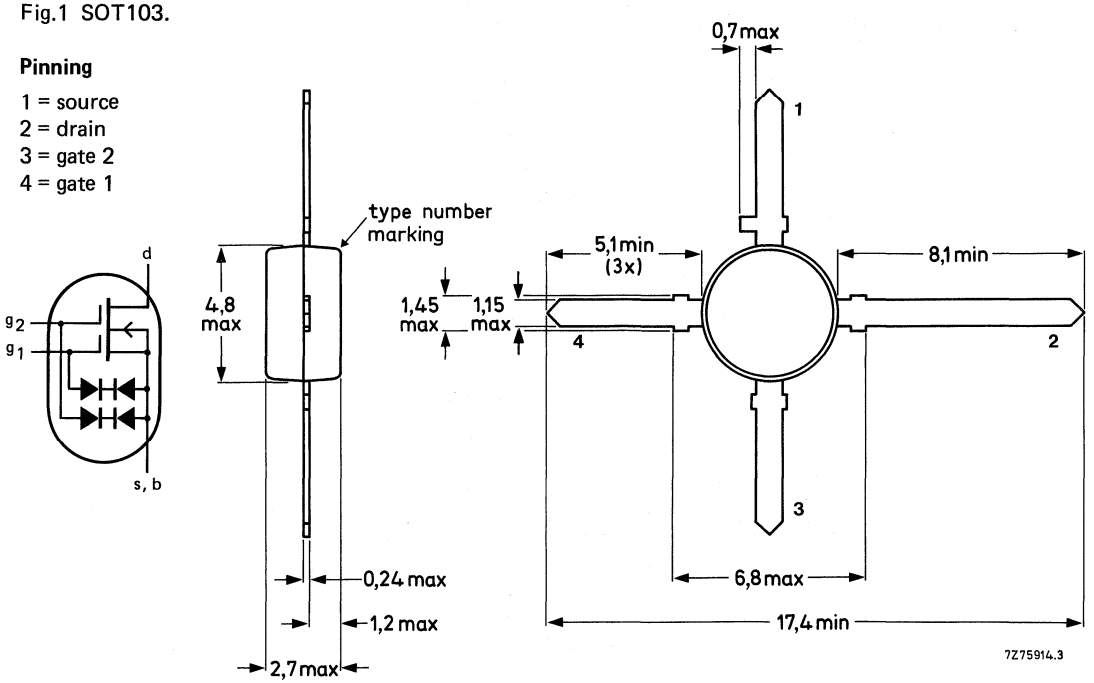
MECHANICAL DATA

Dimensions in mm

Fig.1 SOT103.

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



RATINGS

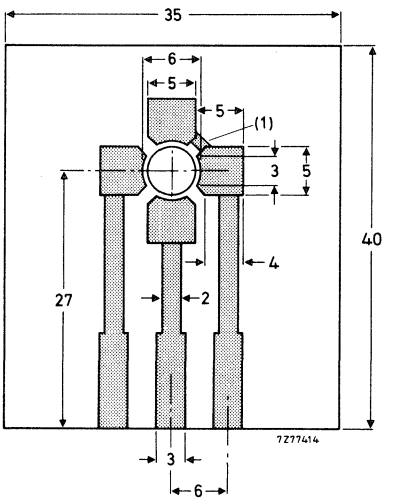
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335 K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents

$\pm V_{G1-S}$ = 7 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	<	25 nA
$\pm V_{G2-S}$ = 7 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	<	25 nA

Gate-source breakdown voltages

$\pm I_{G1-SS}$ = 10 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$	>	8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$	>	8 to 20 V

Gate-source cut-off voltages

I_D = 20 μA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V	$-V_{(P)G1-S}$	<	1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	20 mS
		typ.	25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2.0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1.2 dB

Data sheet	
status	Preliminary specification
date of issue	October 1990

BF988

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	225	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure	1	-	dB

Silicon n-channel dual gate MOS-FET BF988

MECHANICAL DATA

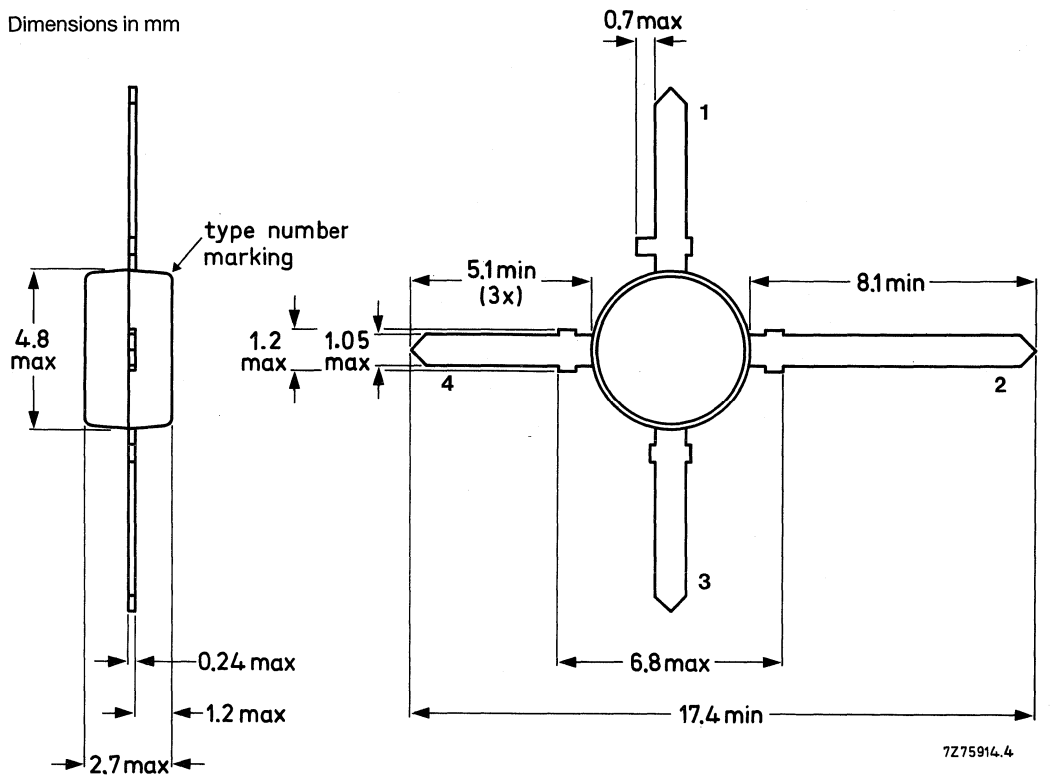


Fig.1 SOT103.

PIN CONFIGURATION

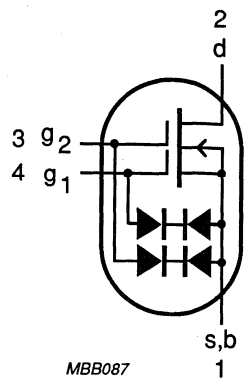


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF988

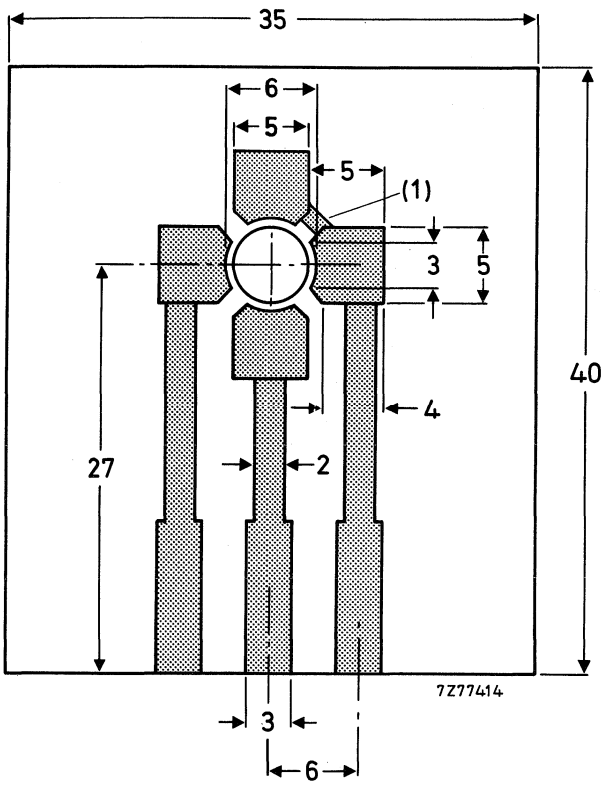
LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	$T_{amb} = 75$ °C	-	225	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air mounted on the printed circuit board (see Fig.3)	335	K/W



(1) Connection made by a strip or copper wire.

Tracks are fully tin-lead plated. Board in horizontal position for thermal resistance measurement.

Fig.3 Single-sided 35 μm copper-clad epoxy fibre-glass printed-circuit board, thickness 1.5 mm.

Silicon n-channel dual gate MOS-FET BF988

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS} = 0$	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS} = 0$	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS} = 0$	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current	V_{DS} = 8 V V_{G1-S} = 0 + V_{G2-S} = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF988

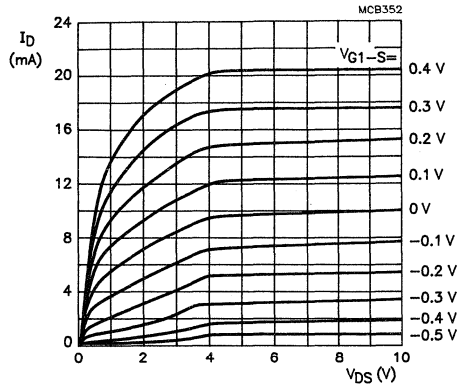


Fig.4 Output characteristics; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

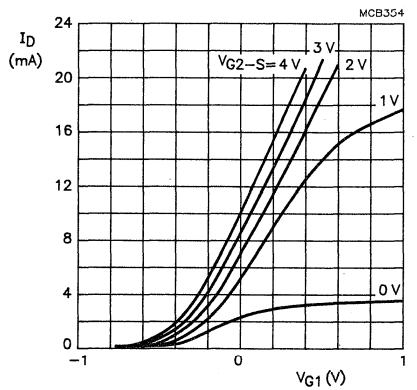


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

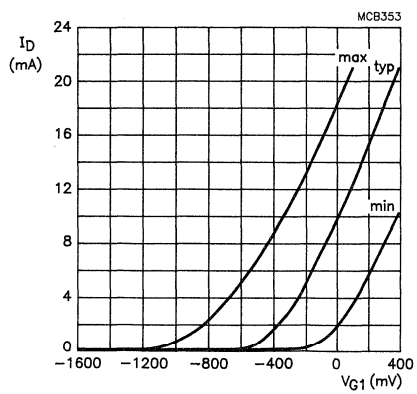


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

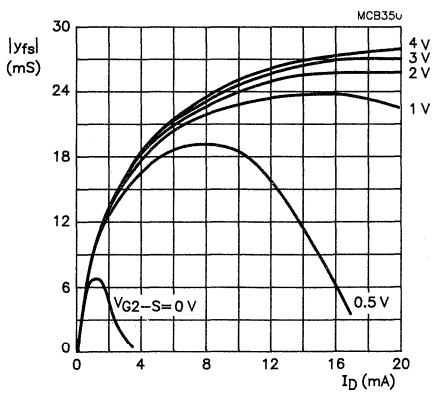


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF988

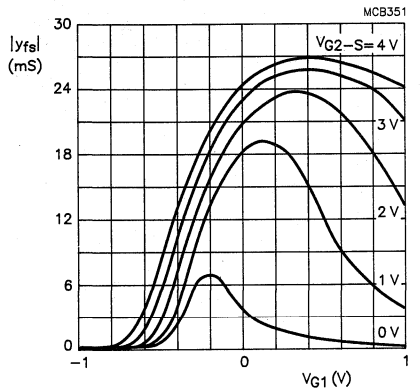


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

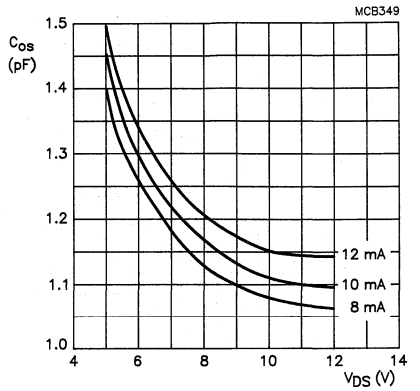


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

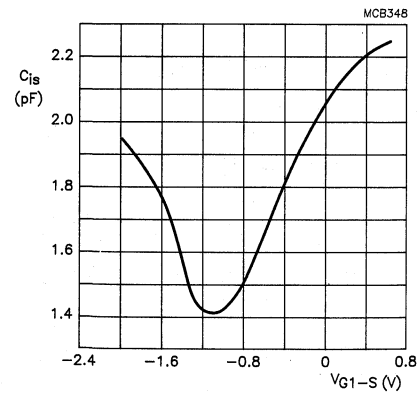


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

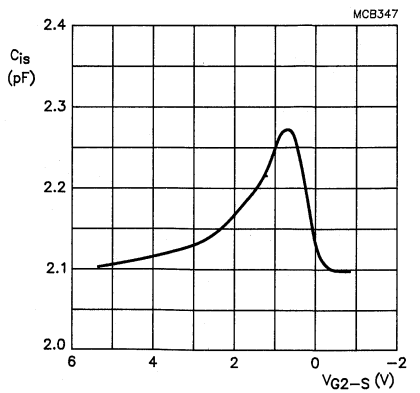


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF988

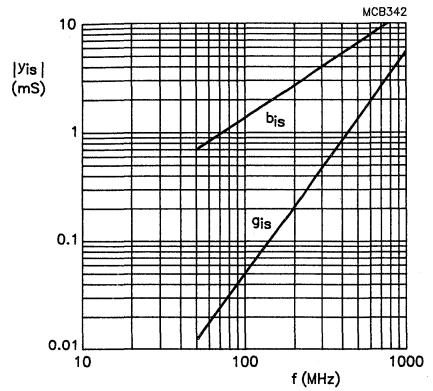


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

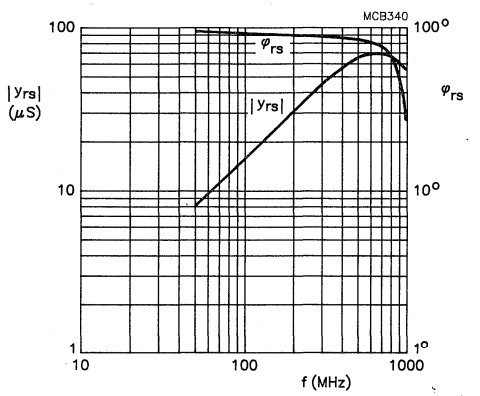


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

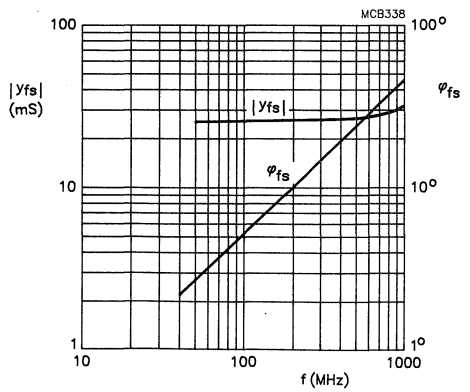


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

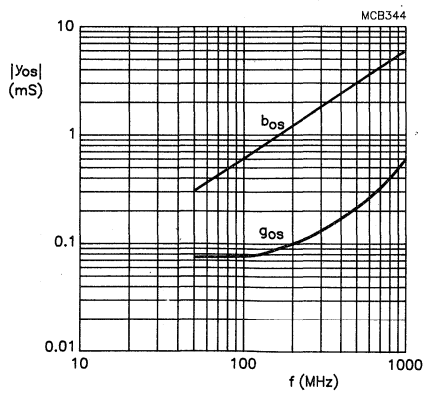


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF988

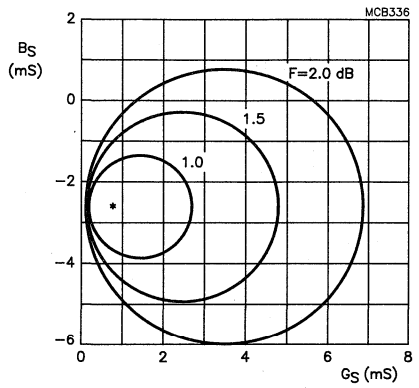


Fig.16 Circles of typical constant noise figures, 200 MHz; F_{opt} = 0.6 dB; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

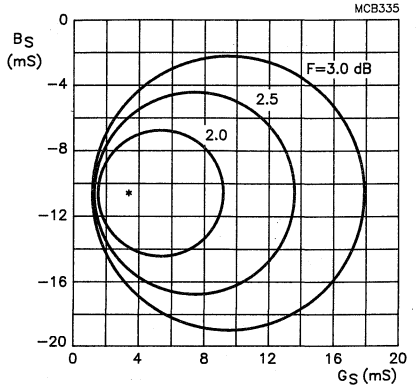
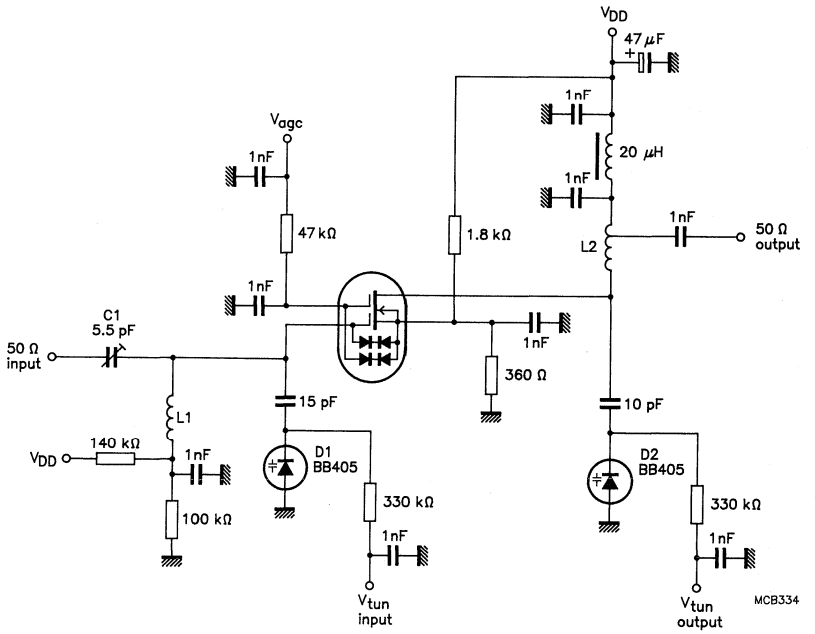


Fig.17 Circles of typical constant noise figures, 800 MHz; F_{opt} = 1.5 dB; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF988



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.18 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

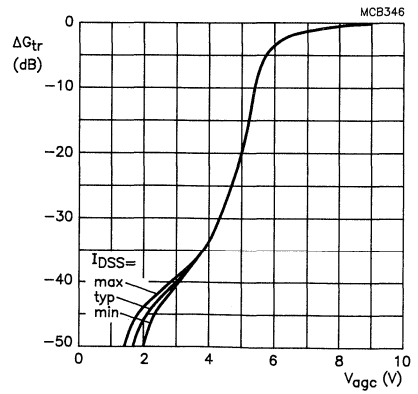
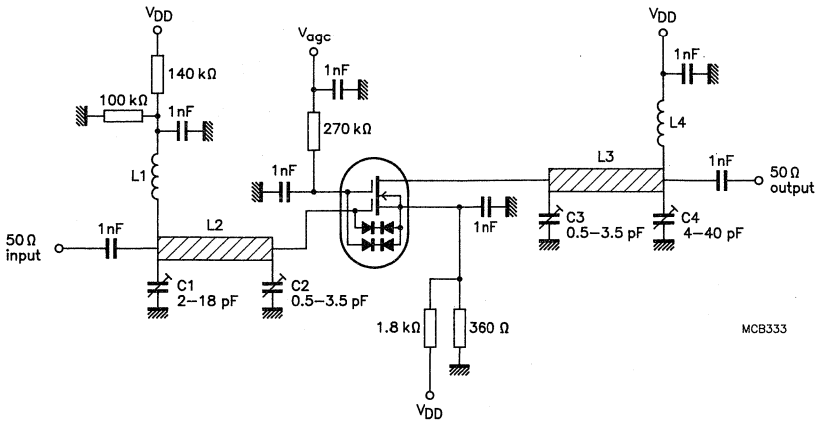


Fig.19 Automatic gain control characteristics measured in circuit of Fig.18; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF988



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.20 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

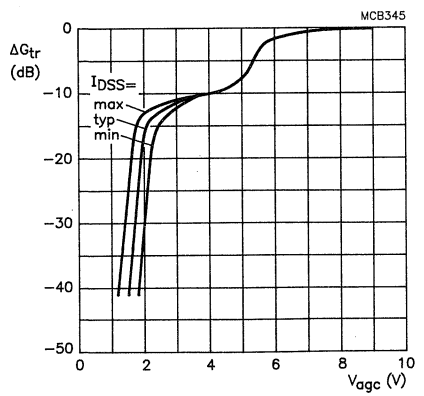


Fig.21 Automatic gain control characteristics measured in circuit of Fig.20; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in u.h.f. applications in television tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	12 mS
Input capacitance at gate 1; f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	1.8 pF
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 7 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.8 dB

MECHANICAL DATA

Fig.1 SOT143.

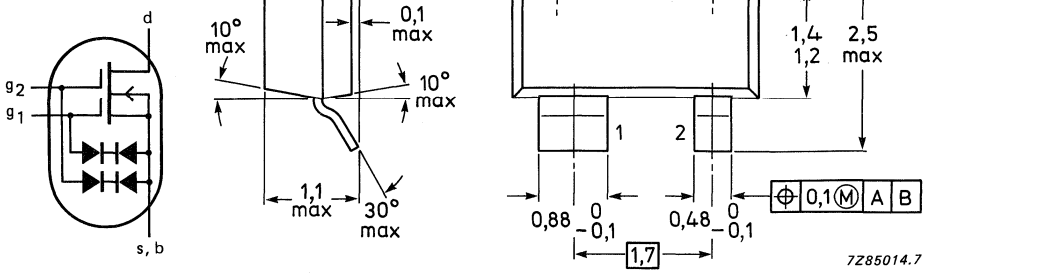
Dimensions in mm

Marking code:

BF989 = MAp

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

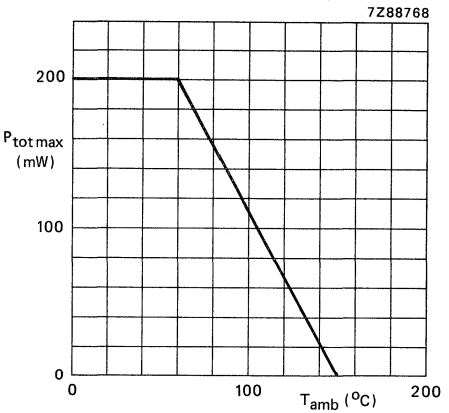


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50	nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50	nA
Drain current				
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		2 to 20	mA
Gate-source breakdown voltages				
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20	V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20	V
Gate-source cut-off voltages				
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.7	V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	9.5	mS
		typ.	12	mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	1.8	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.9	pF
Noise figure at G_S = 2 mS; $B_S = B_S$ opt				
f = 200 MHz	F	typ.	1.6	dB
f = 800 MHz	F	typ.	2.8	dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners with 12 V supply voltage and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ. max.	2.0 dB 3.0 dB

MECHANICAL DATA

Fig.1 SOT143.

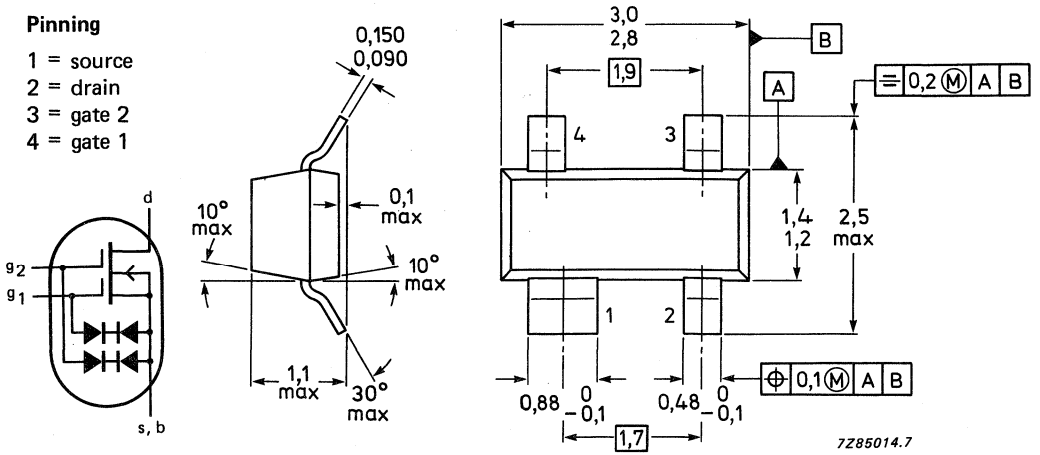
Marking code

BF990A = M87

Dimensions in mm

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18	V
Drain current	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

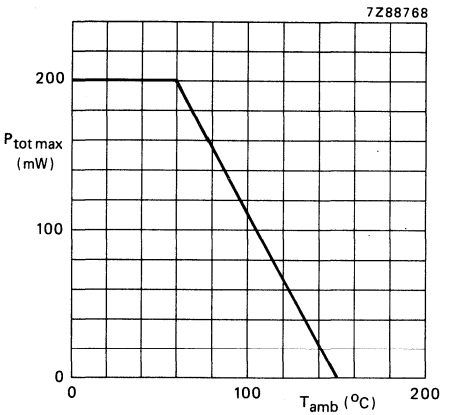


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1;			
$\pm V_{G1\text{-}S}$ = 7 V; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm I_{G1\text{-}SS}$	max.	25 nA
gate 2;			
$\pm V_{G2\text{-}S}$ = 7 V; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm I_{G2\text{-}SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1;			
$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G1\text{-}SS}$		8 to 20 V
gate 2;			
$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS}$ = 0	$\pm V_{(BR)G2\text{-}SS}$		8 to 20 V
Gate-source cut-off voltages			
gate 1;			
I_D = 20 μA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$-V_{(P)G1\text{-}S}$	max.	1.3 V
gate 2;			
I_D = 20 μA; V_{DS} = 10 V; $V_{G1\text{-}S}$ = 0	$-V_{(P)G2\text{-}S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	$C_{ig2\text{-}s}$	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ. max.	2.0 dB 3.0 dB

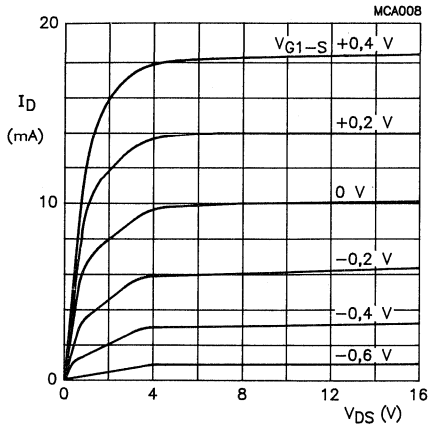


Fig.3 Output characteristics.
V_{G2-S} = 4 V; T_{amb} = 25 °C.

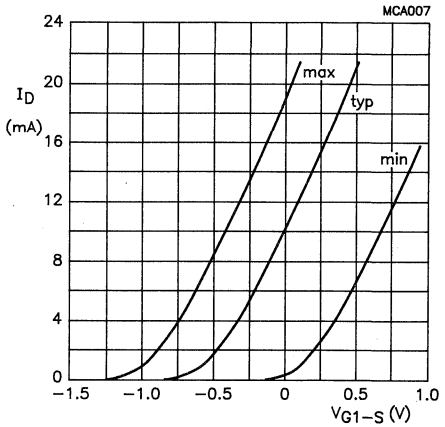


Fig.4 Transfer characteristics.
V_{DS} = 10 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for UHF applications, such as UHF television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	19 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; 3 $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.6 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 800 MHz	F	typ.	2.0 dB

MECHANICAL DATA

Fig.1 SOT143R.

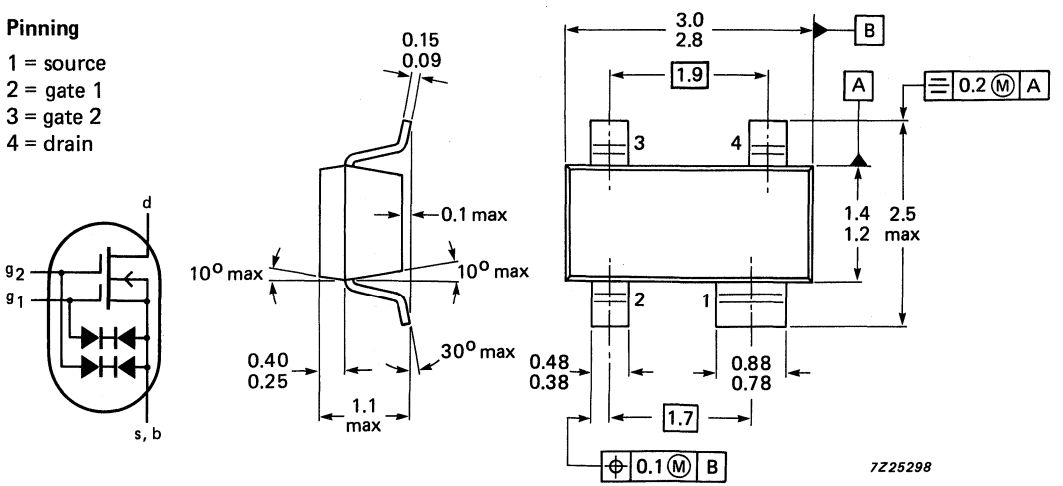
Marking code

BF990AR = M85

Dimensions in mm

Pinning

1 = source
2 = gate 1
3 = gate 2
4 = drain



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	18 V
Drain current	I_D	max.	30 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C*	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air*	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
gate 2; $\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	min.	8 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	min.	8 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	1.3 V
gate 2; I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	18 mS 19 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ. max.	2.6 pF 3.0 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.4 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.2 pF
Noise figure at f = 800 MHz; G_S = 5 mS; $B_S = B_S$ opt	F	typ.	2.0 dB

* Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners and f.m. tuners. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	14 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	2,1 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	20 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 200 MHz	F	typ.	0,7 dB

MECHANICAL DATA

Fig.1 SOT143.

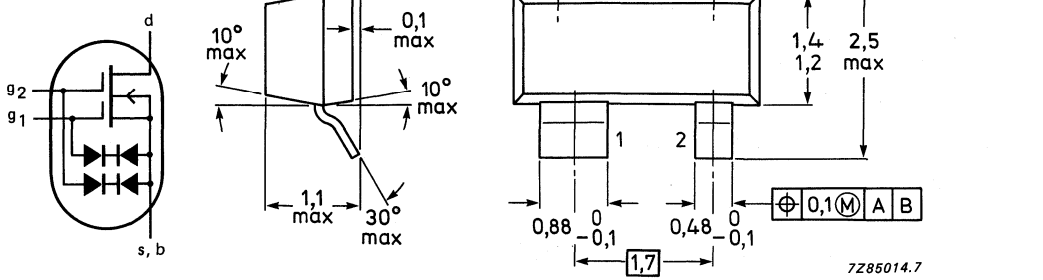
Dimensions in mm

Marking code

BF991 = M91

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	20 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to $T_{amb} = 60\ ^oC$ (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

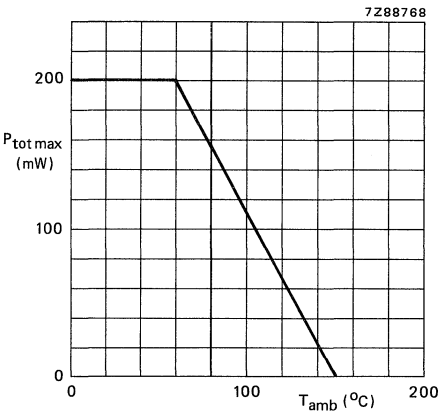


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	<	50 nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	<	50 nA
Drain current			
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		4 to 25 mA
Gate-source breakdown voltages			
± I_{G1-SS} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20 V
± I_{G2-SS} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	<	2,5 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	<	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	10 mS
		typ.	14 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1 pF
Noise figure			
f = 100 MHz; G_S = 1 mS; B_S = B_S opt	F	typ.	0,7 dB
		<	1,7 dB
f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1,0 dB
		<	2,0 dB
Transducer gain (note 1)			
f = 100 MHz; G_S = 1 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	29 dB
f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0,5 mS; B_L = B_L opt	G_{tr}	typ.	26 dB

Note

1. Crystal mounted in a SOT103 envelope.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

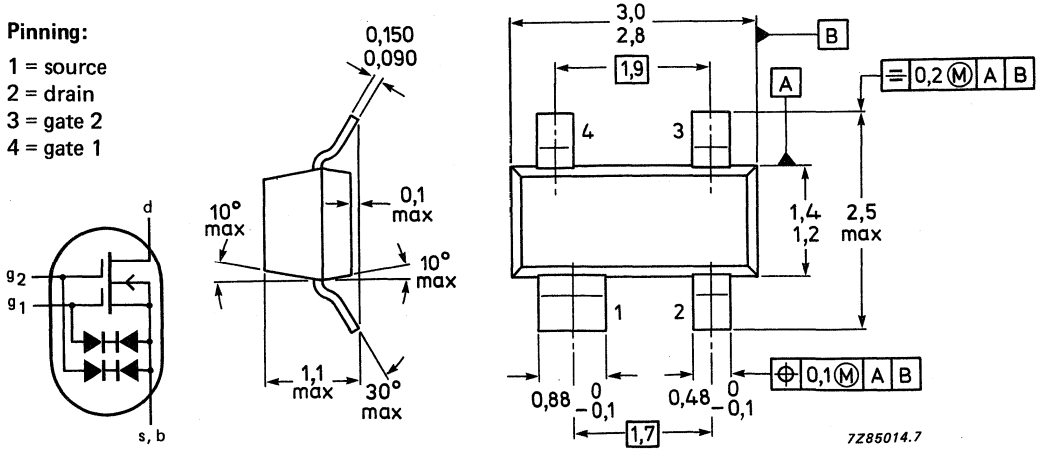
Dimensions in mm

Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

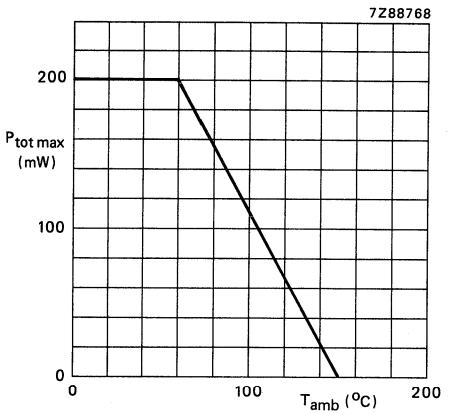


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. max.	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

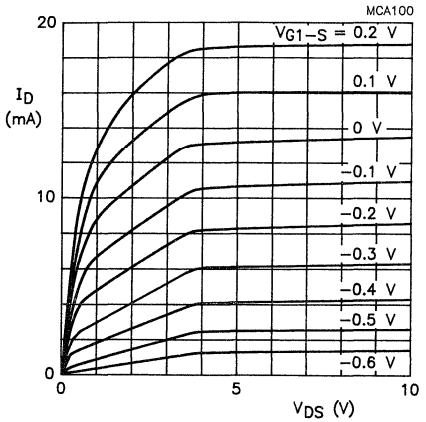


Fig.2 Output characteristics.

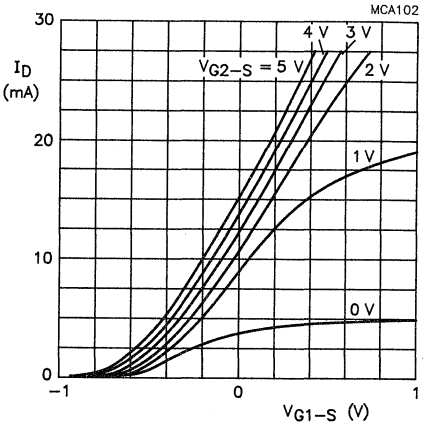


Fig.3 Transfer characteristics.

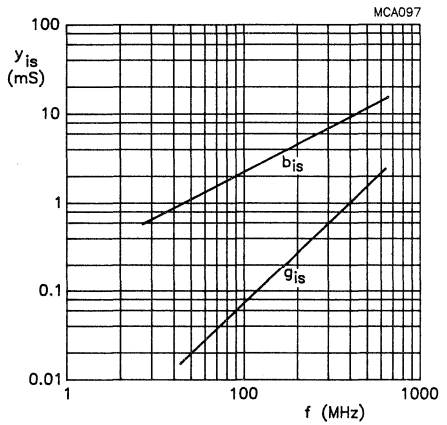


Fig.4 Input admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

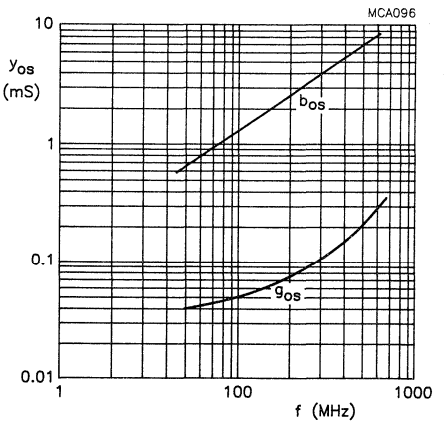


Fig.5 Output admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

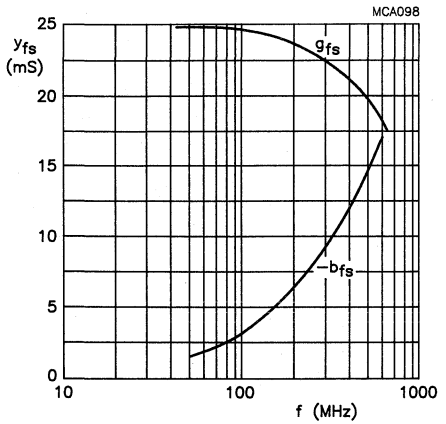


Fig.6 Transfer admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

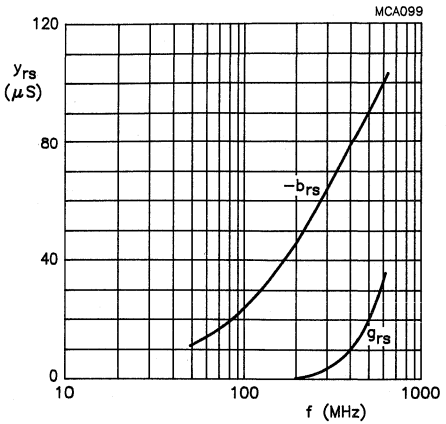


Fig.7 Feedback admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

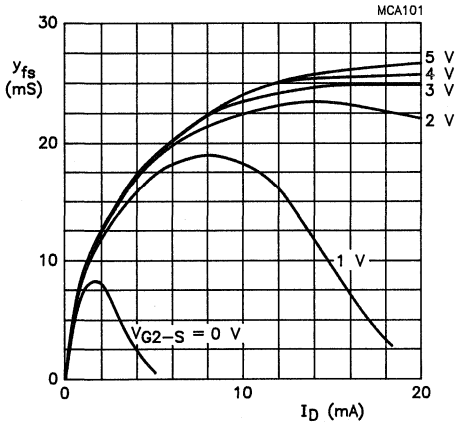


Fig.8 Transfer admittance as a function of drain current.

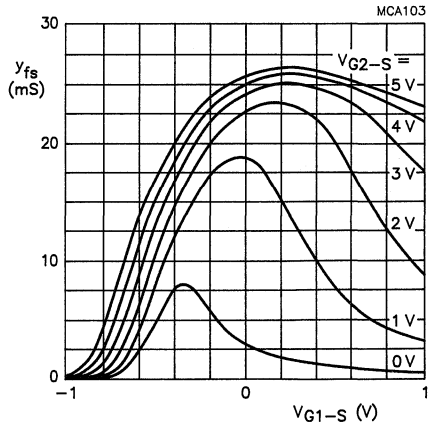


Fig.9 Transfer admittance as a function of gate 2 source voltage.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in VHF applications, such as VHF television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	250 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	25 mS
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Dimensions in mm

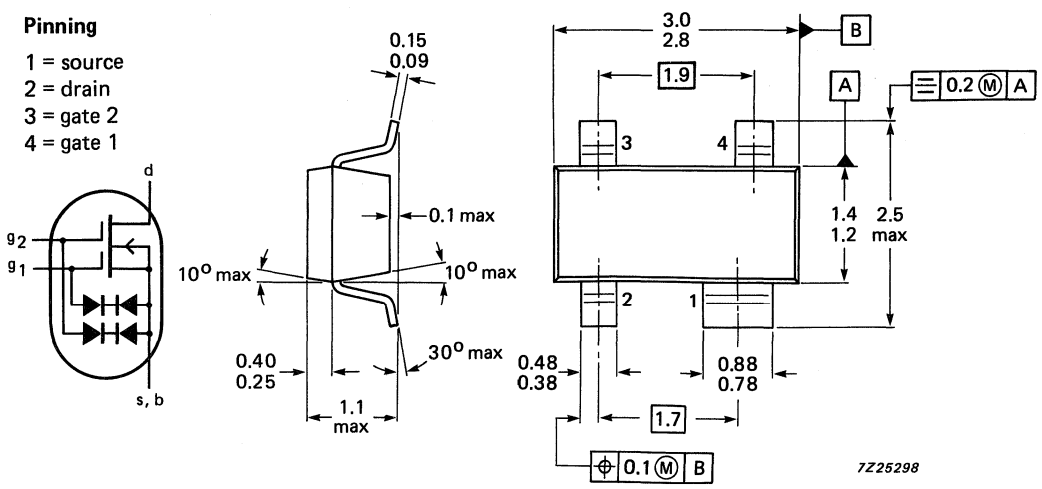
Fig.1 SOT143R.

Marking code

BF992R = M52

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	40 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	20 mS
		typ.	25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
		max.	40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for VHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.5 pF 3.0 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

Fig.1 SOT143.

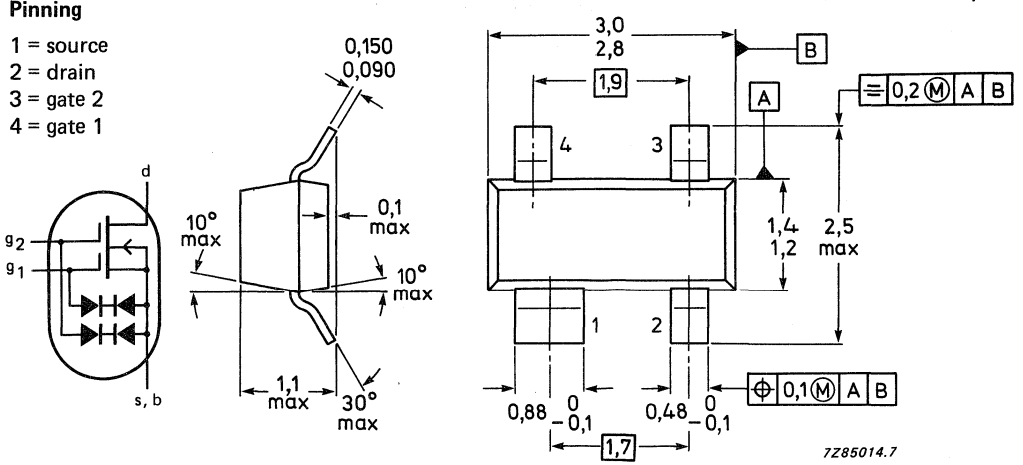
Dimensions in mm

Marking code

BF994S = MGp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	50 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

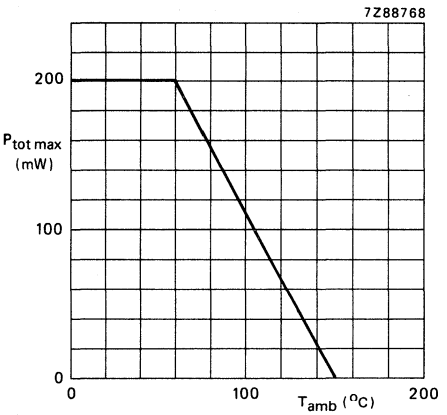


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	50 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-S} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-S} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
$V_{DS} = 15$ V; $V_{G1-S} = 0$; $V_{G2-S} = 4$ V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $+V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	max.	2.5 V
$I_D = 20\ \mu$A; $V_{DS} = 15$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 15$ V; $+V_{G2-S} = 4$ V; $T_{amb} = 25$ °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ. max.	2.5 pF 3.0 pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at $G_S = 2$ mS; $B_S = B_S$ opt; f = 200 MHz	F	typ.	1.0 dB
Power gain at $G_S = 2$ mS; $B_S = B_S$ opt $G_L = 0.5$ mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected and intended for UHF applications in television tuners.
The device is also suitable for use in professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates ans source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	18 mS
Input capacitance at gate 1 : f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ. max.	2.3 pF 2.6 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.8 dB

MECHANICAL DATA

Dimensions in mm

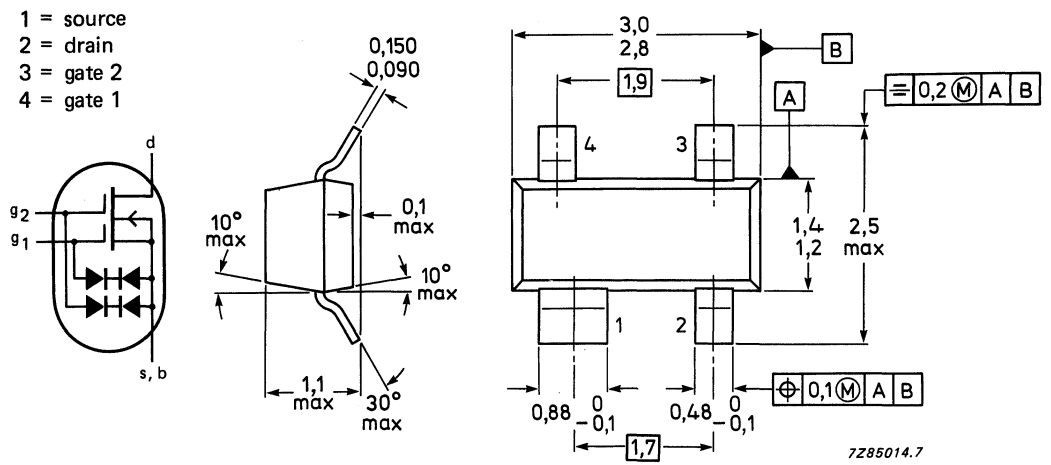
Fig.1 SOT143.

Marking code

BF996S = MHp

Pinning

1 = source
2 = drain
3 = gate 2
4 = gate 1



TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	30	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

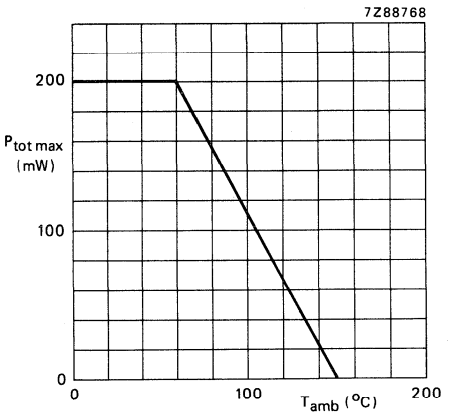


Fig. 2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
± V_{G1-S} = 5 V; V_{G2-S} = V_{DS} = 0	± I_{G1-SS}	max.	50 nA
± V_{G2-S} = 5 V; V_{G1-S} = V_{DS} = 0	± I_{G2-SS}	max.	50 nA
Gate-source breakdown voltages			
± I_{G1-S} = 10 mA; V_{G2-S} = V_{DS} = 0	± $V_{(BR)G1-SS}$		6 to 20 V
± I_{G2-S} = 10 mA; V_{G1-S} = V_{DS} = 0	± $V_{(BR)G2-SS}$		6 to 20 V
Drain current			
V_{DS} = 15 V; V_{G1-S} = 0; V_{G2-S} = 4 V	I_{DSS}		4 to 20 mA
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C.

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min.	15 mS
		typ.	18 mS
Input capacitance at gate 1: f = 1 MHz	C_{ig1-s}	typ.	2.3 pF
		max.	2.6 pF
Input capacitance at gate 2: f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0.8 pF
Noise figure			
f = 200 MHz; G_S = 2 mS; B_S = B_S opt	F	typ.	1.0 dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt		typ.	1.8 dB
Power gain			
f = 200 MHz; G_S = 2 mS; B_S = B_S opt; G_L = 0.5 mS; B_L = B_L opt	G_p	typ.	25 dB
f = 800 MHz; G_S = 3.3 mS; B_S = B_S opt; G_L = 1.0 mS; B_L = B_L opt		typ.	18 dB

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for u.h.f. and v.h.f. applications, such as u.h.f./v.h.f. television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source and has an integrated drain resistance to suppress oscillation in the frequency range higher than 1 GHz.

This device is especially intended for use in pre-amplifiers in CATV tuners with a large tuning range up to 500 MHz.

QUICK REFERENCE DATA

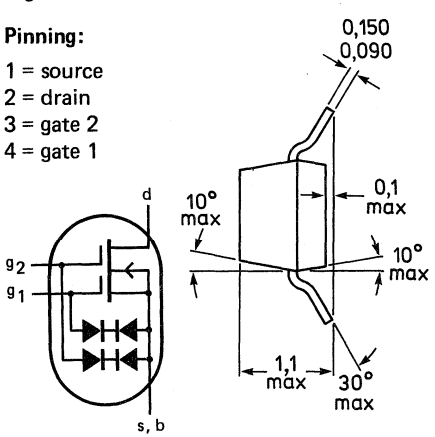
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	30 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	18 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	2.5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF
Noise figure at G_S = 2 mS; B_S = B_S opt I_D = 10 mA; V_{DS} = 15 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.0 dB

MECHANICAL DATA

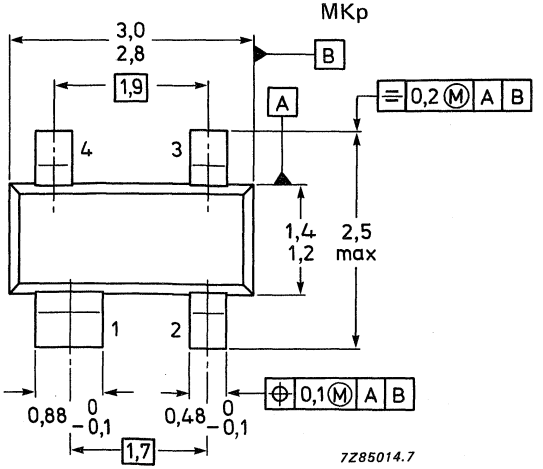
Fig.1 SOT143.

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1



Dimensions in mm



TOP VIEW

Marking code:

MKp

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	30 mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460 K/W

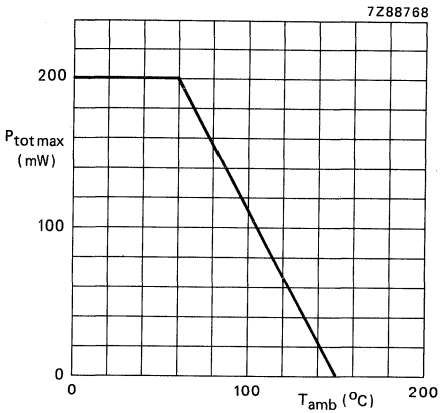


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
gate 1; $\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	max.	50 nA
gate 2; $\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	max.	50 nA
Gate-source breakdown voltages			
gate 1; $\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
gate 2; $\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Gate-source cut-off voltages			
gate 1; I_D = 20 μA; V_{DS} = 15 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	max.	2.5 V
gate 2; I_D = 20 μA; V_{DS} = 15 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	max.	2.0 V
Drain-source cut-off voltage V_{DS} = 15 V; V_{G2-S} = 4 V; V_{G1-S} = 0	I_{DSS}		2 to 20 mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 10 mA; V_{DS} = 15 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	15 mS 18 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2.5 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.2 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1.0 pF
Noise figure at f = 200 MHz; G_S = 2 mS; $B_S = B_S$ opt	F	typ.	1.0 dB
Power gain at G_S = 2 mS; $B_S = B_S$ opt G_L = 0.5 mS; $B_L = B_L$ opt; f = 200 MHz	G_p	typ.	25 dB

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

BF998

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

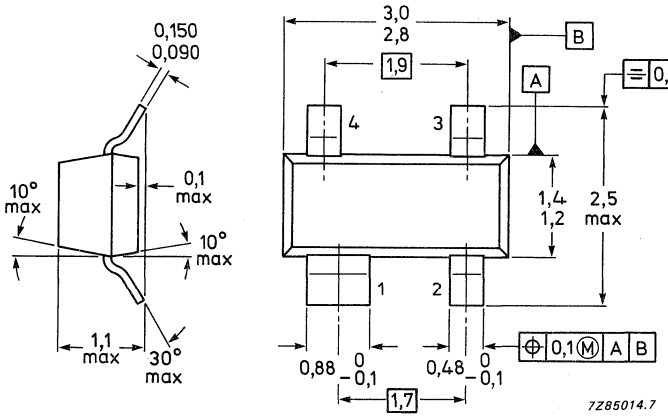
Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp



TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

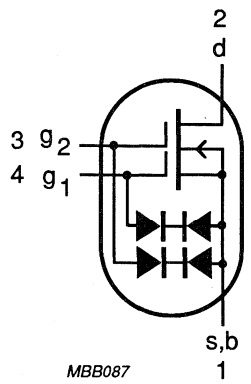


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF998

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C (note 1)	-	200	mW
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 2)	-	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	460	K/W
$R_{th\ j-a}$	from junction to ambient in free air (note 2)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Device mounted on printed circuit board.

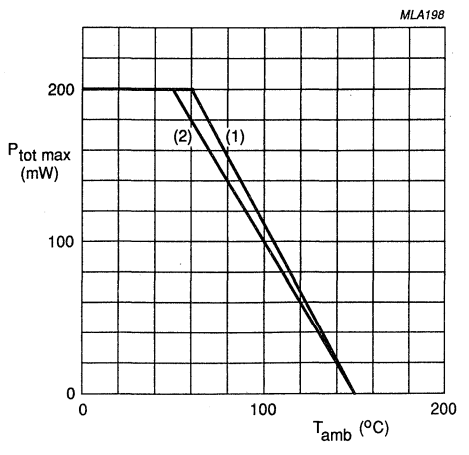


Fig.3 Power derating curve;
(1) ceramic substrate;
(2) printed-circuit board.

Silicon n-channel dual gate MOS-FET BF998

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS}$ = 0	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS}$ = 0	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS}$ = 0	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS}$ = 0	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current (measured under pulse condition)	V_{DS} = 8 V V_{G1-S} = 0 $+V_{G2-S}$ = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Y_{fs}\|$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF998

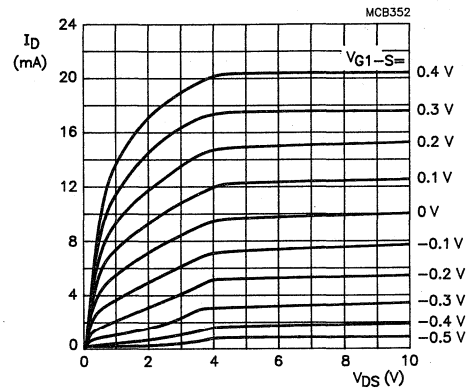


Fig.4 Output characteristics; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

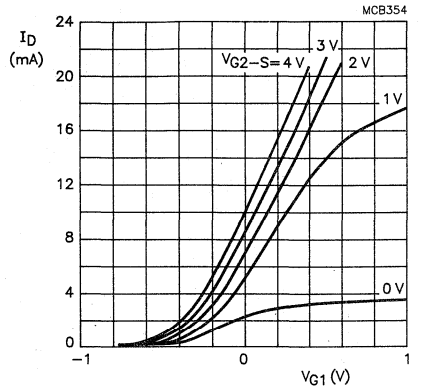


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

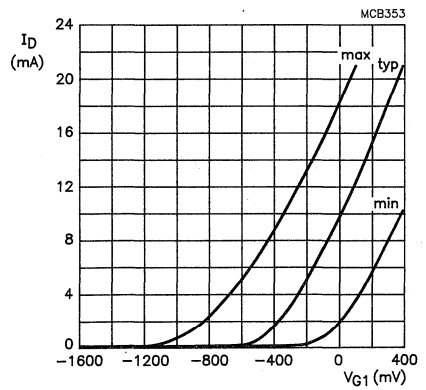


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

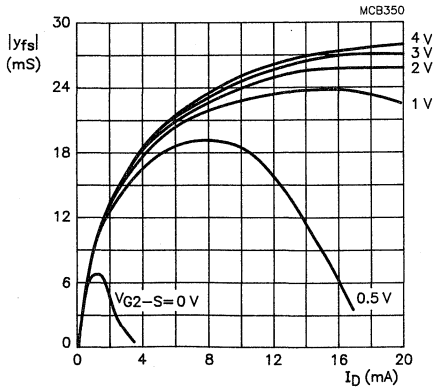


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF998

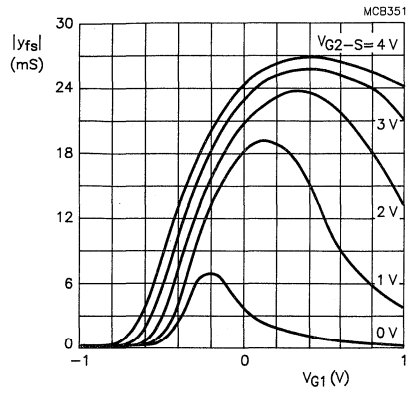


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

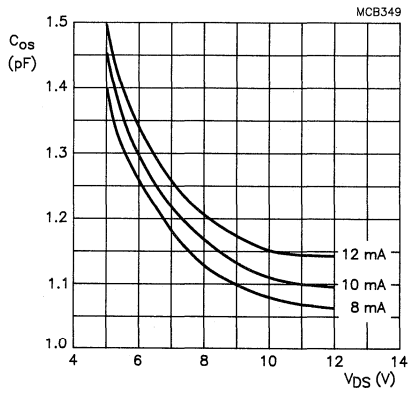


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

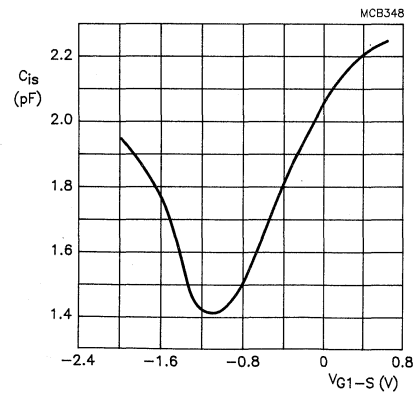


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

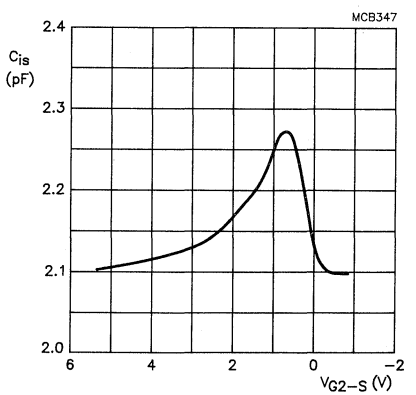


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF998

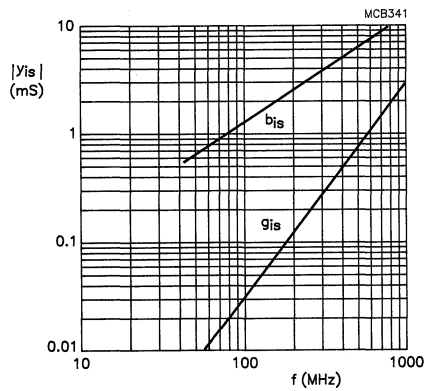


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

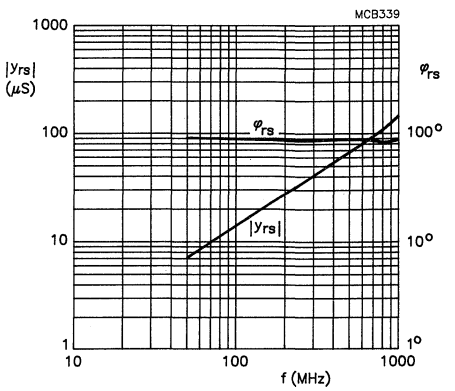


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

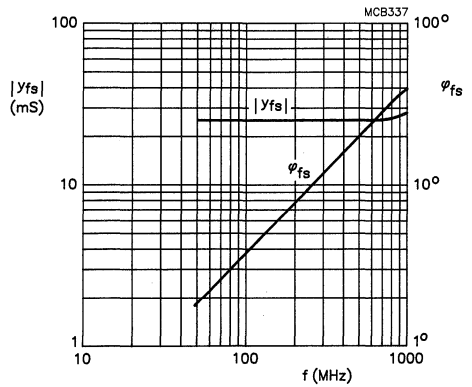


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

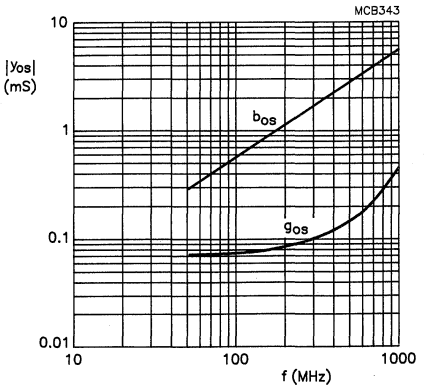
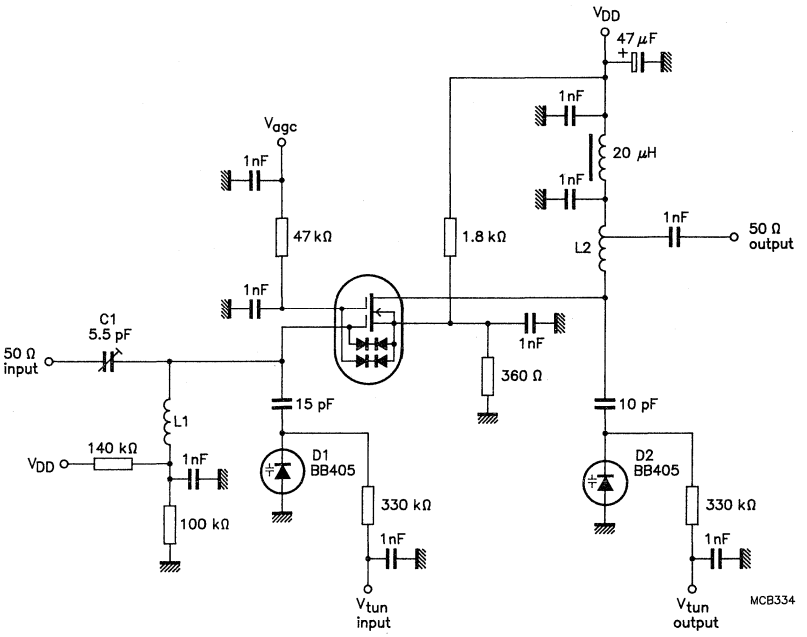


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

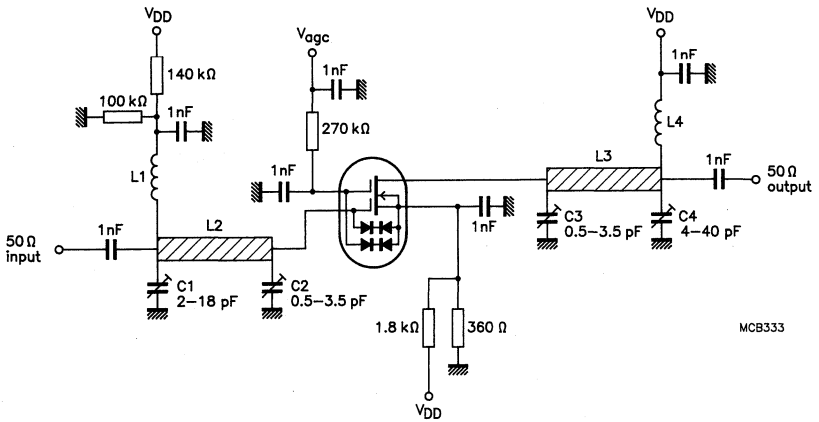
Silicon n-channel dual gate MOS-FET BF998



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

Silicon n-channel dual gate MOS-FET BF998



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

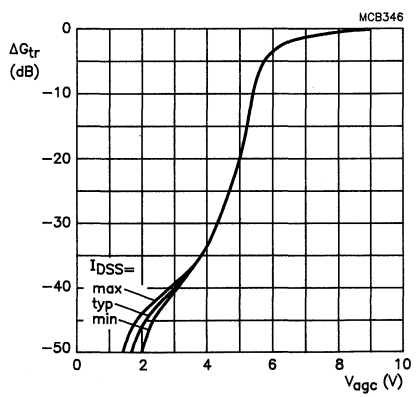


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

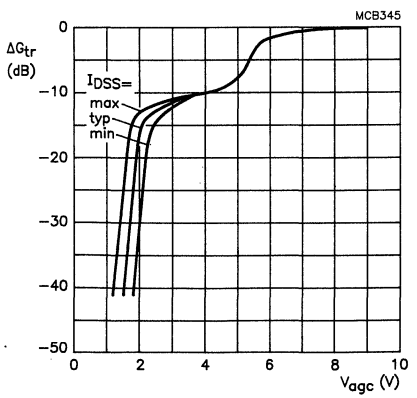


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

BF998R

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143R microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as UHF television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	pF
F	noise figure at 800 MHz	1	-	dB

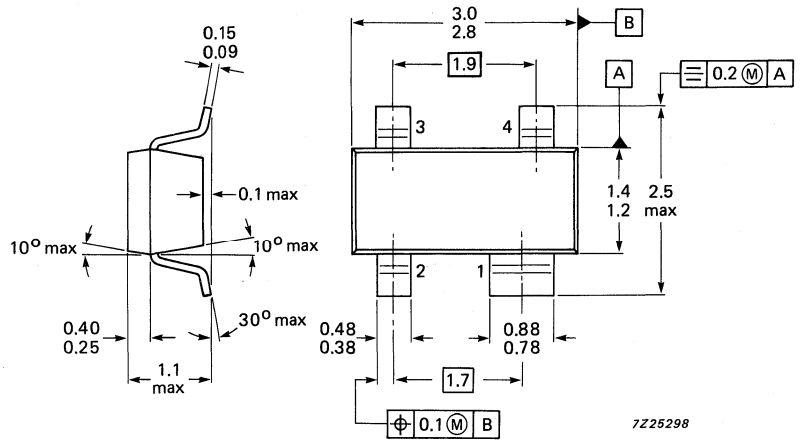
Silicon n-channel dual gate MOS-FET BF998R

MECHANICAL DATA

Dimensions in mm

Marking code

BF998R = MO$\overline{p}$



See also soldering recommendations.

Fig.1 SOT143R.

PIN CONFIGURATION

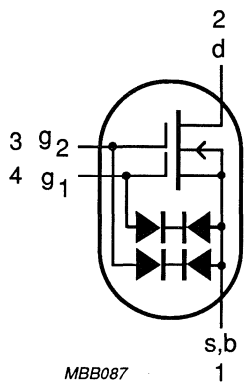


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Silicon n-channel dual gate MOS-FET BF998R

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 1)	-	200	mW
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.

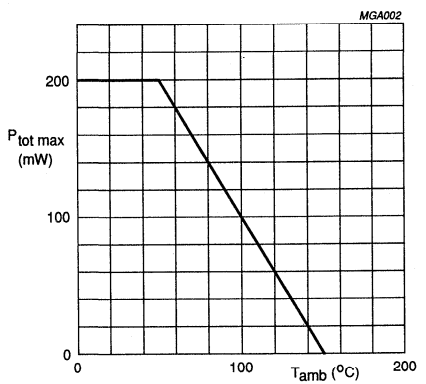


Fig.3 Power derating curve.

Silicon n-channel dual gate MOS-FET BF998R

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS} = O$	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS} = 0$	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS} = 0$	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current	V_{DS} = 8 V V_{G1-S} = 0 + V_{G2-S} = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

Silicon n-channel dual gate MOS-FET BF998R

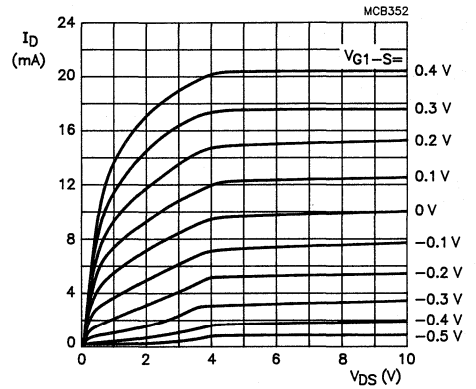


Fig.4 Output characteristics; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

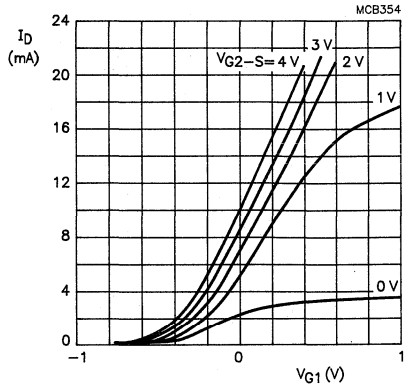


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

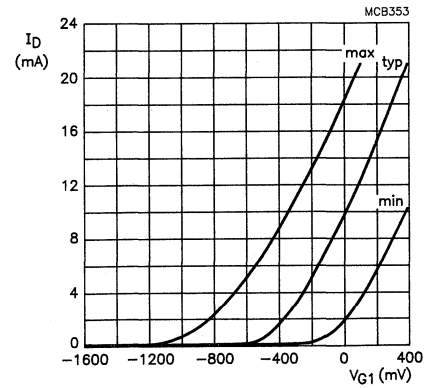


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

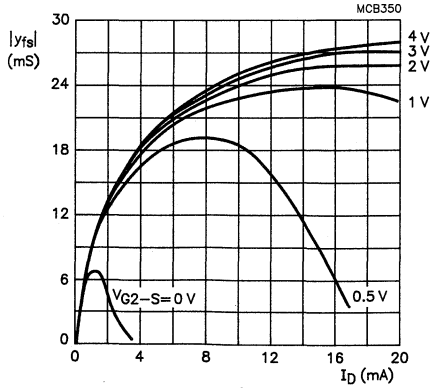


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

Silicon n-channel dual gate MOS-FET BF998R

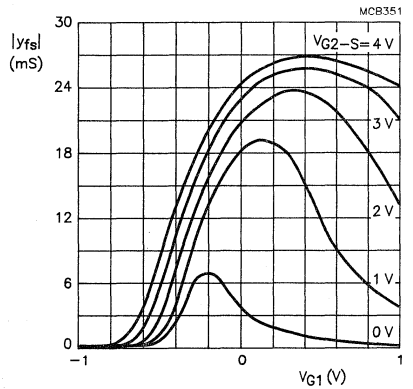


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

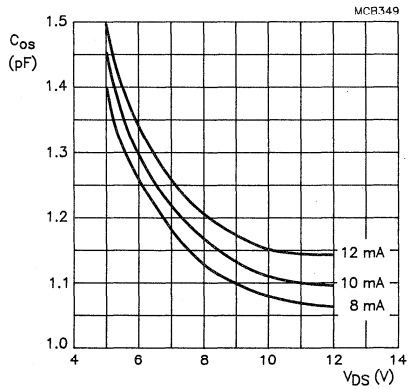


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

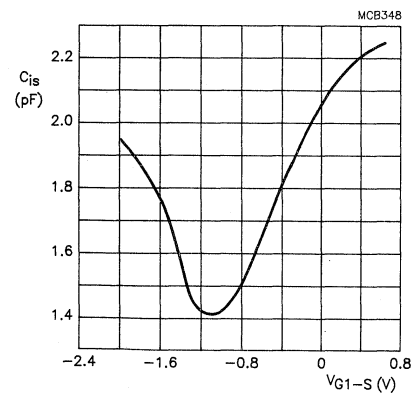


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

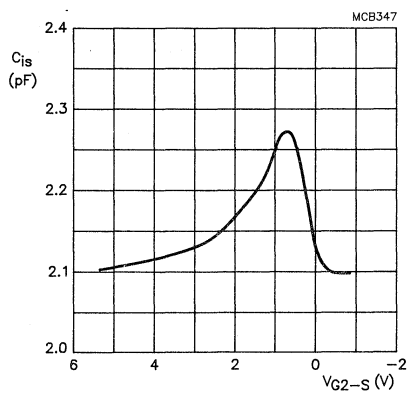


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

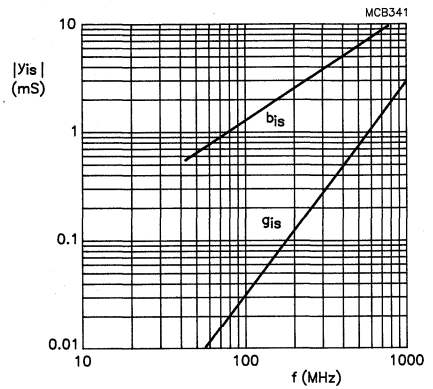


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

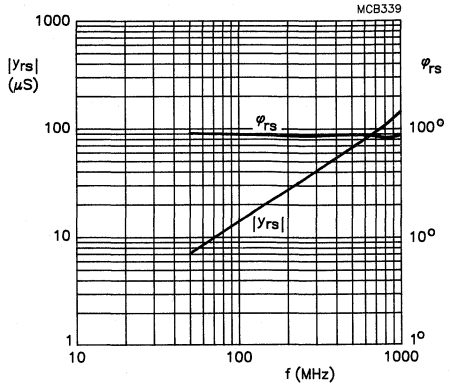


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

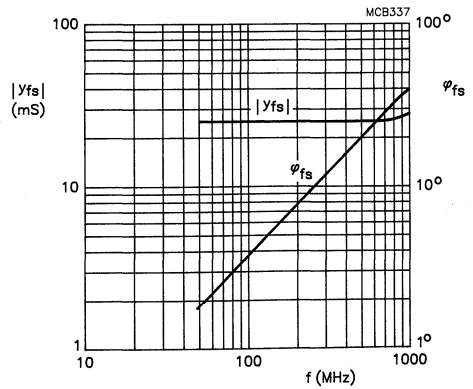


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

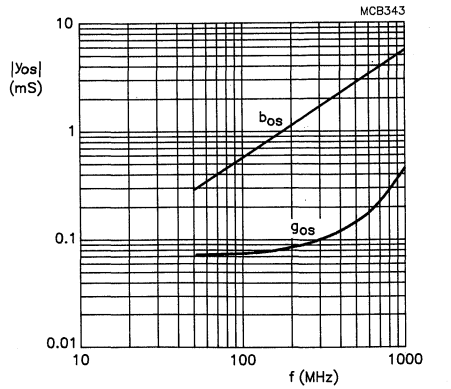
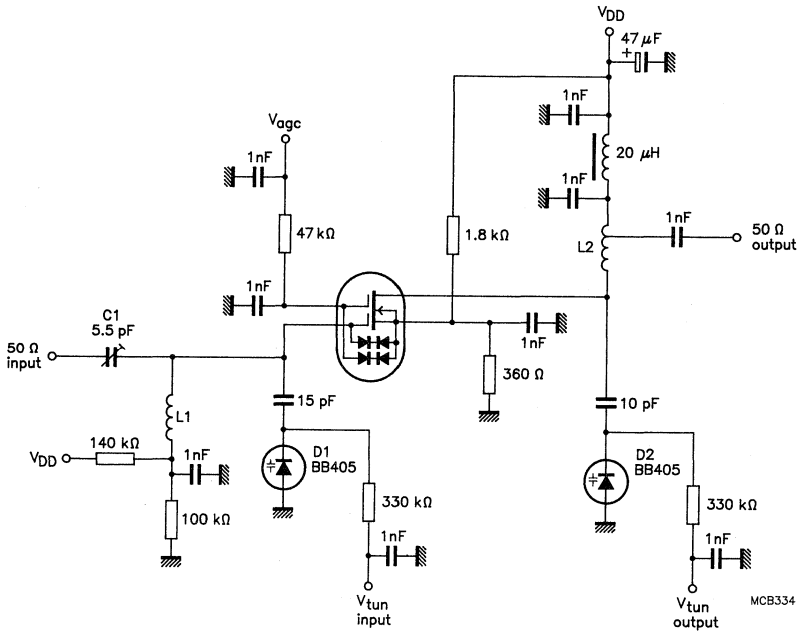


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

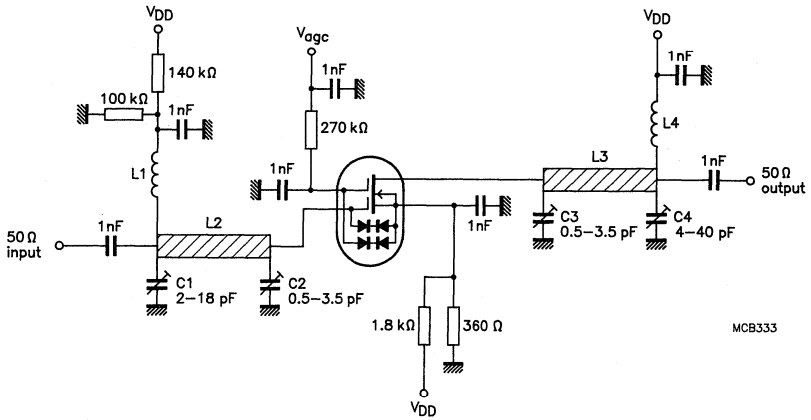


L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.

L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.

Silicon n-channel dual gate MOS-FET BF998R



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.

L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.

L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

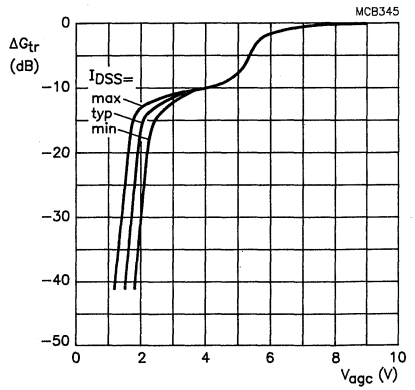


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

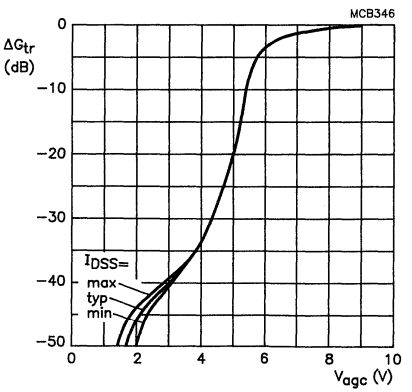


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a metal TO-72 envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:
a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
b) excellent signal handling capability over the entire gain control range.
c) low noise figure combined with high gain.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	50 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	175 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	15 mS
Input capacitance at gate 1; f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{ig1-s}	typ.	5.5 pF
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30 fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V G_S = 1.2 mA; $-B_S$ = 5.7 mS; f = 200 MHz	F	typ.	2.3 dB

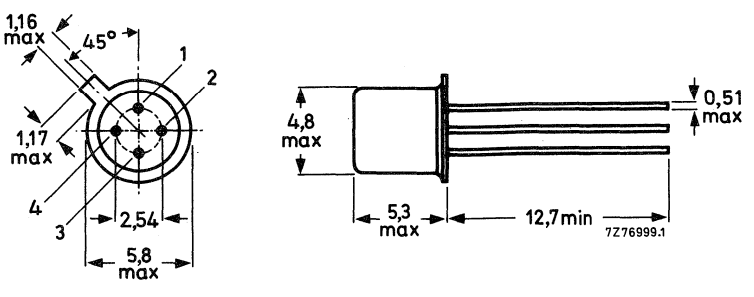
MECHANICAL DATA

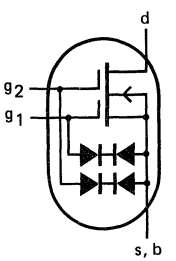
Dimensions in mm

Fig.1 TO-72.

Source and substrate connected to the case.

Pinning:
1 = drain
2 = gate 2
3 = gate 1
4 = source





Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20 V
Drain current (DC or average)	I_D	max.	50 mA
Drain current (peak value)	I_{DM}	max.	100 mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10 mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}	−65 to +	175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W

STATIC CHARACTERISTICS

T_j = 25 °C

Gate cut-off currents			
$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0	$\pm I_{G1-SS}$	max.	10 nA
$\pm V_{G1-S}$ = 5 V; V_{G2-S} = V_{DS} = 0; T_j = 150 °C	$\pm I_{G1-SS}$	max.	10 μA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0	$\pm I_{G2-SS}$	max.	10 nA
$\pm V_{G2-S}$ = 5 V; V_{G1-S} = V_{DS} = 0; T_j = 150 °C	$\pm I_{G2-SS}$	max.	10 μA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 0.1 mA; V_{G2-S} = V_{DS} = 0	$\pm V_{(BR)G1-SS}$		6 to 20 V
$\pm I_{G2-SS}$ = 0.1 mA; V_{G1-S} = V_{DS} = 0	$\pm V_{(BR)G2-SS}$		6 to 20 V
Drain current			
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}		20 to 55 mA
Gate 1-source voltage			
I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{G1-SS}$		0.6 to 2.1 V
Gate-source cut-off voltages			
I_D = 10 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		1.5 to 3.8 V
I_D = 10 μA; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$		1.5 to 3.4 V

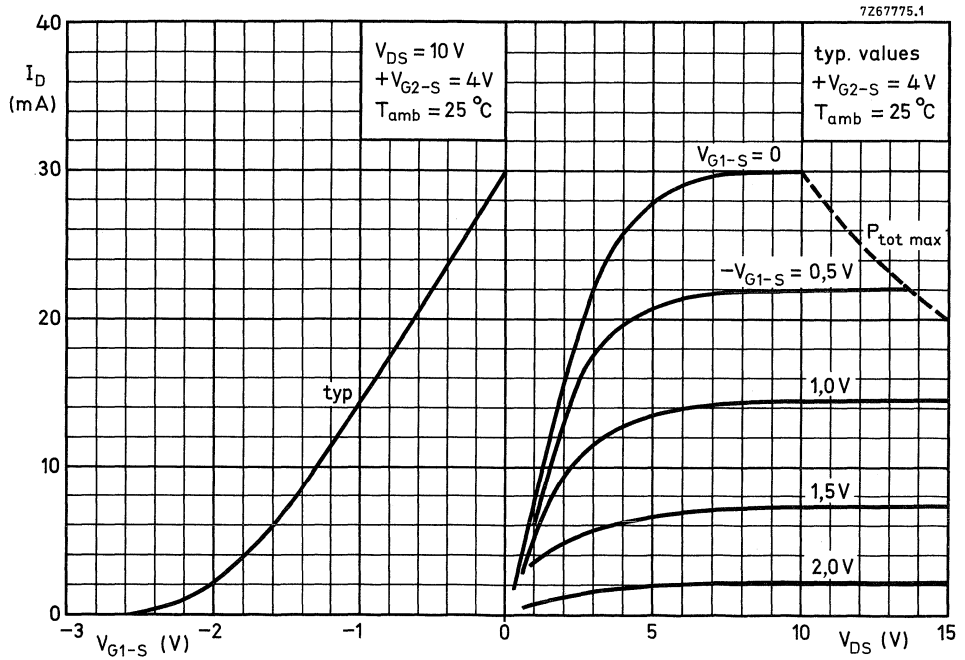
DYNAMIC CHARACTERISTICS

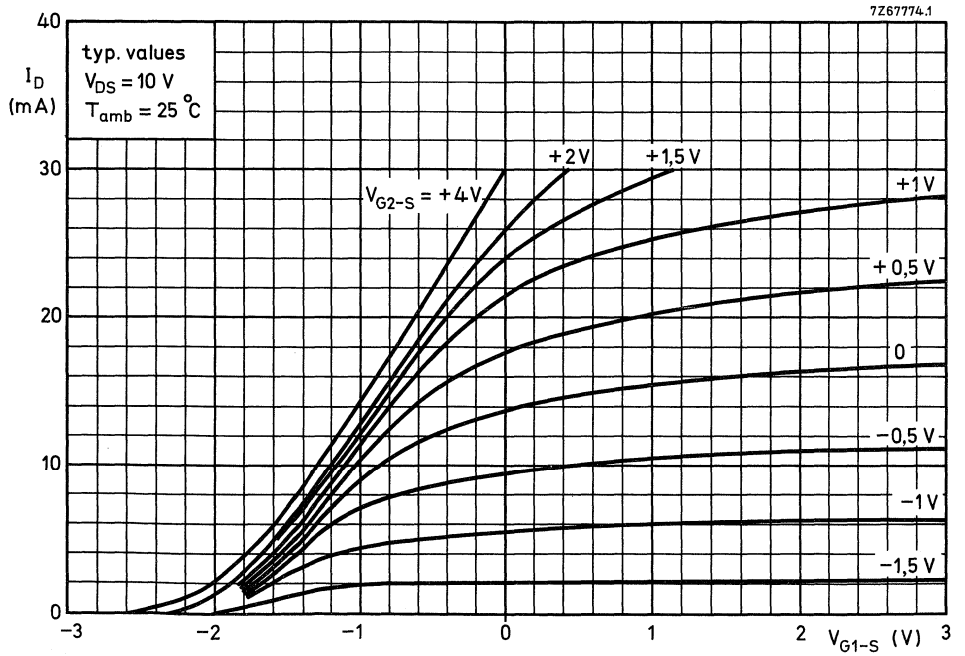
Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

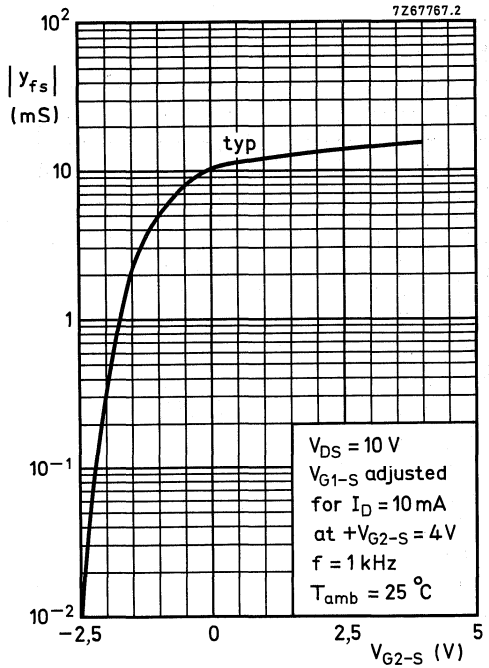
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	12 mS 15 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	5.5 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3.5 pF
Noise figure at optimum source admittance			
G_S = 0.95 mS; $-B_S$ = 5.0 mS; f = 100 MHz	F	typ.	1.9 dB
G_S = 1.20 mS; $-B_S$ = 5.7 mS; f = 200 MHz	F	typ. max.	2.3 dB 3.0 dB
Cross modulation at f = 200 MHz Wanted signal at f_o = 197.5 MHz Unwanted signal at f_{int} = 202.5 MHz			
Interference voltage at g_1 for K = 1%	V_{int}	typ.	100 mV (note 1)

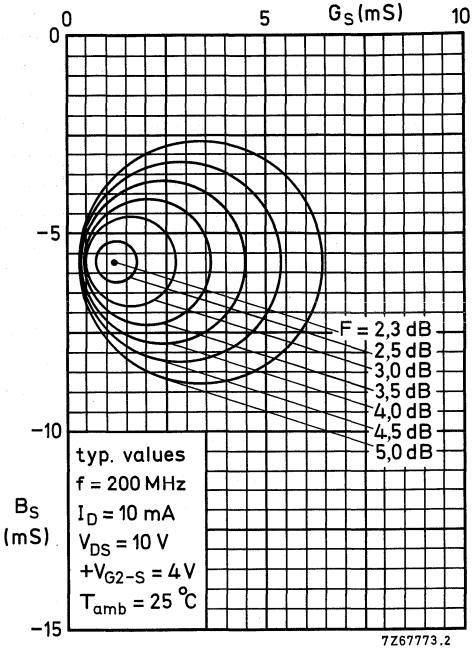
Note

1. Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0.8% modulation depth on the wanted signal (a.m. definition).


7Z67775.1
I_D (mA)
V_{DS} = 10 V
+V_{G2-S} = 4 V
T_{amb} = 25 °C
typ. values
+V_{G2-S} = 4 V
T_{amb} = 25 °C
V_{G1-S} = 0
$P_{tot\ max}$
−V_{G1-S} = 0,5 V
1,0 V
1,5 V
2,0 V
typ
V_{G1-S} (V)
V_{DS} (V)


7Z67774.1
I_D (mA)
typ. values
V_{DS} = 10 V
T_{amb} = 25 °C
V_{G2-S} = +4 V
+2 V
+1,5 V
+1 V
+0,5 V
0
−0,5 V
−1 V
−1,5 V
V_{G1-S} (V)





circles of constant noise figure

DEVICE DATA
VERTICAL D-MOS-FETs

Philips Components

Data sheet	
status	Preliminary specification
date of issue	February 1991

BS107

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PIN CONFIGURATION

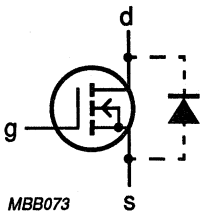


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

N-channel enhancement mode vertical D-MOS transistor

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	150	mA
I_{DM}	drain current	peak	-	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

N-channel enhancement mode vertical D-MOS transistor

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	4	20	ns

N-channel enhancement mode vertical D-MOS transistor

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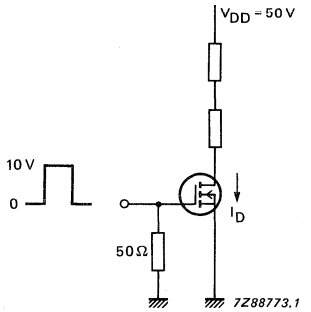

Fig.2 Switching time test circuit.

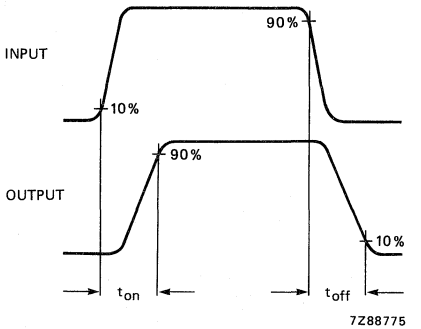

Fig.3 Input and output waveforms.

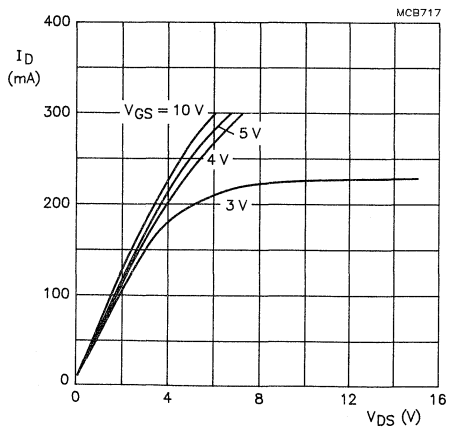

Fig.4 Typical output characteristics; T_j = 25 °C.

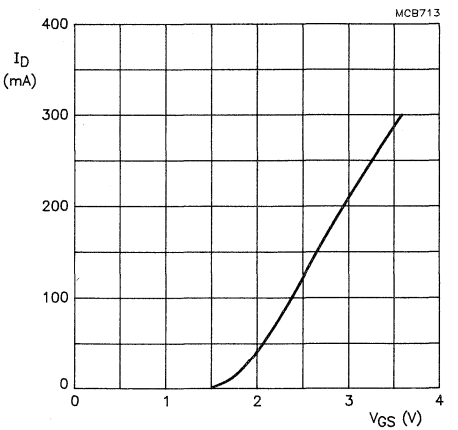

Fig.5 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

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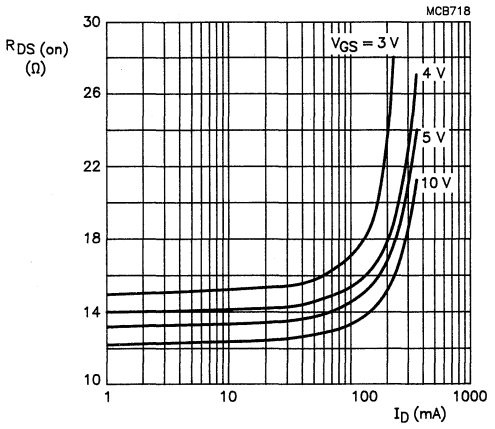


Fig.6 Typical on-resistance as a function of drain current; T_j = 25 °C.

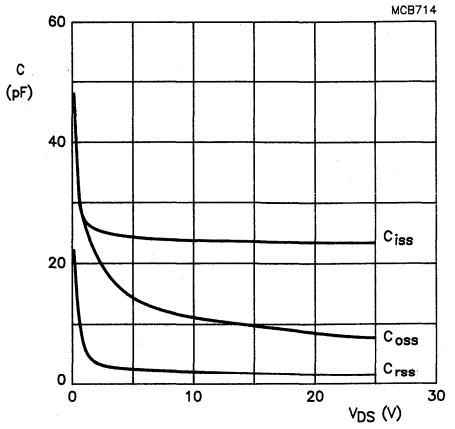


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

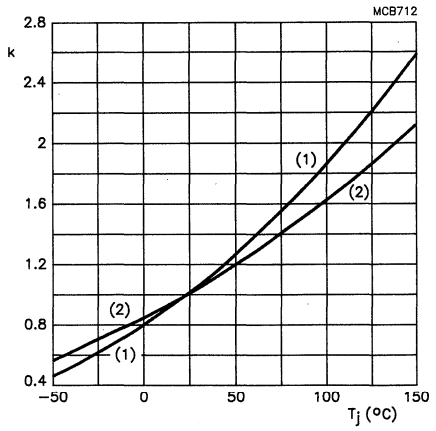


Fig.8 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}; \text{ typical } R_{DS(on)}$$

at 150 mA/10 V;
(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

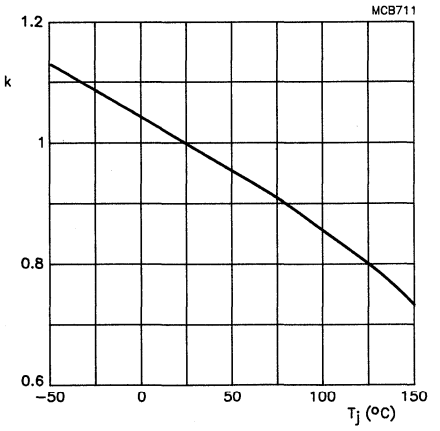


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}; \text{ typical } V_{GS(th)}$$

at 1 mA.

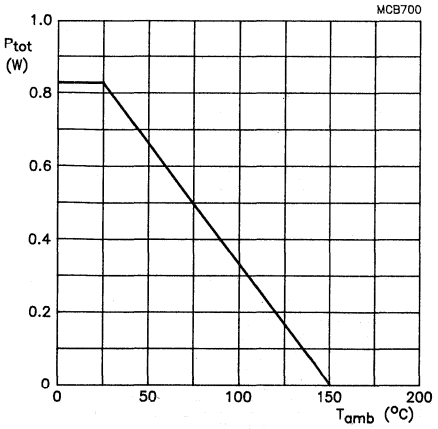


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BS107

PACKAGE OUTLINE

Dimensions in mm

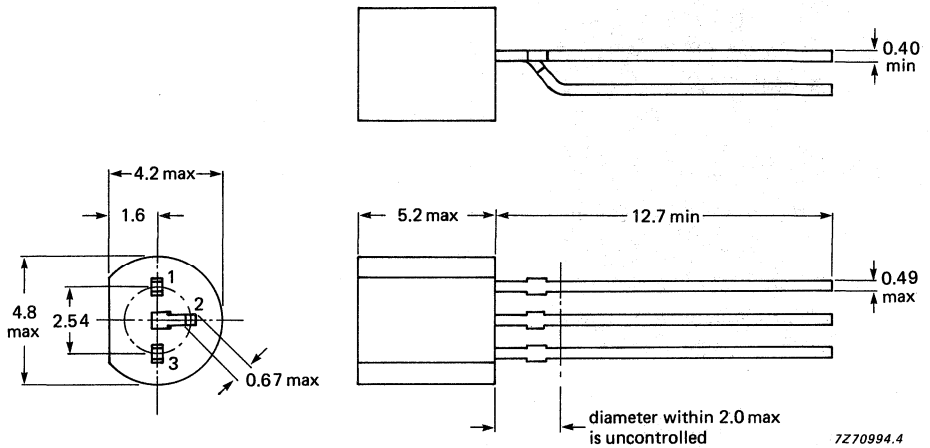


Fig.11 TO-92 variant.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	200 mS 350 mS

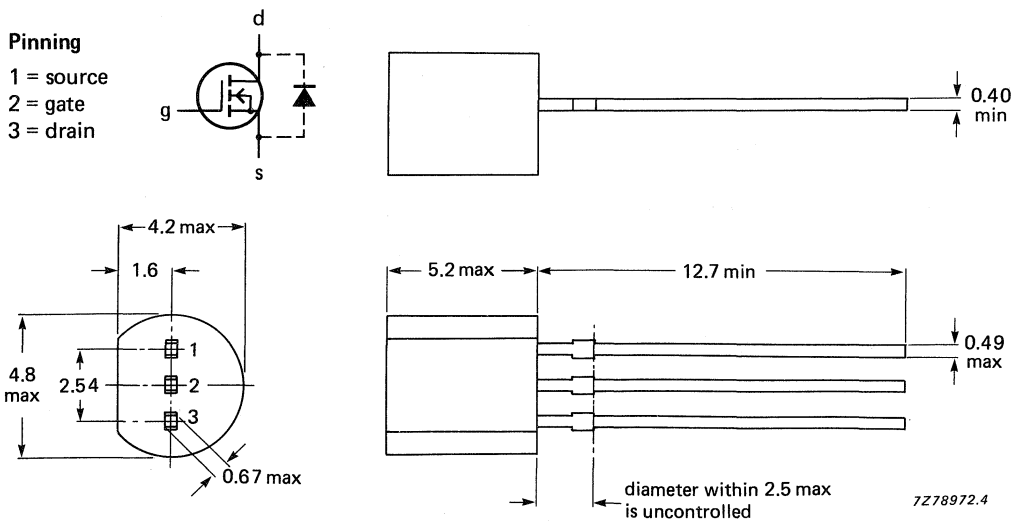
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinnings are available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6 W
Storage temperature	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 130 V; V_{GS} = 0	I_{DSS}	max.	30 nA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.0 V 3.0 V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.4 Ω
I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.2 Ω 6.0 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

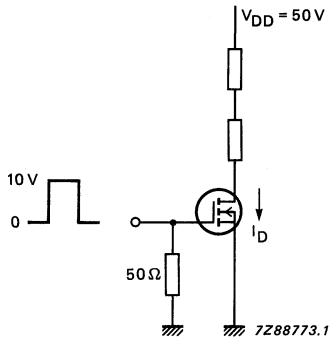


Fig.2 Switching times test circuit.

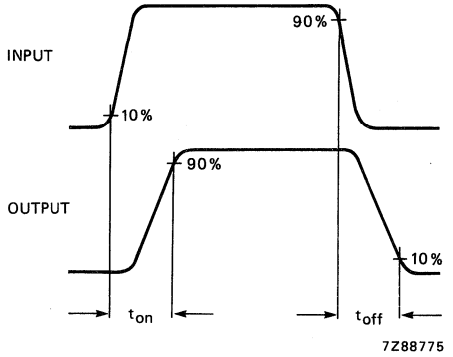


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5 Ω

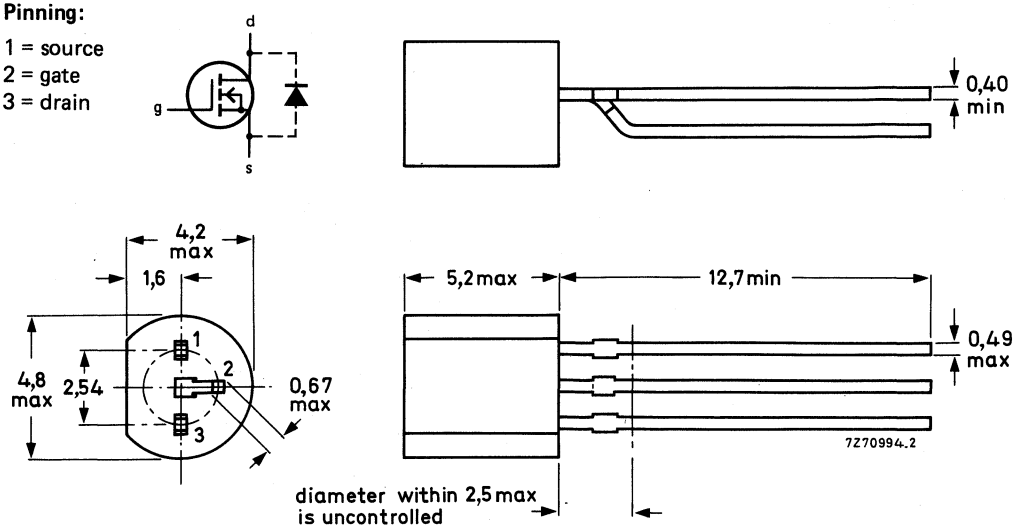
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pin configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Drain-gate voltage	V_{DG}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC) at T_c = 25 °C	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage V_{GS} = 0; I_D = 100 μA	$V_{(BR)DSS}$	min. typ.	60 V 90 V
Gate threshold voltage V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min. max.	0.8 V 3.0 V
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10 nA
Drain cut-off current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5 μA
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	typ. max.	2.5 Ω 5.0 Ω
Transfer admittance V_{DS} = 10 V; I_D = 200 mA;	$\lvert Y_{fs}\rvert$	typ.	200 mS
Capacitances at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	25 pF 40 pF
	C_{oss}	typ. max.	22 pF 30 pF
	C_{rss}	typ. max.	6 pF 10 pF
Switching times at I_D = 200 mA I_D = 200 mA; V_{DD} = 50 V;	t_{on}	typ. max.	4 ns 10 ns
V_{GS} = 0 to 10 V	t_{off}	typ. max.	4 ns 10 ns

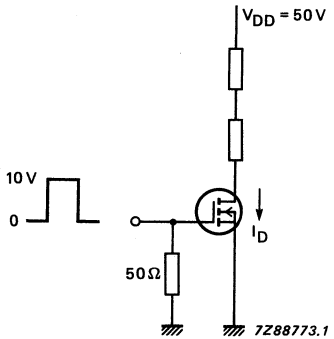


Fig. 2 Switching times test circuit.

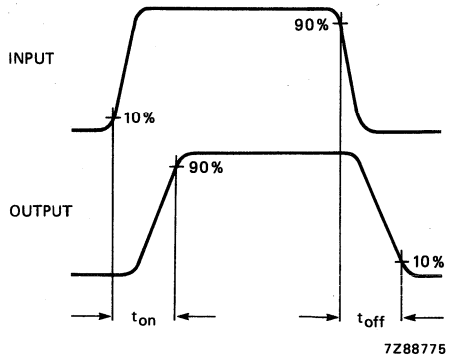


Fig. 3 Input and output waveforms.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

BS208

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

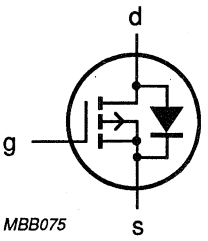


Fig.1 Symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	0.83	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

P-channel enhancement mode vertical D-MOS transistor

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	0.83	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
R_{thj-a}	from junction to ambient	150	K/W

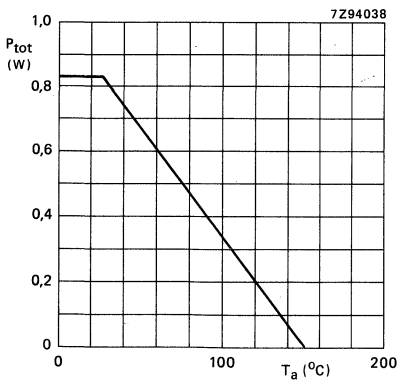

Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	200	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 130 V V_{GS} = 0	-	-	1	μA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 70 V $-V_{GS}$ = 0.2 V	-	-	25	μA
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	-	14	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	-	mS
C_{iss}	input capacitances	note 1	-	55	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	5	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

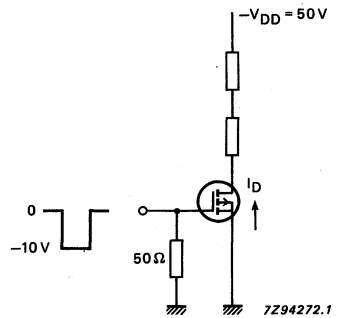

Fig.3 Switching times test circuit.

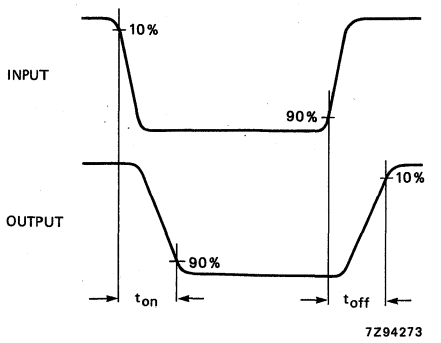

Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BS208

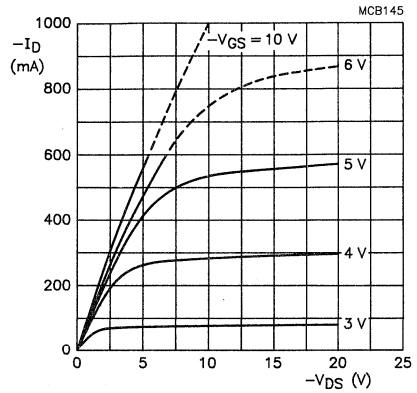

Fig.5 Typical output characteristics; T_j = 25 °C.

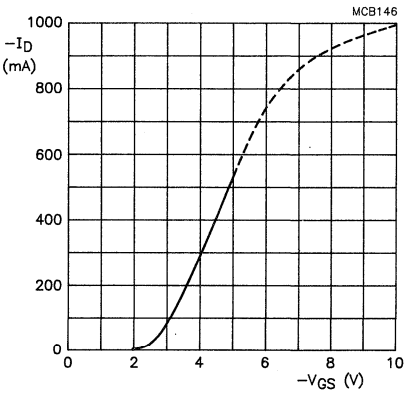

Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

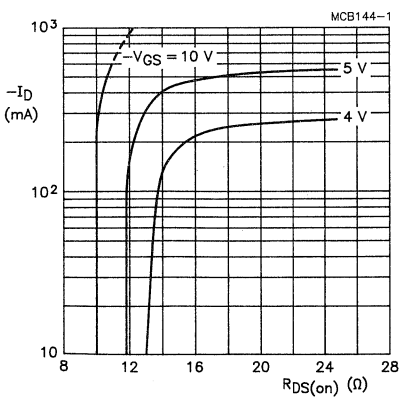

Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

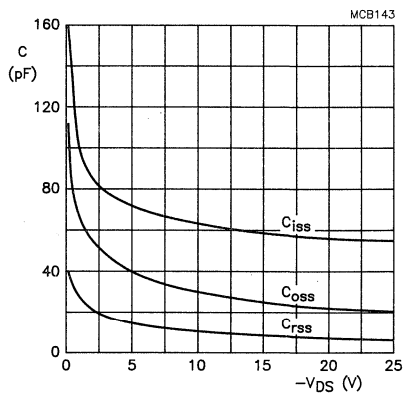

Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

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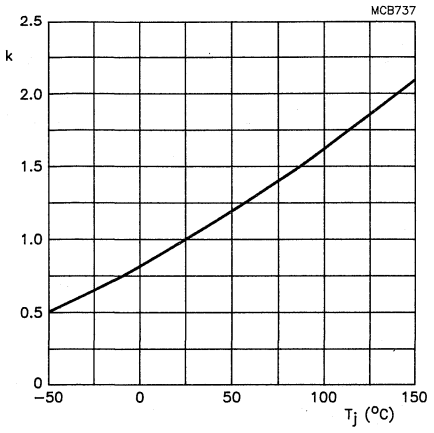

Fig.9 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C}$; typical $R_{DS\,(on)}$ at 200 mA/10 V;

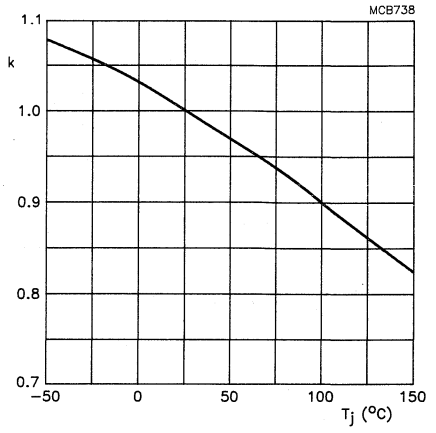

Fig.10 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C}$; typical $V_{GS\,(th)}$ at 1 mA.

P-channel enhancement mode vertical D-MOS transistor

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PACKAGE OUTLINE

Dimensions in mm

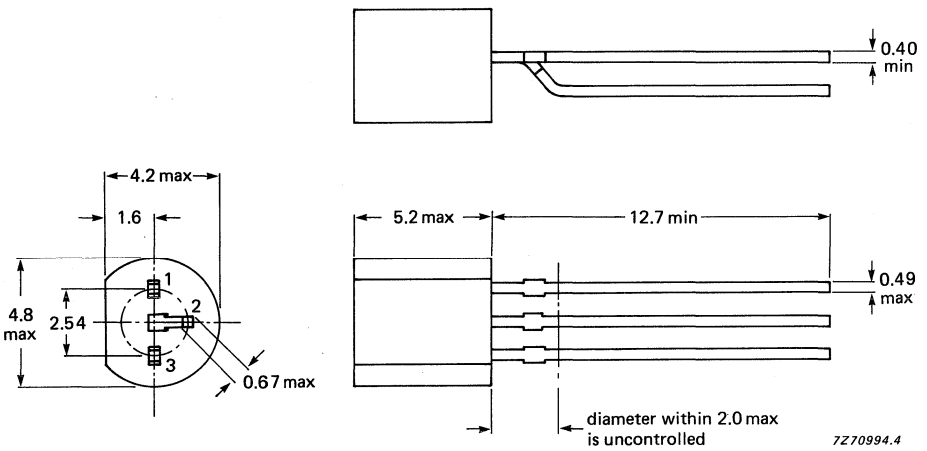


Fig.11 TO-92.

P-CHANNEL VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance at f = 1 kHz $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

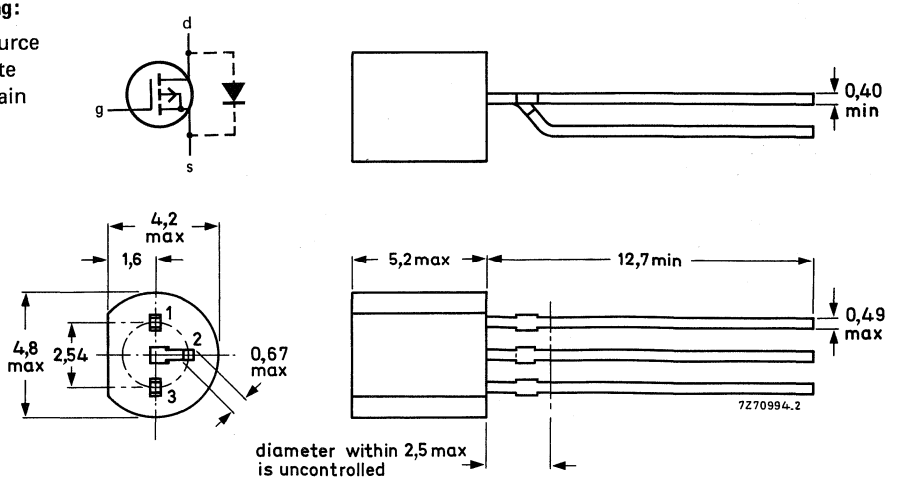
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak value)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DS}$	min.	45 V
Drain-source leakage current $-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5 μA
Gate-source leakage current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.0 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	9 Ω 14 Ω
Transfer admittance at f = 1 kHz $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{is}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{os}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rs}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_D$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

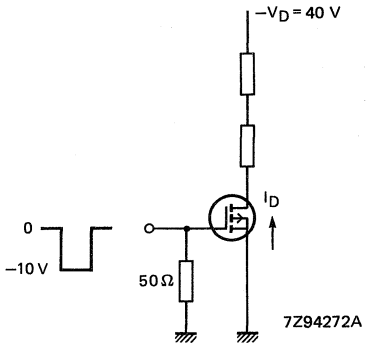


Fig. 2 Switching times test circuit.

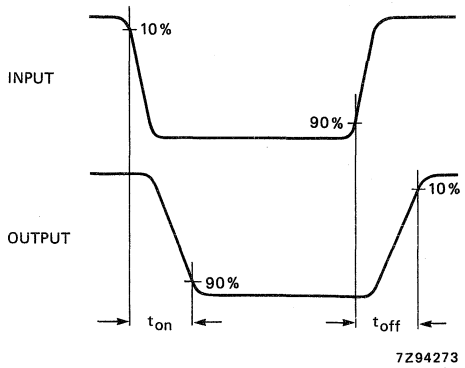


Fig. 3 Input and output waveforms.

Philips Components

Data sheet	
status	Product specification
date of issue	December 1990

BSN204/BSN204A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 (BSN204)

PIN	DESCRIPTION
1	source
2	gate
3	drain

PINNING - TO-92 (BSN204A)

PIN	DESCRIPTION
1	gate
2	drain
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	1.8	V

PIN CONFIGURATION

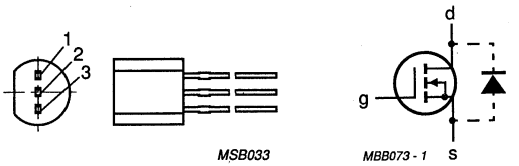


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.4	1	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

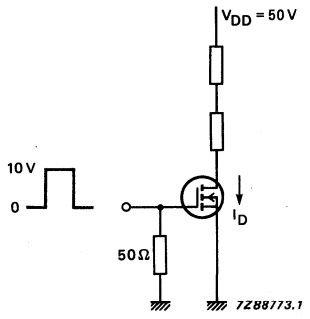


Fig.2 Switching time test circuit.

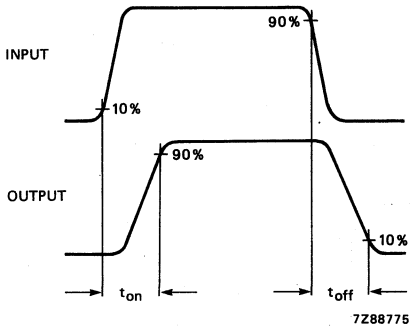
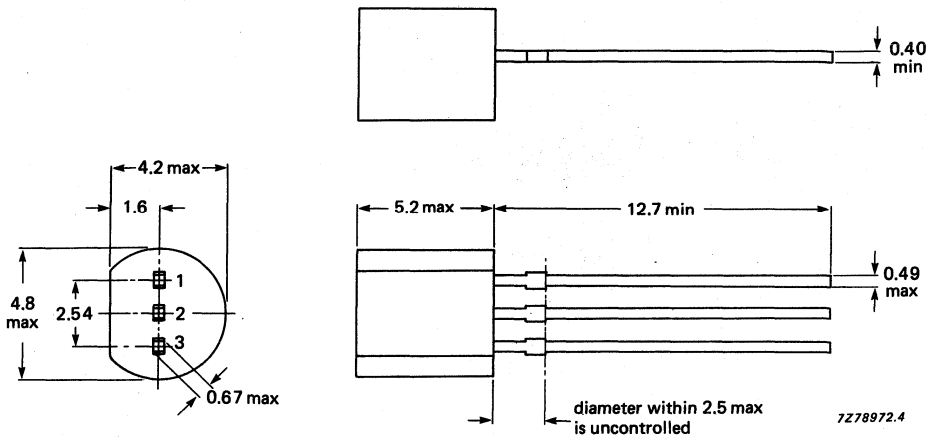


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSN204/BSN204A

PACKAGE OUTLINE



Dimensions in mm.

Fig.4 TO-92.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS

MECHANICAL DATA

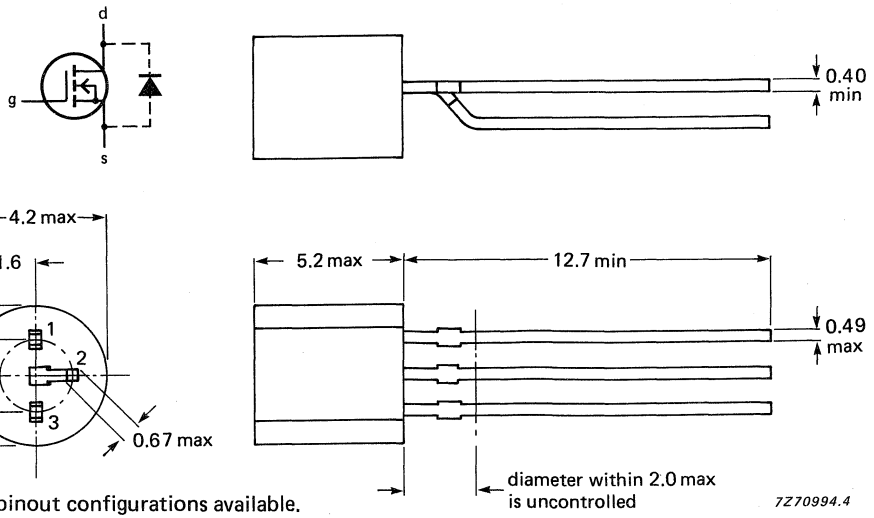
Dimensions in mm

Fig.1 TO-92 variant.

Pinning

BSN205
1 = gate
2 = drain
3 = source

BSN205A
1 = source
2 = gate
3 = drain



Note: various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

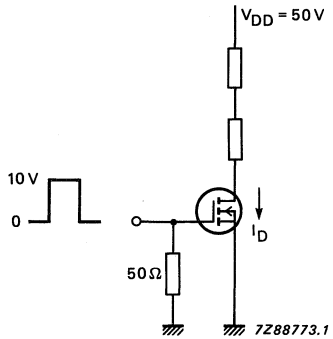


Fig.2 Switching time test circuit.

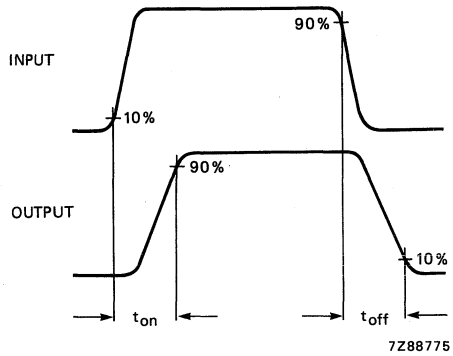


Fig.3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

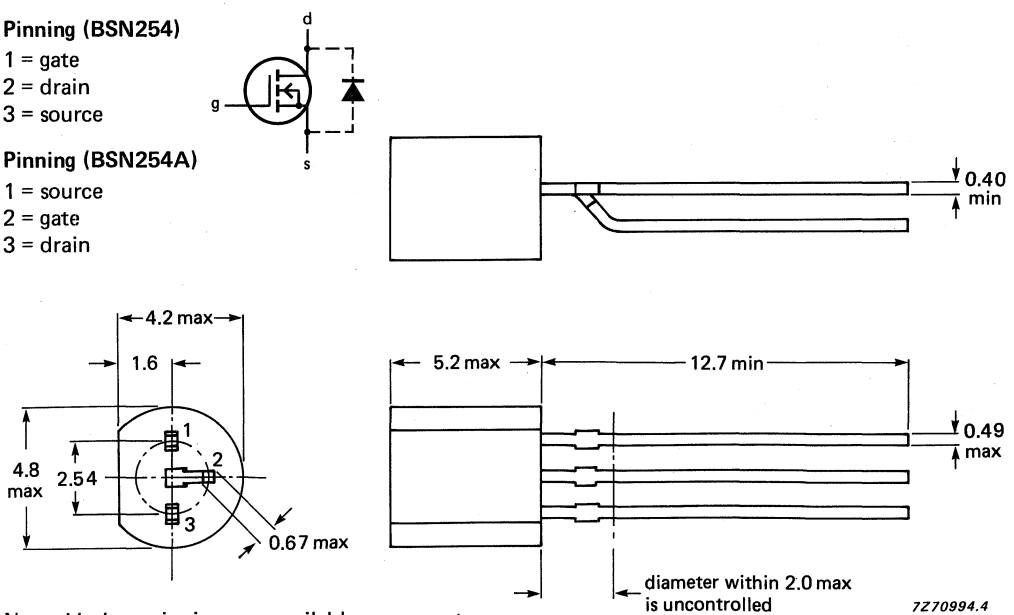
Fig.1 TO-92 variant.

Pinning (BSN254)

1 = gate
2 = drain
3 = source

Pinning (BSN254A)

1 = source
2 = gate
3 = drain



Note: Various pinnings are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250 V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.0 V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
I_D = 20mA; V_{GS} = 2.4V	$R_{DS(on)}$	max.	10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 400 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 15 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	20 ns 30 ns

Note

1. Device mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

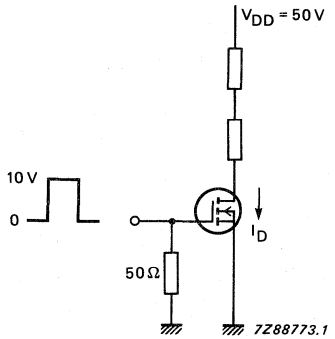


Fig.2 Switching times test circuit.

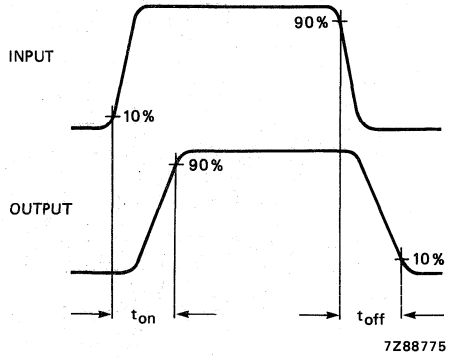


Fig.3 Input and output waveforms.

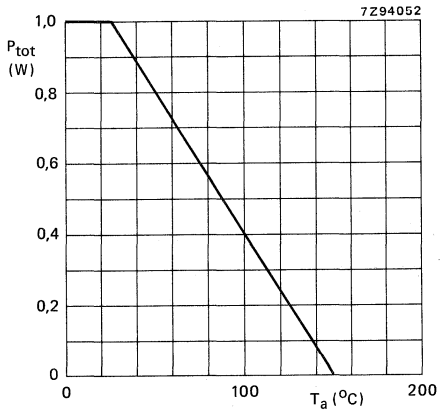


Fig.4 Power derating curve.

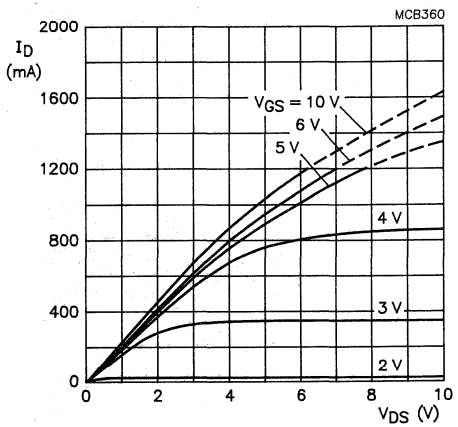


Fig.5 Output characteristics; T_j = 25 °C; typical values.

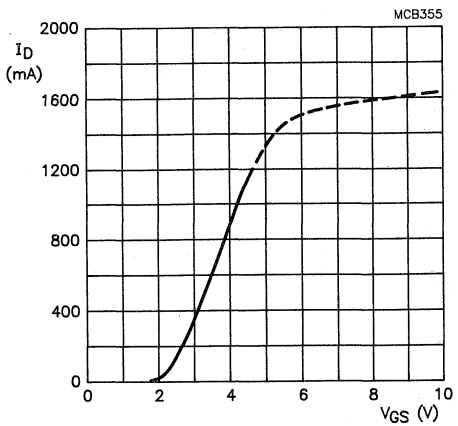


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

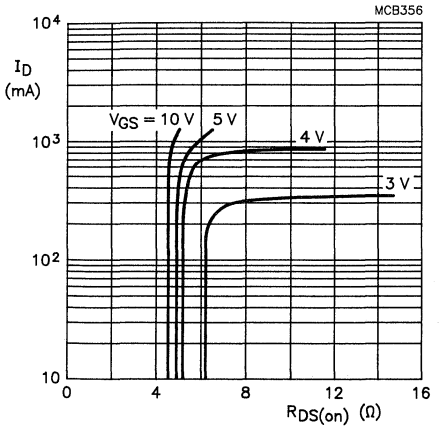


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

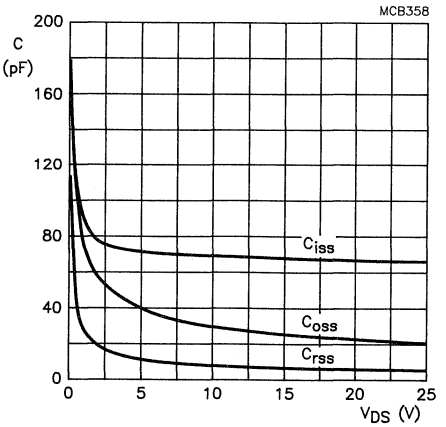


Fig.8 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

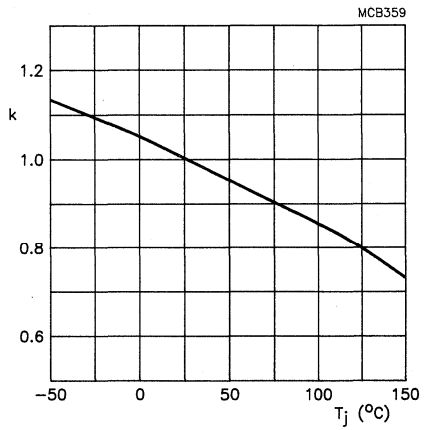


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$;

$V_{GS(th)}$ at 1 mA; typical values.

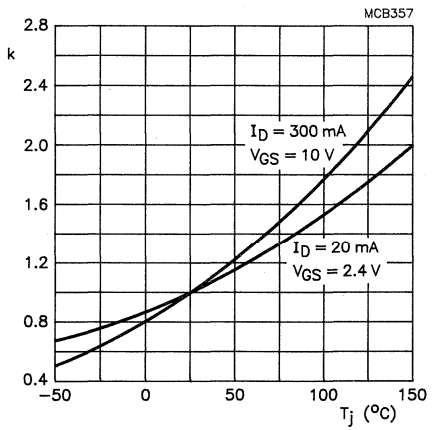


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^oC}$;

typical values.

Data sheet	
status	Preliminary specification
date of issue	October 1990

BSN274/BSN274A

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

MECHANICAL DATA

Dimensions in mm

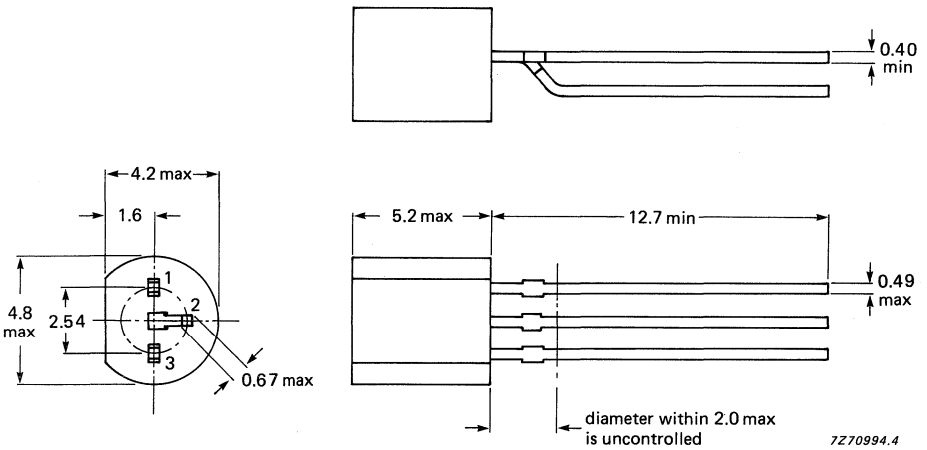


Fig.1 TO-92 variant.

PIN CONFIGURATION

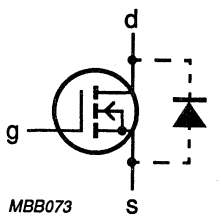


Fig.2 Pin configuration.

PINNING (BSN274)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	250	mA
I_{DM}	drain current	peak	-	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	270	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V V_{GS} = 0	-	-	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA V_{GS} = 10 V	-	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.4 V	-	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 25 V	200	400	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	5	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

BSN274/BSN274A

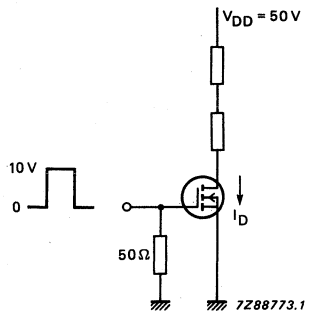


Fig.2 Switching time test circuit.

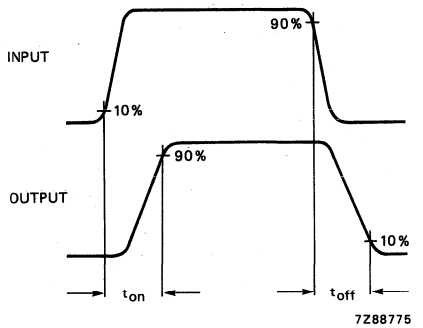


Fig.3 Input and output waveforms.

Philips Components

Data sheet	
status	Product specification
date of issue	November 1990

BSP103/BSP105/BSP109
N-channel enhancement mode vertical D-MOS transistors

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS(on)}$.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, designed for application as low power, high frequency inverters and line drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

MARKING CODES

BSP103: BSP103
BSP105: BSP105
BSP109: BSP109

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage			
	BSP103		35	V
	BSP105		60	V
	BSP109		90	V
I_D	drain current	DC value		
	BSP103		700	mA
	BSP105		500	mA
	BSP109		450	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 1 A V_{GS} = 10 V		
	BSP103		1.8	Ω
	BSP105		3	Ω
	BSP109		4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2	V

PIN CONFIGURATION

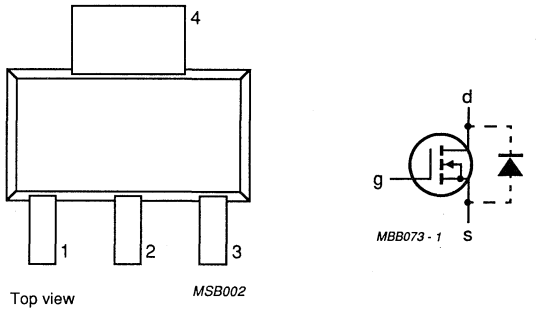


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistors

BSP103/BSP105/BSP109

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage				
	BSP103		–	35	V
	BSP105		–	60	V
	BSP109		–	90	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	30	V
I_D	drain current	DC value			
	BSP103		–	700	mA
	BSP105		–	500	mA
	BSP109		–	450	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead minimum 6 mm^2.

N-channel enhancement mode vertical D-MOS transistors

BSP103/BSP105/BSP109

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA V_{GS} = 0				
	BSP103		35	–	–	V
	BSP105		60	–	–	V
	BSP109		90	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = $V_{DS\ max.}$ V_{GS} = 0	–	–	10	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2	V
$I_{D(on)}$	on-state drain current	V_{DS} = 25 V V_{GS} = 10 V	1	2	–	A
$R_{DS(on)}$	drain-source on-resistance	I_D = 300 mA V_{GS} = 5 V				
	BSP103		–	1.5	5	Ω
	BSP105		–	1.8	5	Ω
	BSP109		–	2.4	5.3	Ω
		I_D = 1 A V_{GS} = 10 V				
	BSP103		–	0.9	1.8	Ω
	BSP105		–	1.4	3	Ω
	BSP109		–	1.9	4	Ω
$\lvert y_{fs} \rvert$	transfer admittance	I_D = 500 mA V_{DS} = 25 V	170	–	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	–	60	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz				
	BSP103		–	–	50	pF
	BSP105		–	–	40	pF
	BSP109		–	–	40	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	–	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 500 mA V_{DD} = 25 V V_{GS} = 0 to 10 V	–	–	10	ns

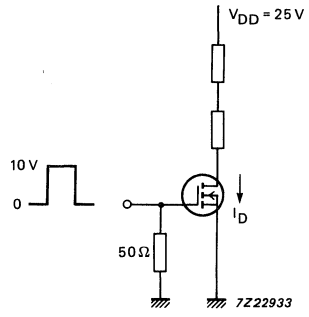


Fig.2 Switching time test circuit.

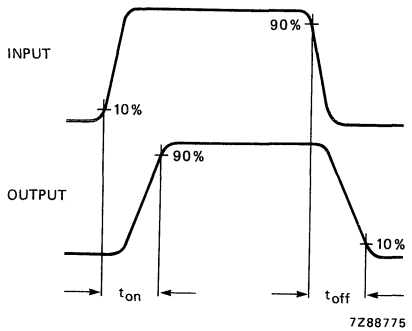
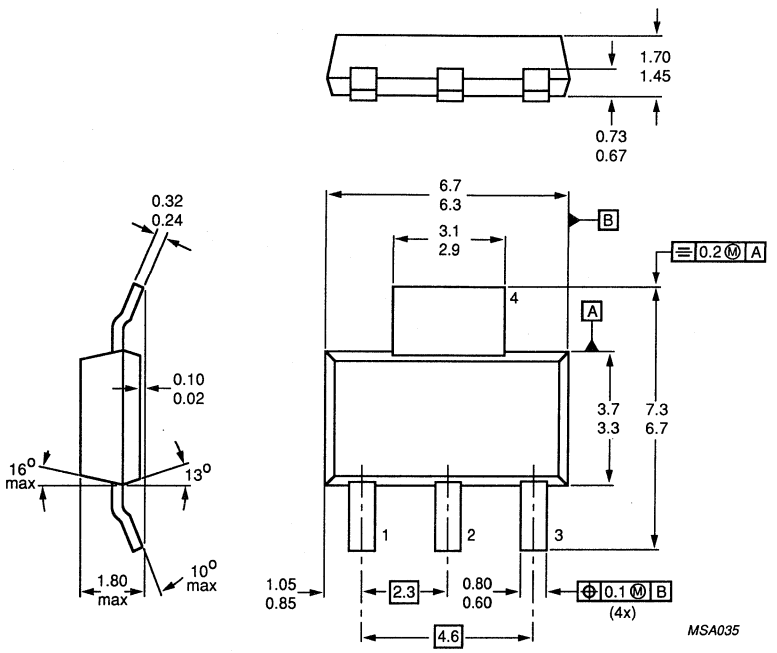


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSP103/BSP105/BSP109

PACKAGE OUTLINE



Dimensions in mm.

Fig.4 SOT223.

Data sheet	
status	Product specification
date of issue	October 1990

BSP106
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

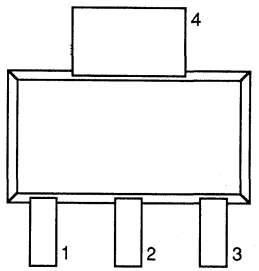
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION



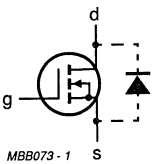


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP106

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP106

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

N-channel enhancement mode vertical D-MOS transistor

BSP106

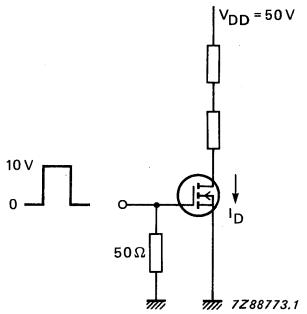


Fig.2 Switching time test circuit.

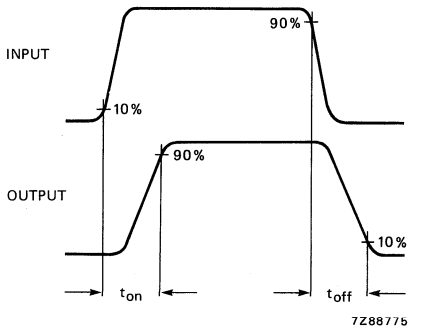


Fig.3 Input and output waveforms.

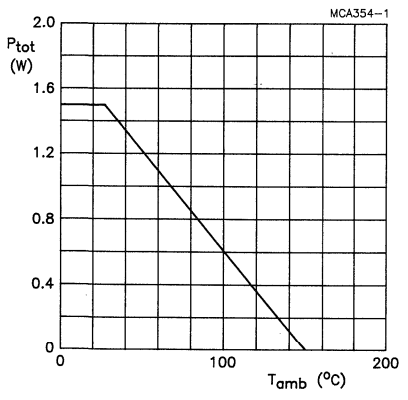


Fig.4 Power derating curve.

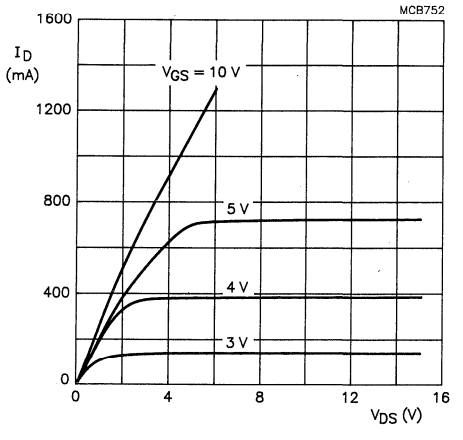


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

BSP106

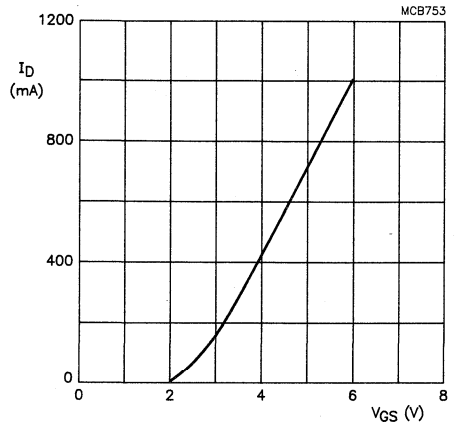


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

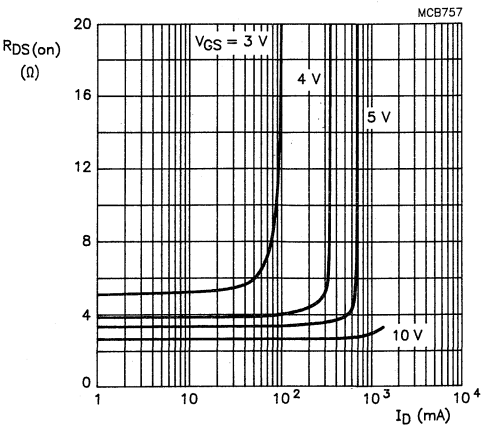


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

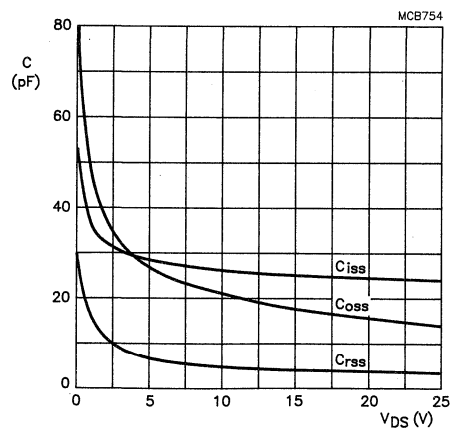


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

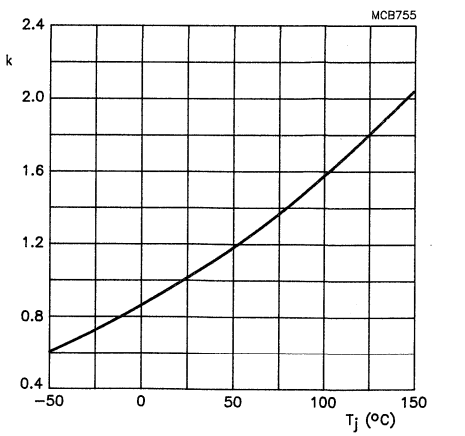


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}$; typical $R_{DS(on)}$ at 200 mA/10 V.

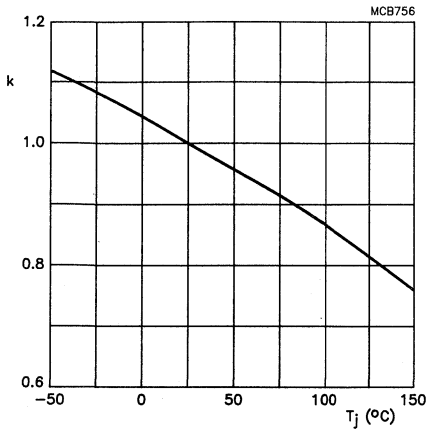
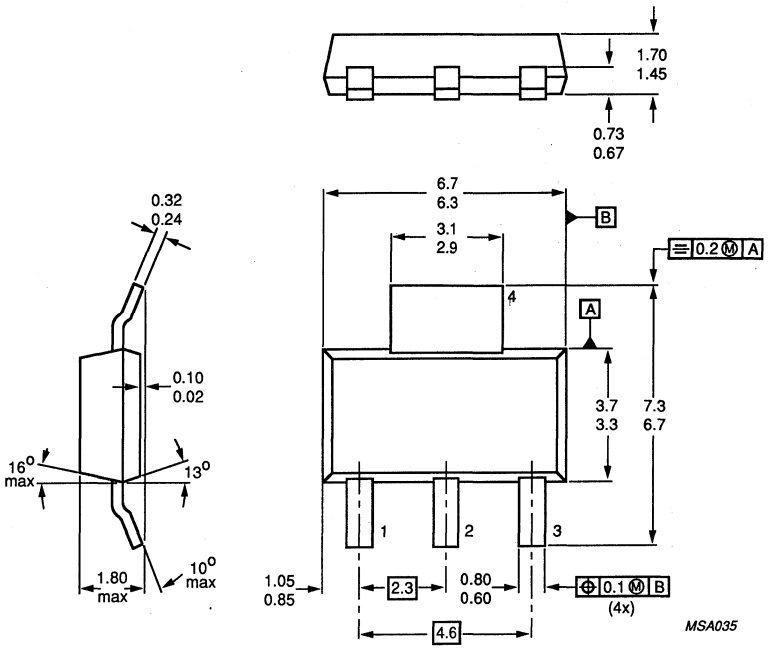


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,°C}$; typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BSP106

PACKAGE OUTLINE



Dimensions in mm.

Marking code: BSP106.

Fig.11 SOT223.

Data sheet	
status	Preliminary specification
date of issue	October 1990

BSP107

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer driver switching.

PIN CONFIGURATION

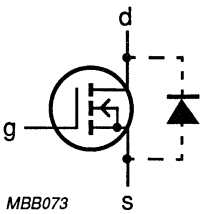


Fig.1 Symbol.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	200	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

N-channel enhancement mode vertical D-MOS transistor

BSP107

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
I_D	drain current	DC	-	200	mA
I_{DM}	drain current	peak	-	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	-	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Notes

1. Device mounted on an epoxy printed circuit board, 40 mm x 40 mm x 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 µA	200	-	-	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	-	-	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	-	-	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	-	-	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	-	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	-	14	-	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	-	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	-	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 - 10 V	-	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSP107

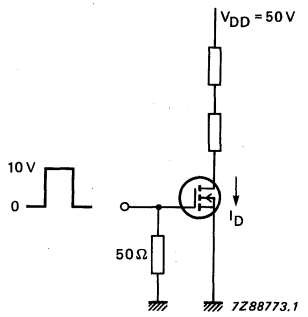


Fig.2 Switching time test circuit.

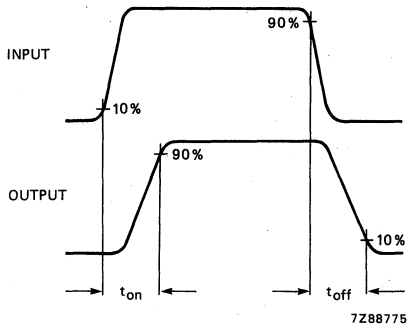


Fig.3 Input and output waveforms.

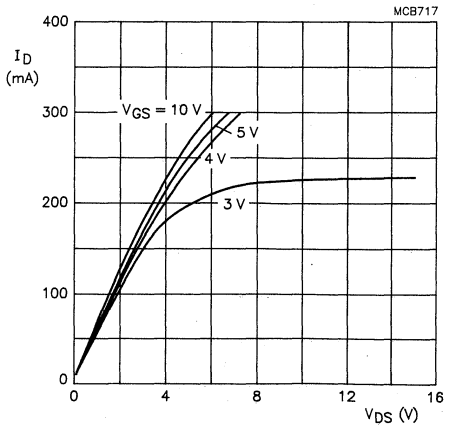


Fig.4 Typical output characteristics; T_j = 25° C.

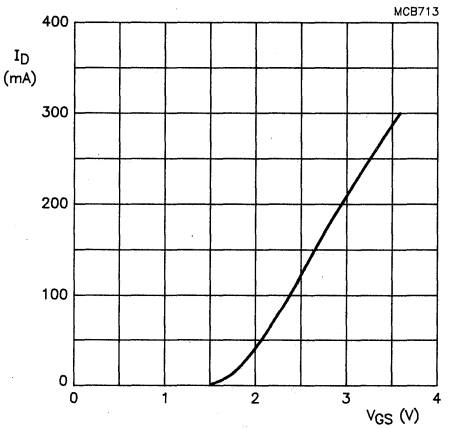


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

N-channel enhancement mode vertical D-MOS transistor

BSP107

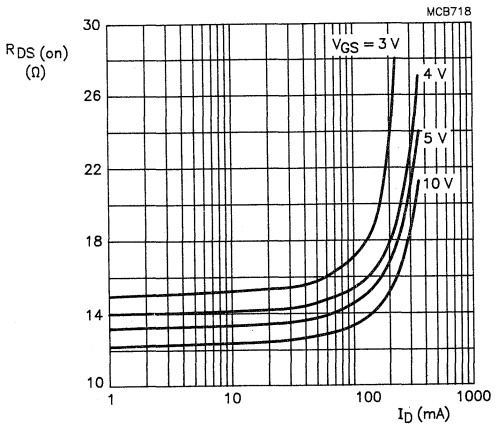


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

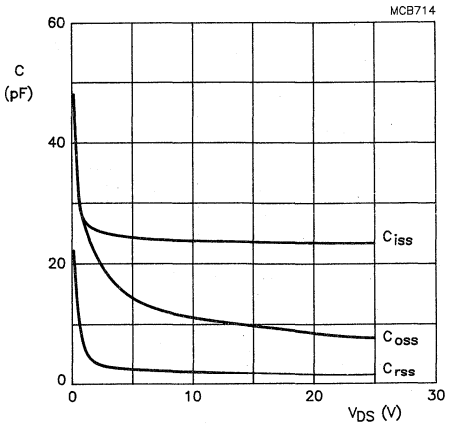


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C

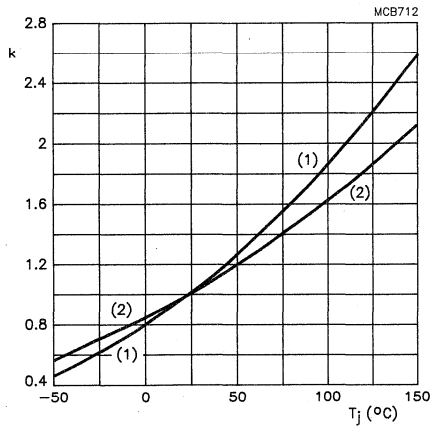


Fig.8 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25°\,C}$;

typical $R_{DS(on)}$ at 150 mA/10 V;

(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V;

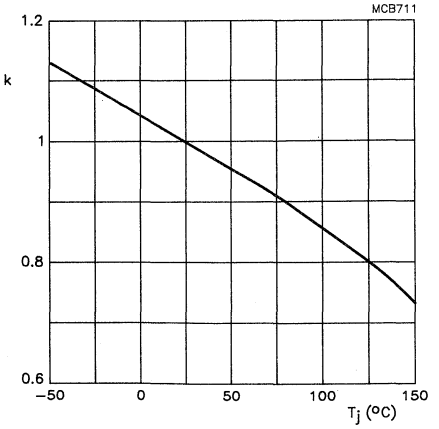


Fig.9 Temperature coefficient of gate-source threshold voltage;

$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25°\,C}$; typical $V_{Gs(th)}$ at 1 mA.

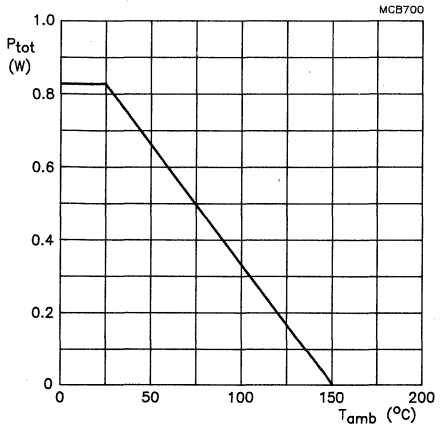


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BSP107

PACKAGE OUTLINE

Dimensions in mm

Marking code:

BSP107 = BSP107

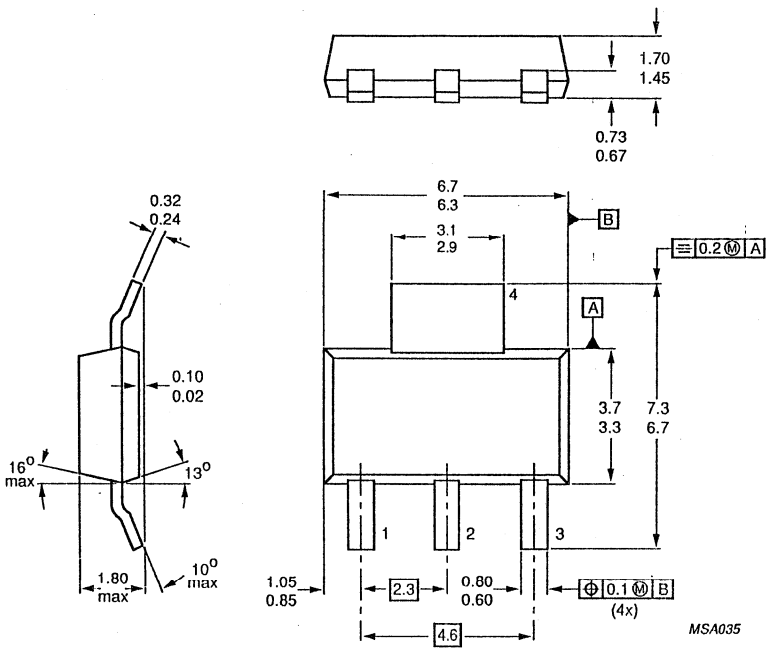


Fig.11 SOT223

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.0 Ω 3.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	min. typ.	150 mS 300 mS

MECHANICAL DATA Dimensions in mm

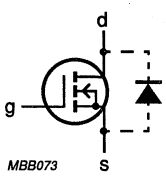
Fig.1 SOT223.

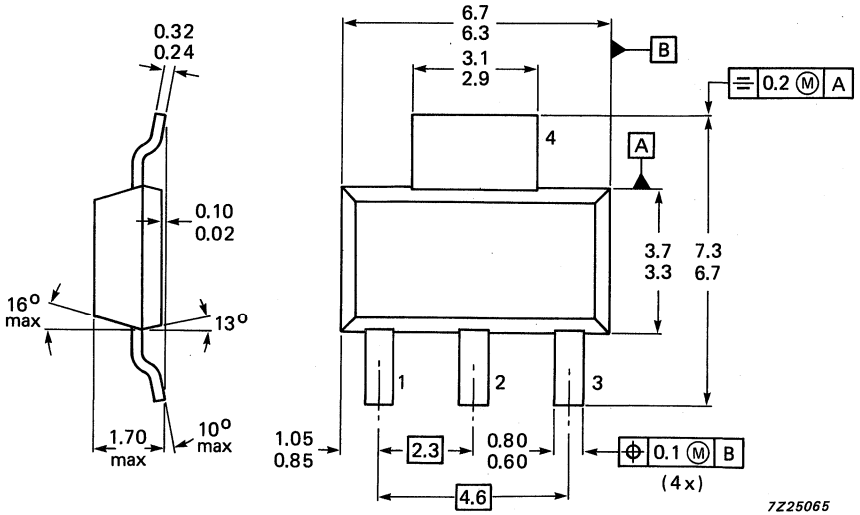
Marking code

BSP108

Pinning

1 = gate
2 = drain
3 = source
4 = drain





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	500 mA
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.0 Ω 3.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	min. typ.	150 mS 300 mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 8 ns
	t_{off}	typ. max.	10 ns 15 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

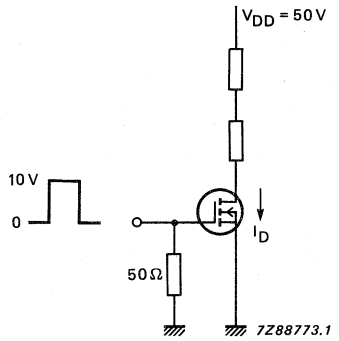


Fig.2 Switching times test circuit.

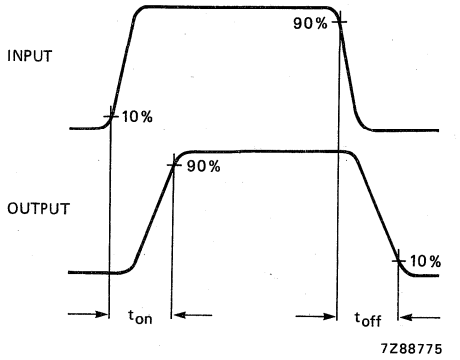


Fig.3 Input and output waveforms.

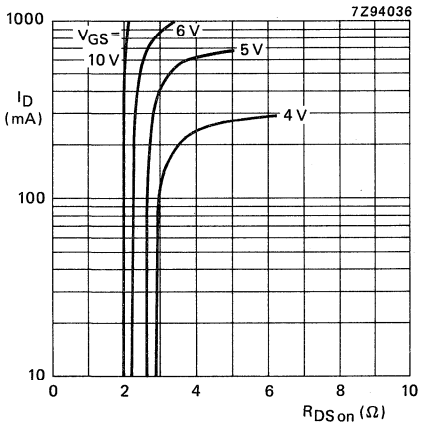


Fig.4 T_j = 25 °C; typical values.

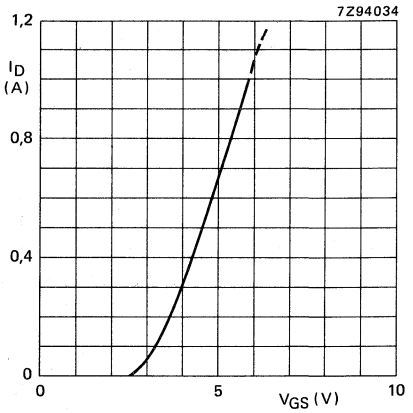


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

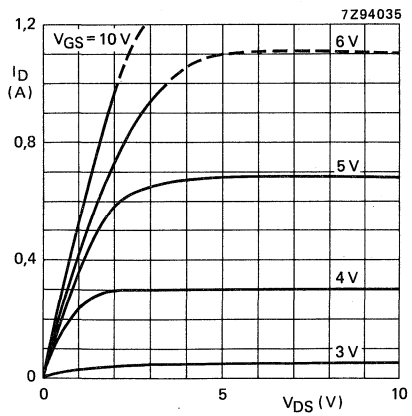


Fig.6 T_j = 25 °C; typical values.

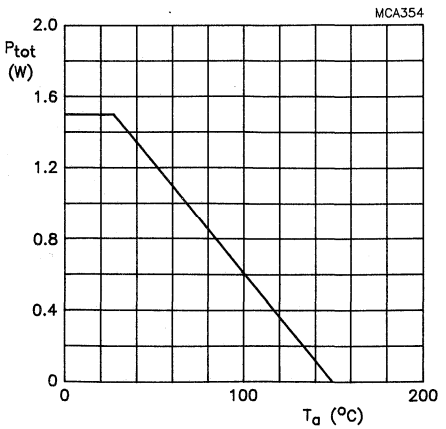


Fig.7 Power derating curve.

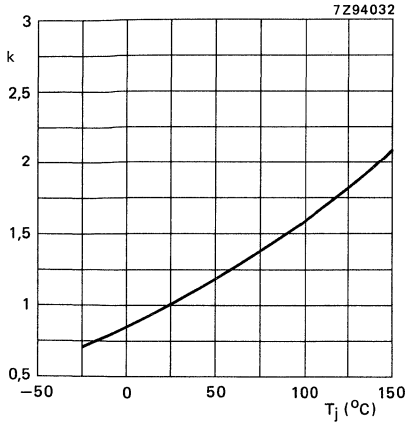


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typ. values at 500 mA/10 V.

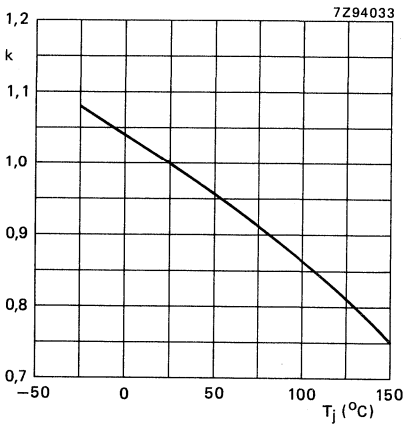


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

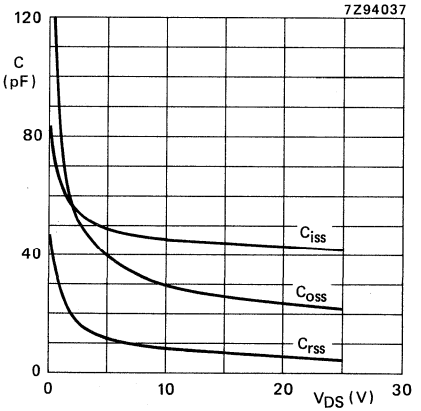


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

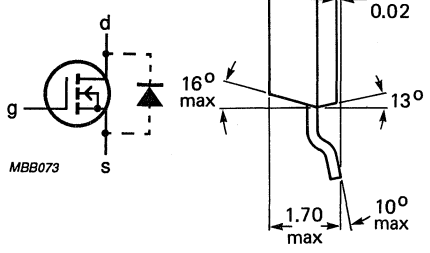
Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	325 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1.5 W
Drain-source ON-resistance $I_D = 200$ mA; $V_{GS} = 10$ V	R_{DSon}	typ. max.	4.5 Ω 7 Ω
Transfer admittance $I_D = 200$ mA; $V_{DS} = 15$ V	$\|Y_{fs}\|$	min. typ.	75 mS 150 mS

MECHANICAL DATA

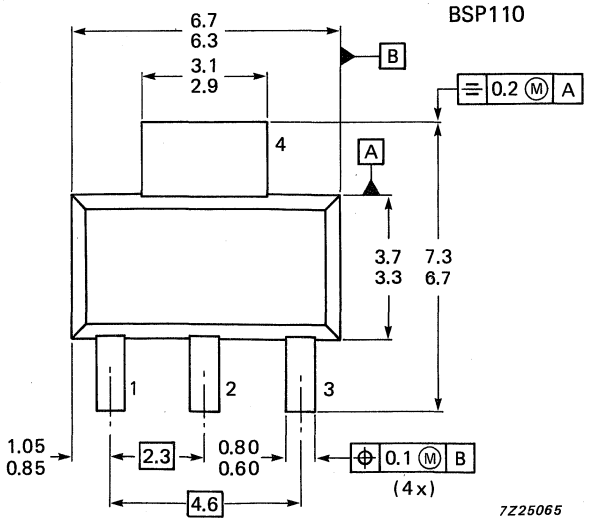
Fig.1 SOT223.

Pinning

1 = gate
2 = drain
3 = source
4 = drain



Dimensions in mm



Marking code

BSP110

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	325 mA
Drain current (peak)	I_{DM}	max.	650 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$I_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
I_D = 200 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 7 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min. typ.	75 mS 150 mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm².

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3 pF
		max.	6 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2 ns
		max.	5 ns
	t_{off}	typ.	5 ns
		max.	10 ns

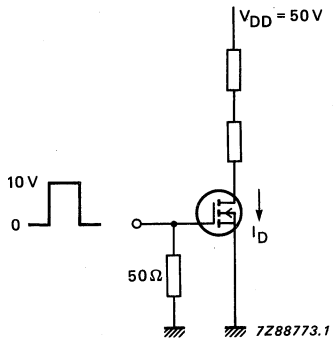


Fig.2 Switching time test circuit.

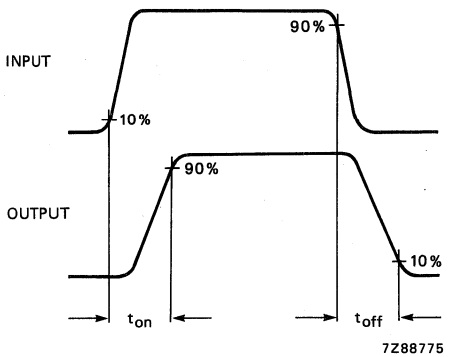


Fig.3 Input and output waveforms.

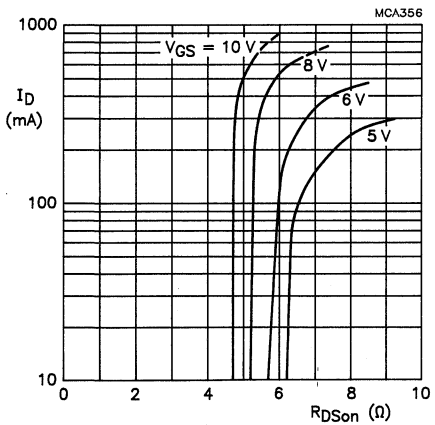


Fig.4 T_j = 25 °C; typical values.

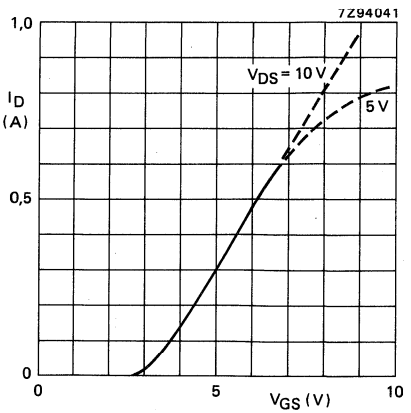


Fig.5 T_j = 25 °C; typical values.

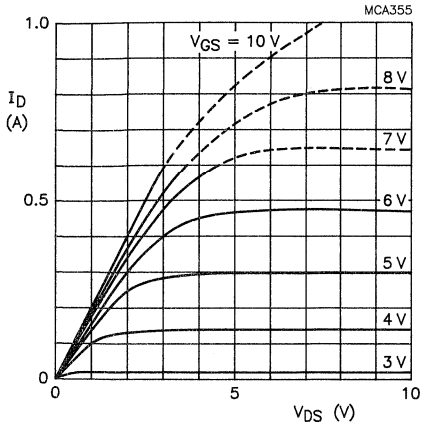


Fig.6 T_j = 25 °C; typical values.

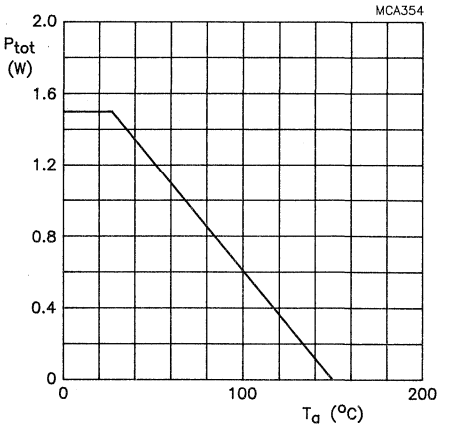


Fig.7 Power derating curve.

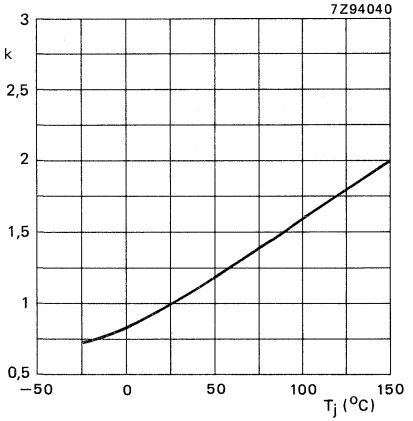


Fig.8 $k = \frac{R_{DSon \text{ at } T_j}}{R_{DSon \text{ at } 25\,^oC}}$;
typical values at 150 mA/5 V.

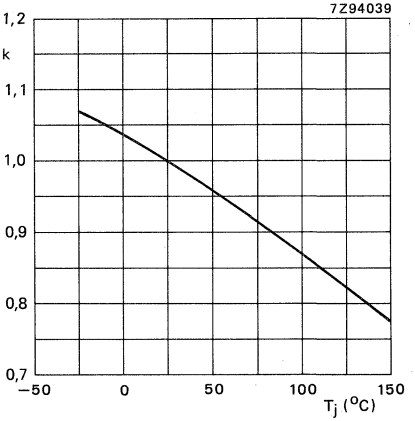


Fig.9 $k = \frac{V_{GS(th) \text{ at } T_j}}{V_{GS(th) \text{ at } 25\,^oC}}$;
$V_{GS(th)}$ at 1 mA; typical values.

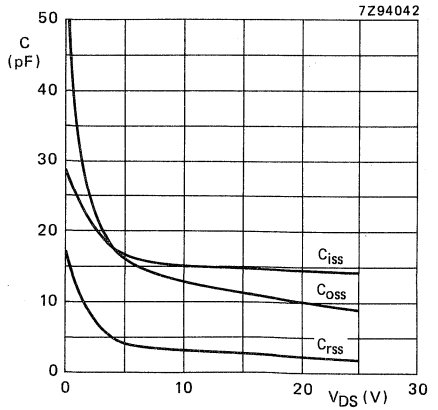


Fig.10 T_j = 25 °C; V_{GS} = 0;
f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain-current (DC)	I_D	max.	250 mA
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 Ω 12 Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8 V

MECHANICAL DATA

Dimensions in mm

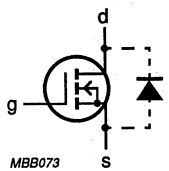
Fig.1 SOT223.

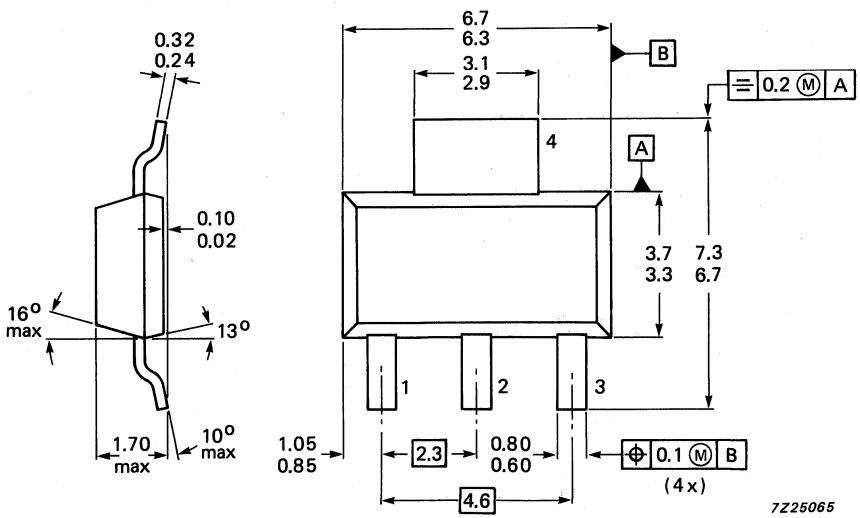
Marking code

BSP120

Pinning

1 = gate
2 = drain
3 = source
4 = drain





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Drain-source ON-resistance (see Fig.4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	7 Ω 12 Ω
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	min. typ.	125 mS 250 mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 65 pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	3	ns
	max.	6	ns
t_{off}	typ.	15	ns
	max.	20	ns

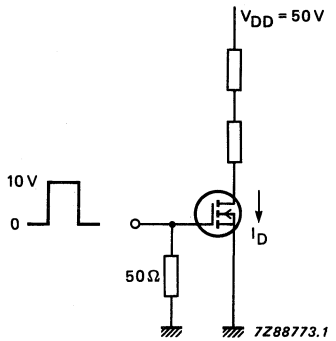


Fig.2 Switching time test circuit.

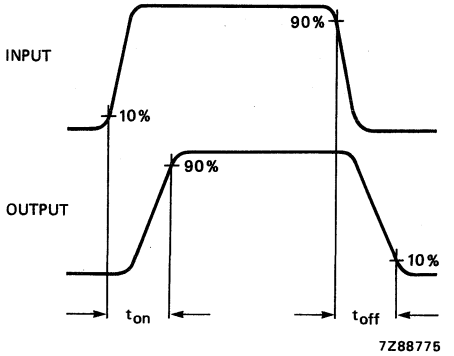


Fig.3 Input and output waveforms.

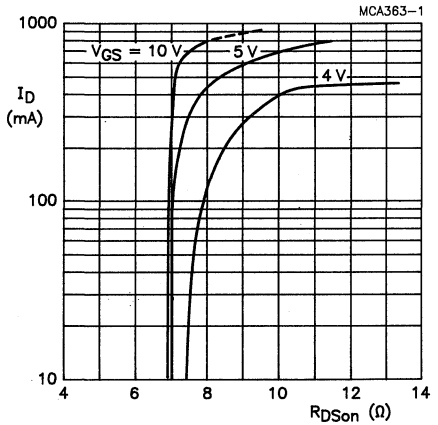


Fig.4 T_j = 25 °C; typical values.

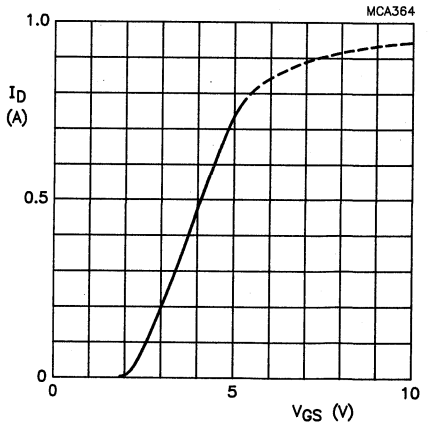


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

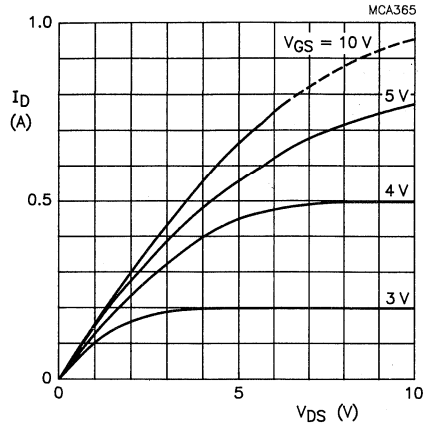


Fig.6 T_j = 25 °C; typical values.

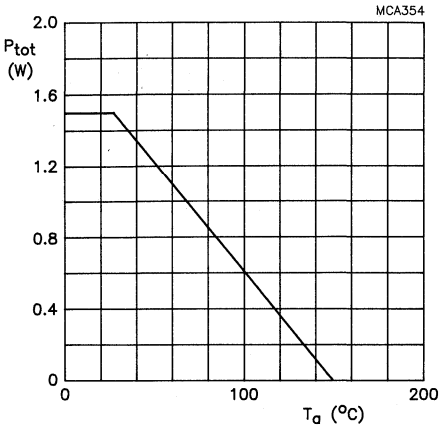


Fig.7 Power derating curve.

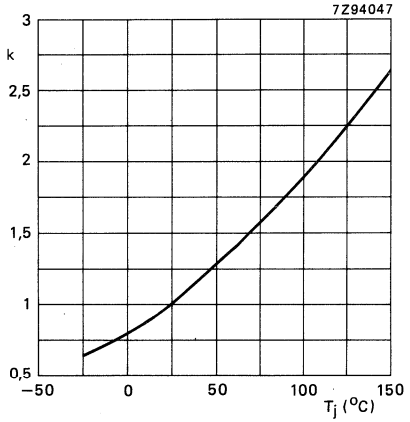


Fig.8 $k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ ^oC}$; at 250 mA/10 V; typical values.

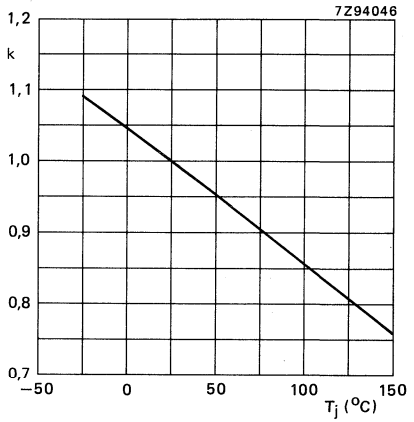


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

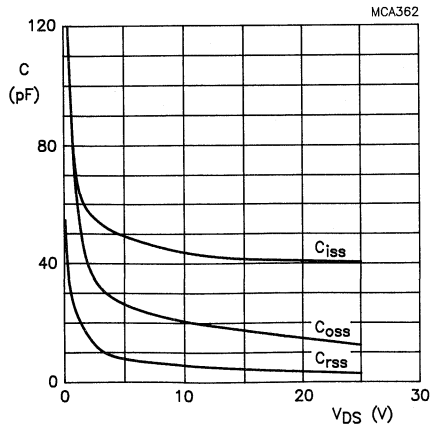


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min. typ.	200 mS 350 mS

MECHANICAL DATA

Dimensions in mm

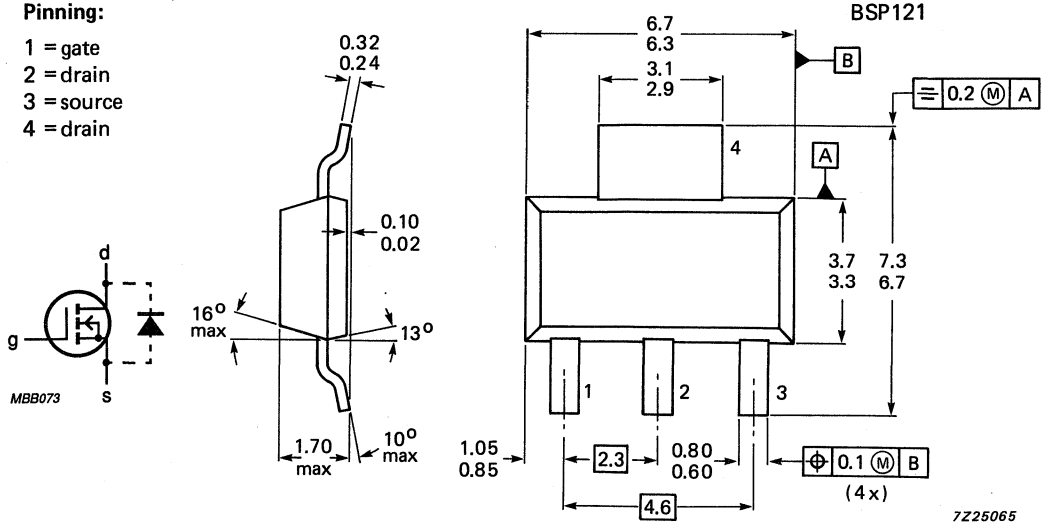
Fig.1 SOT223.

Pinning:

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP121



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.2 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{thj\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 mS 350 mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V

t_{on}	typ.	5	ns
	max.	10	ns
t_{off}	typ.	15	ns
	max.	20	ns

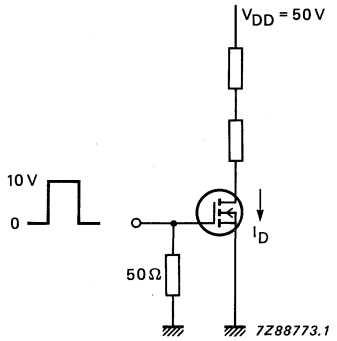


Fig.2 Switching time test circuit

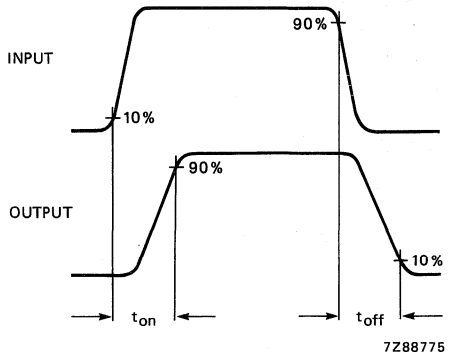


Fig.3 Input and output waveforms.

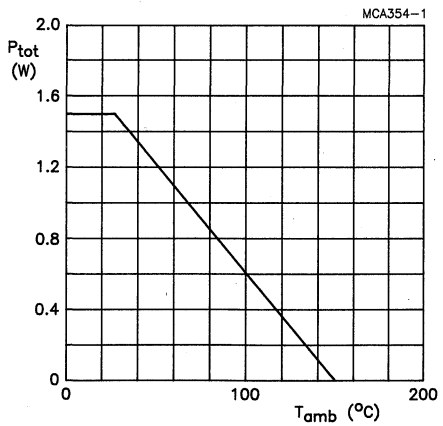


Fig.4 Power derating curve.

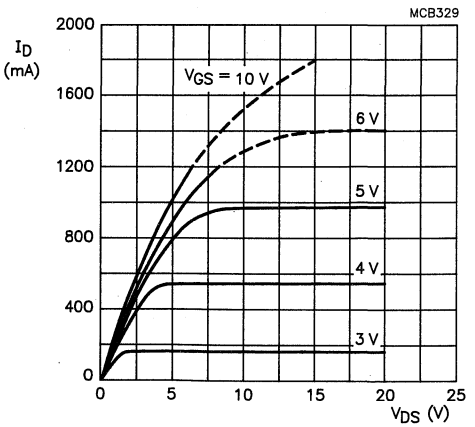


Fig.5 Output characteristic;
T_j = 25 °C; typical value.

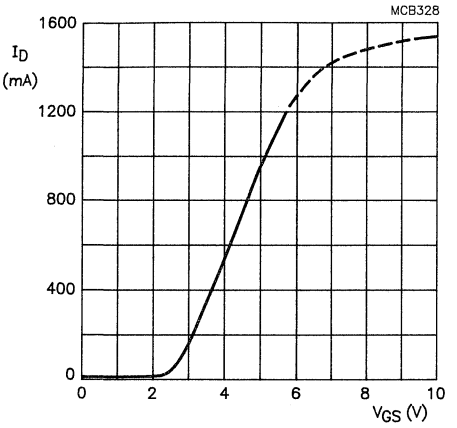


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical values.

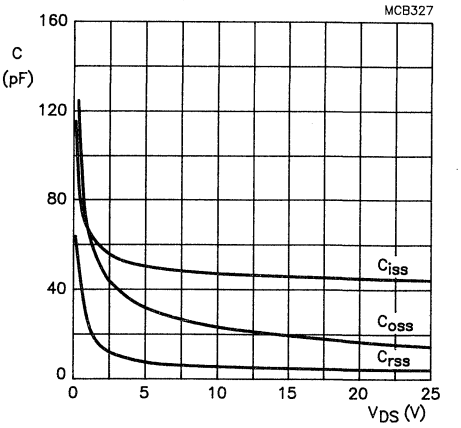


Fig.7 Capacitance as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

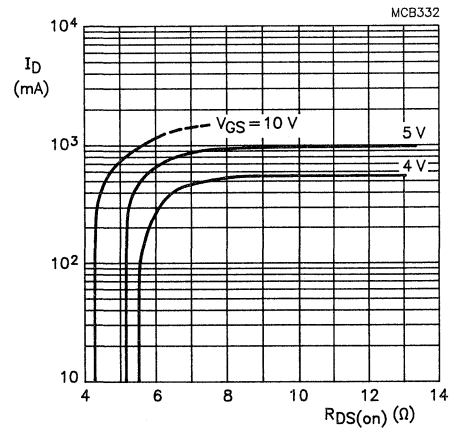


Fig.8 T_j = 25 °C; typical values.

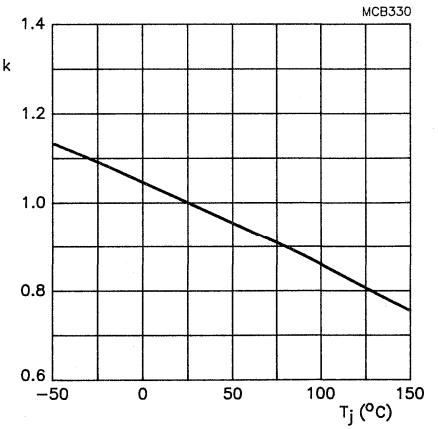


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

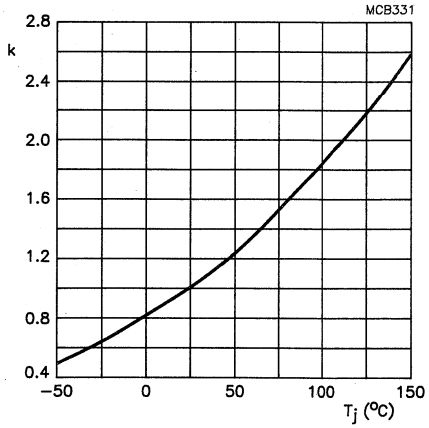


Fig.10 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^{o}C}$; at 400 mA/10V; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

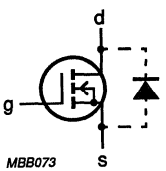
Fig.1 SOT223.

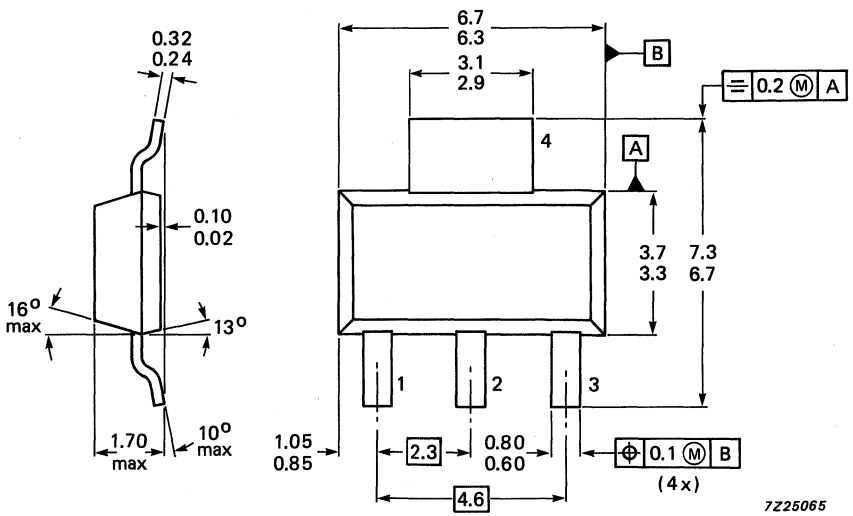
Marking code

BSP126

Pinning

1 = gate
2 = drain
3 = source
4 = drain





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.0	V V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 7.0	Ω Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 400	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 90	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	5 15	pF pF

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

Switching times (see Figs 2 and 3)
I_D = 250 mA; V_{DD} = 50 V;
V_{GS} = 0 to 10 V

t_{on}	typ.	5 ns
	max.	10 ns
t_{off}	typ.	20 ns
	max.	30 ns

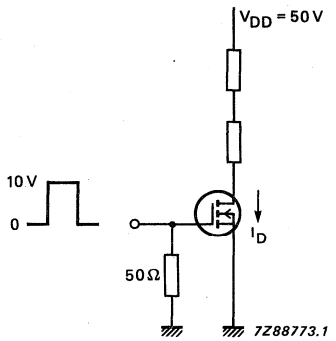


Fig.2 Switching time test circuit.

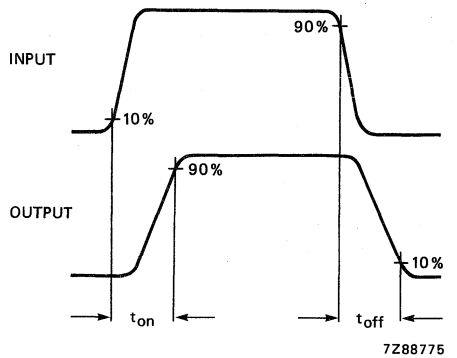


Fig.3 Input and output waveforms.

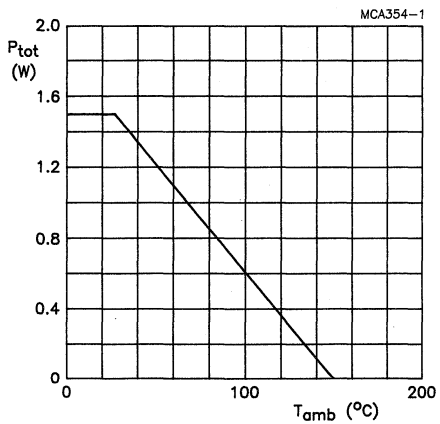


Fig.4 Power derating curve.

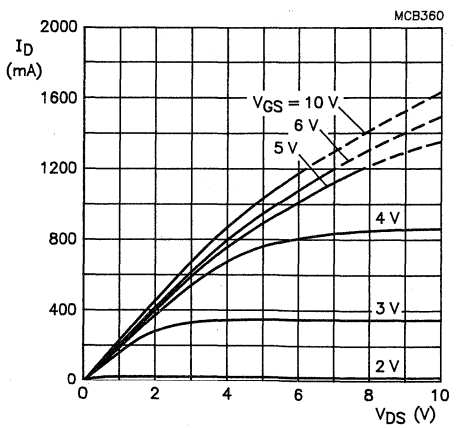


Fig.5 Output characteristics; T_j = 25 °C; typical values.

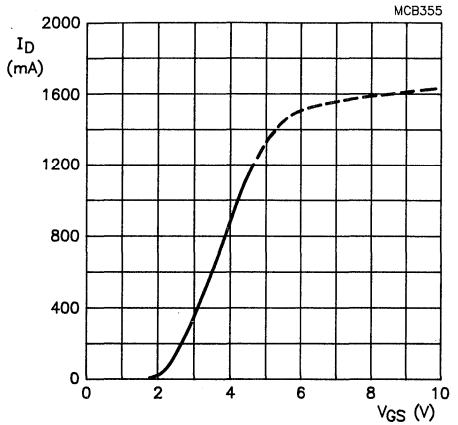


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

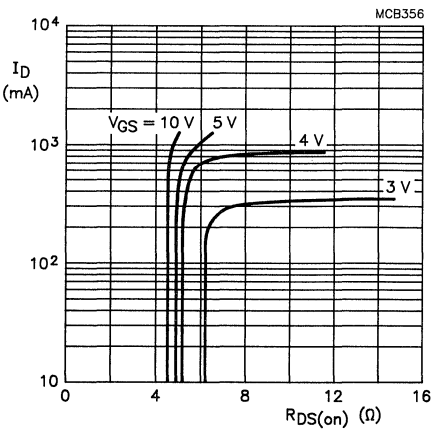


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

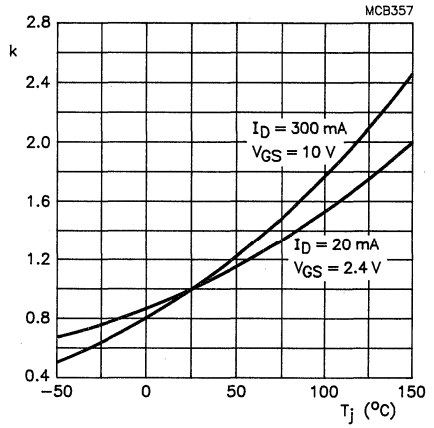


Fig.8 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^\circ C}$; typical values.

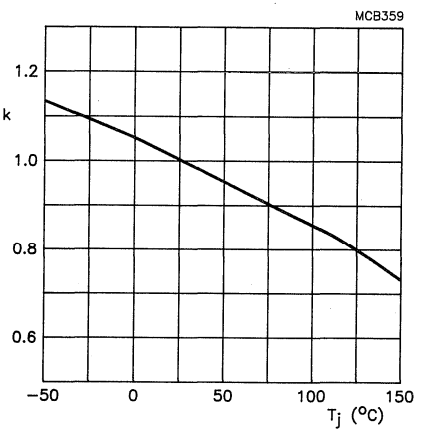


Fig.9 $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C}$; $V_{GS(th)}$ at 1 mA; typical values.

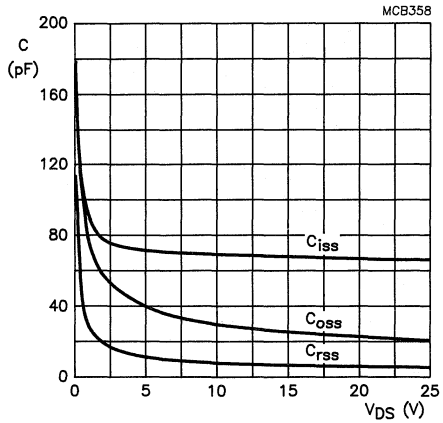


Fig.10 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

Data sheet	
status	Product specification
date of issue	November 1990

BSP204/BSP204A
P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

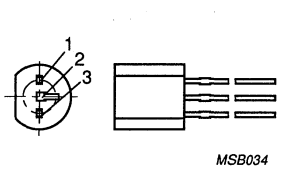
PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION



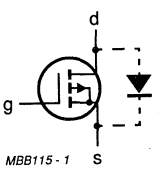


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

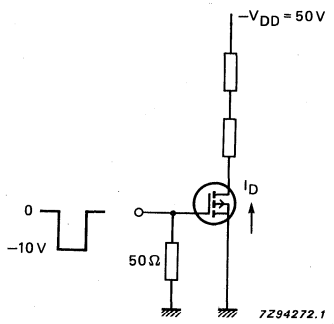


Fig.2 Switching time test circuit.

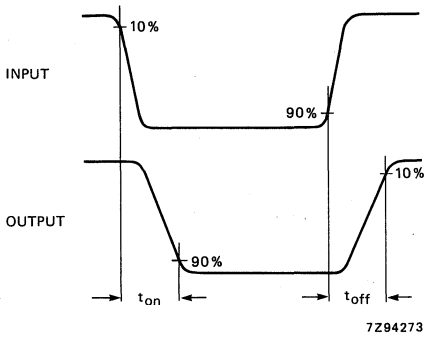


Fig.3 Input and output waveforms.

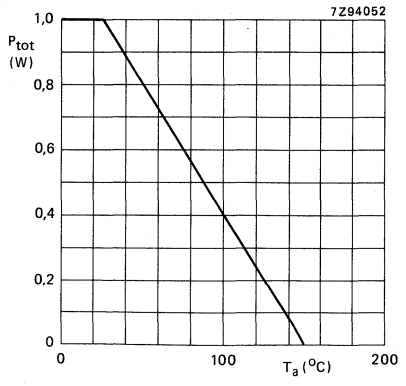


Fig.4 Power derating curve.

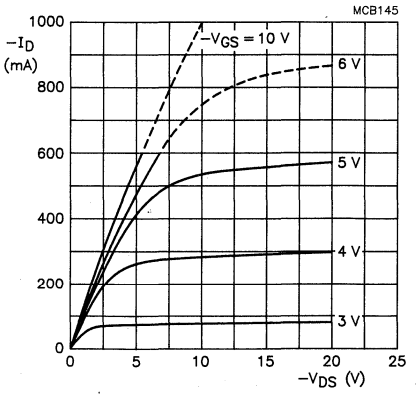


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

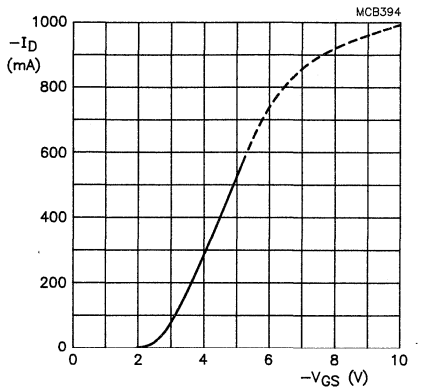


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

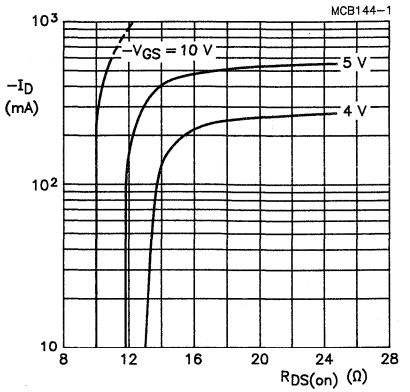


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

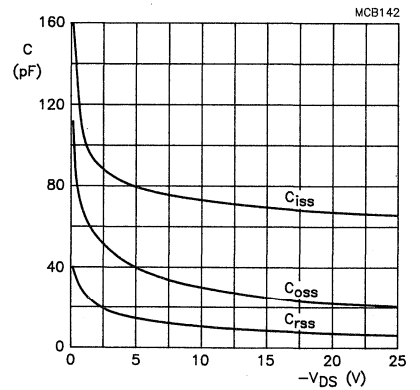


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

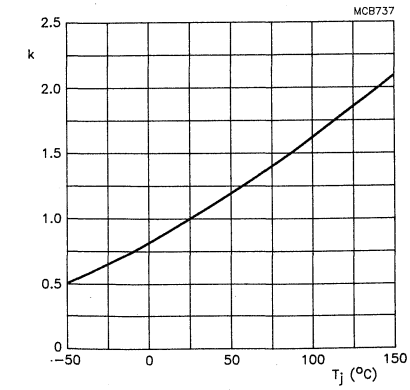


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

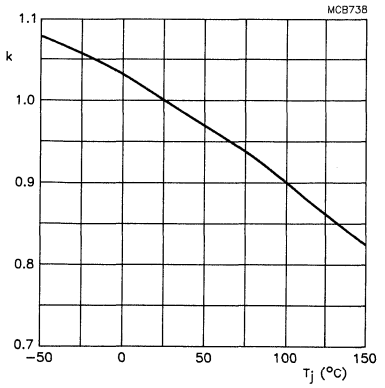
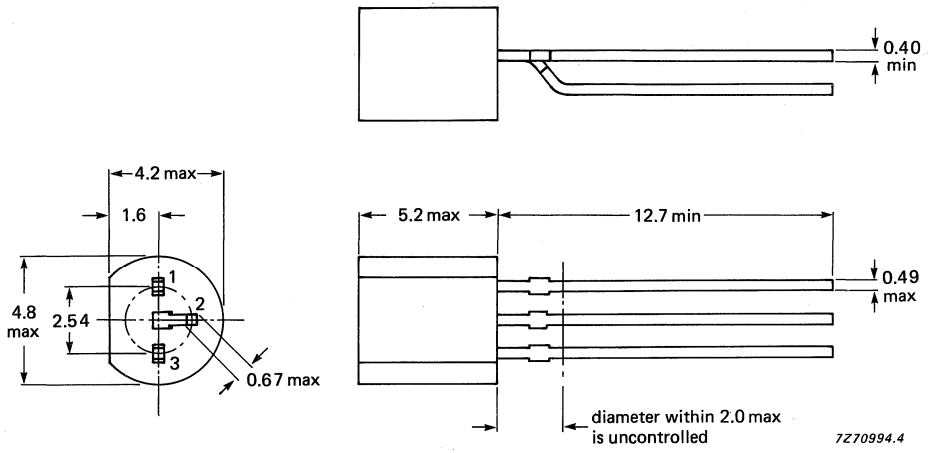


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP204/BSP204A

PACKAGE OUTLINE



Dimensions in mm.

Fig.11 TO-92 variant.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	275 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	10 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA

Fig.1 SOT223.

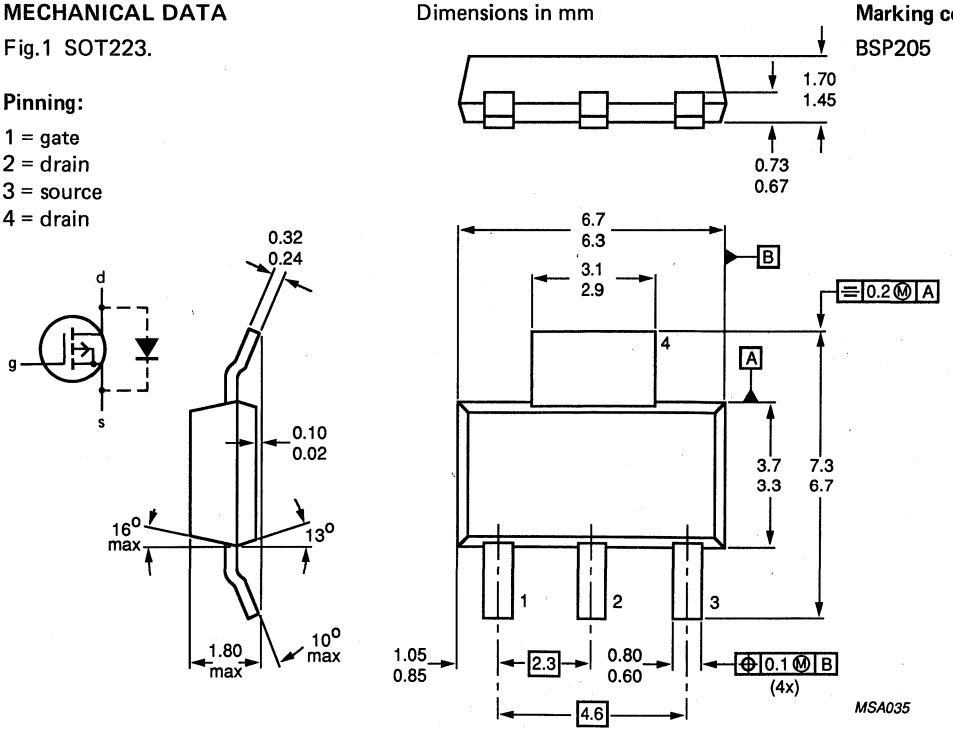
Pinning:

1 = gate
2 = drain
3 = source
4 = drain

Dimensions in mm

Marking code

BSP205



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain current (peak)	$-I_{DM}$	max.	550	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0	μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	60 125	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 45	pF pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	3 6	ns ns
	t_{off}	typ. max.	10 15	ns ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

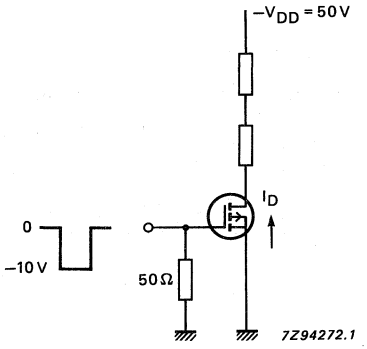


Fig.2 Switching time test circuit.

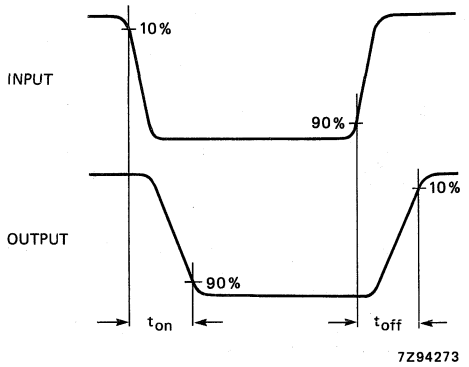


Fig.3 Input and output waveforms.

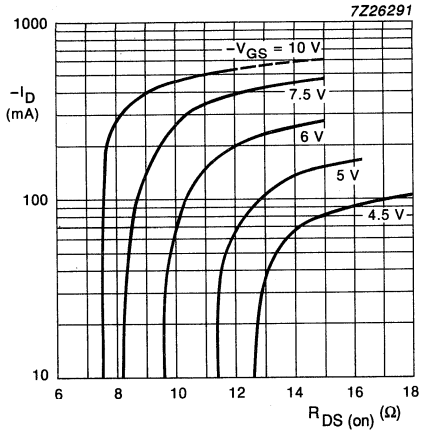


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

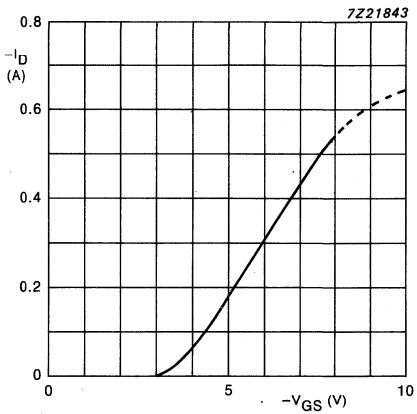


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

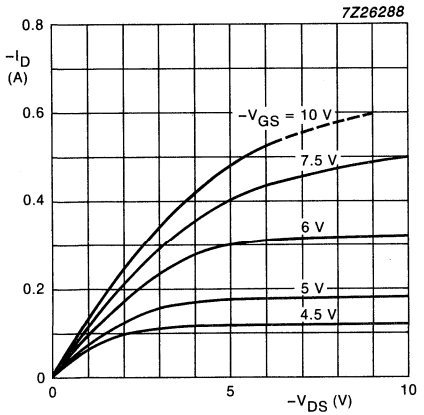


Fig.6 Output characteristics; T_j = 25 °C; typical values.

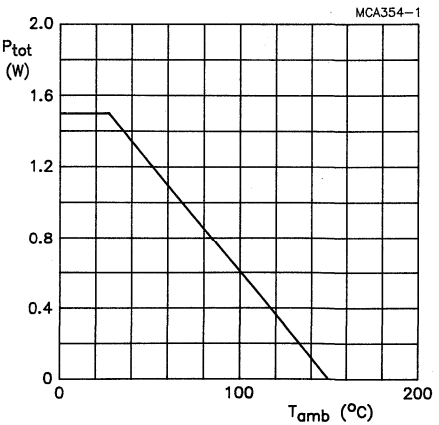


Fig.7 Power derating curve.

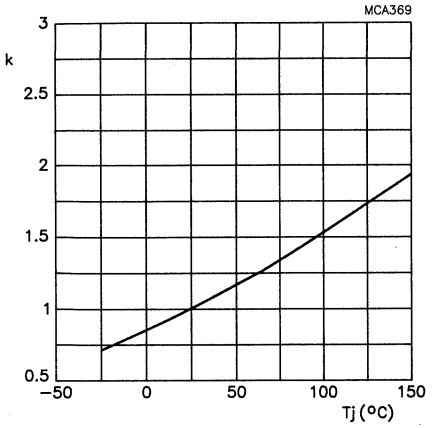


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10 V; typical values.

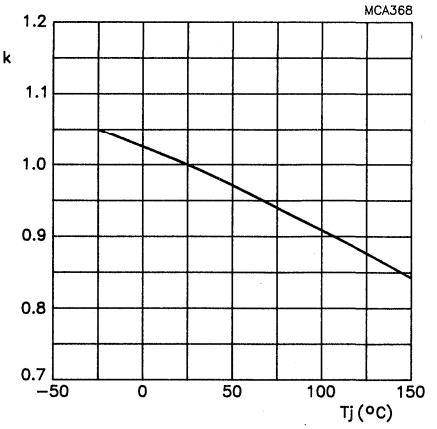


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

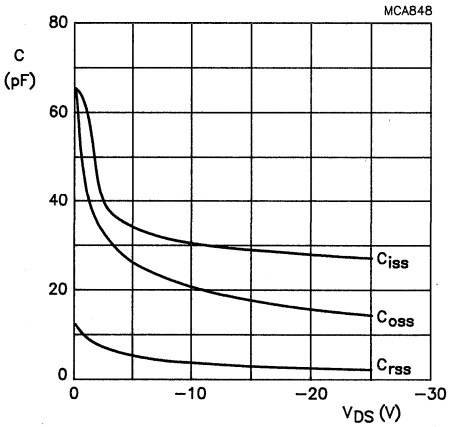


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low $r_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	max.	6 Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5 V

MECHANICAL DATA

Fig.1 SOT223.

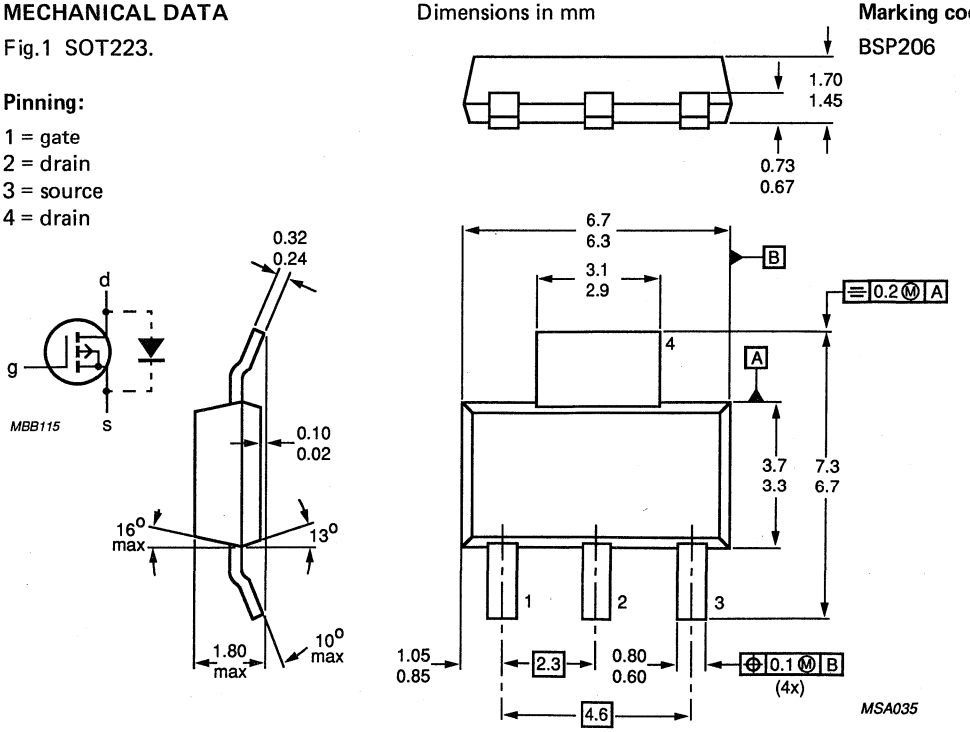
Pinning:

1 = gate
2 = drain
3 = source
4 = drain

Dimensions in mm

Marking code

BSP206



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	350 mA
Drain current (peak)	$-I_{DM}$	max.	700 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0 μA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$r_{DS(on)}$	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	100 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 ns 8 ns
	t_{off}	typ. max.	15 ns 25 ns

Note

1. Device mounted on an epoxy printed-circuit board 40 mm x 40 mm x 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

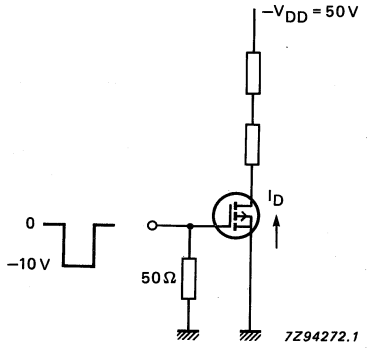


Fig.2 Switching time test circuit.

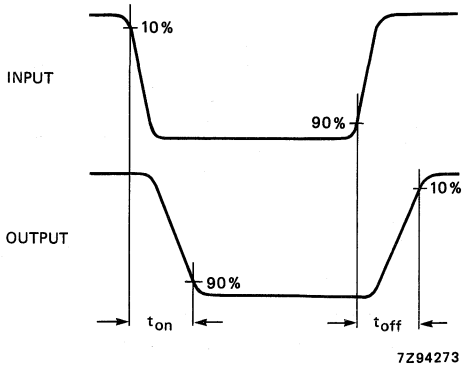


Fig.3 Input and output waveforms.

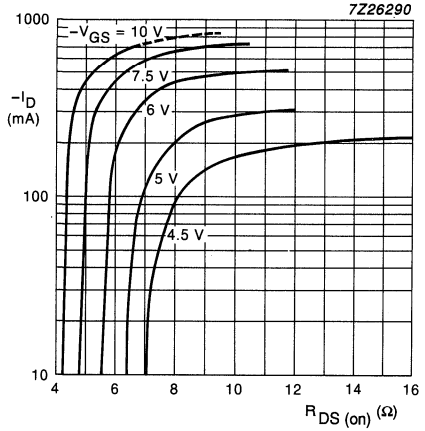


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

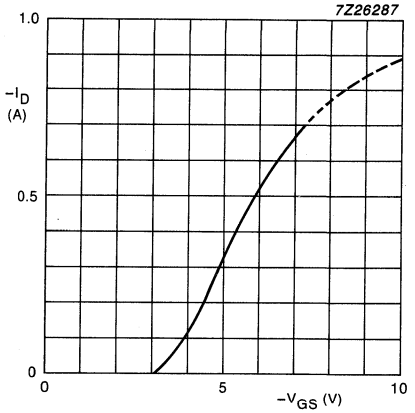


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

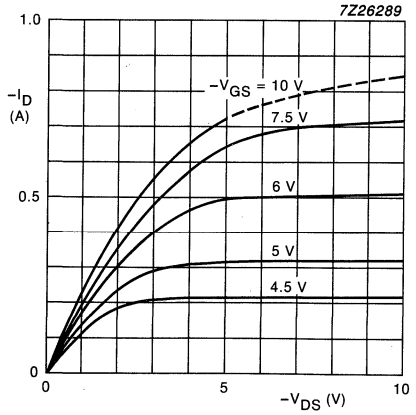


Fig.6 Output characteristics; T_j = 25 °C; typical values.

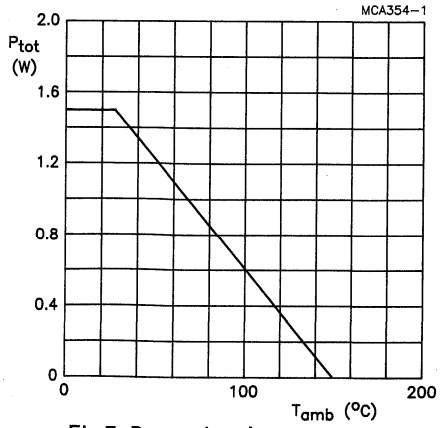


Fig.7 Power derating curve.

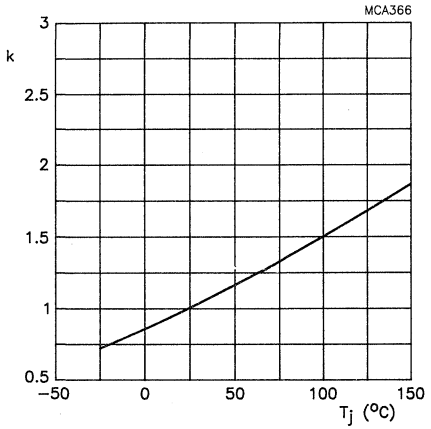


Fig.8 $k = \frac{r_{DS(on)} \text{ at } T_j}{r_{DS(on)} \text{ at } 25\ ^oC}$; at −200 mA/−10V; typical values.

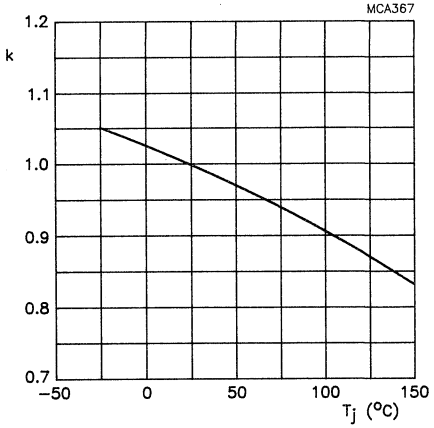


Fig.9 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^oC}$; $-V_{GS(th)}$ at −1 mA; typical values.

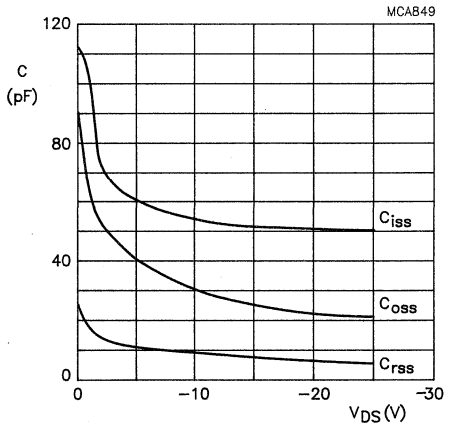


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

Philips Components

Data sheet	
status	Product specification
date of issue	August 1990

BSP220

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	12	Ω
$-V_{GS(th)}$	gate-source threshold voltage		2.8	V

PIN CONFIGURATION

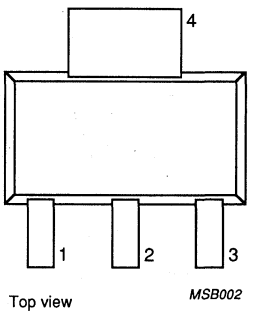


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP220

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP220

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	12	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	20	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP220

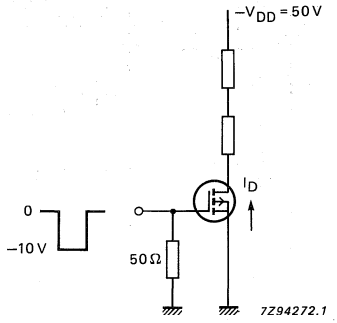


Fig.2 Switching time test circuit.

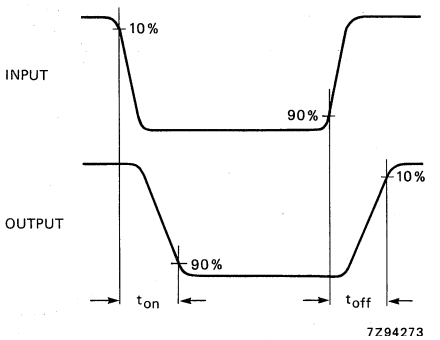


Fig.3 Input and output waveforms.

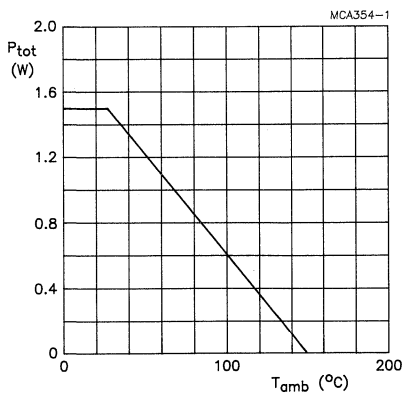


Fig.4 Power derating curve.

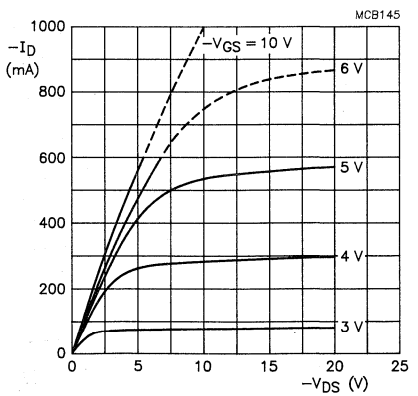


Fig.5 Typical output characteristics; $T_j = 25\,°C$.

P-channel enhancement mode vertical D-MOS transistor

BSP220

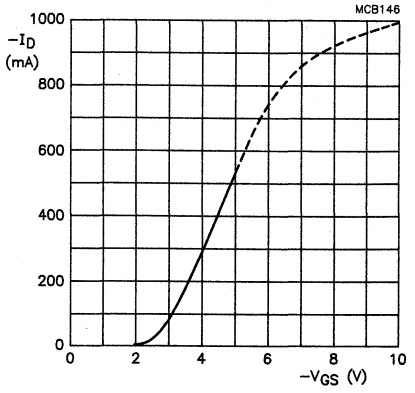


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

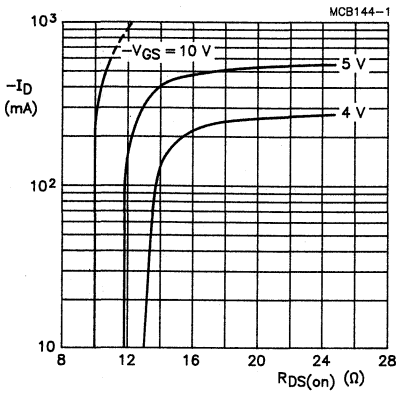


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

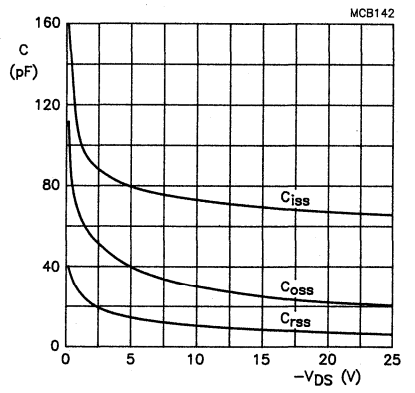


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

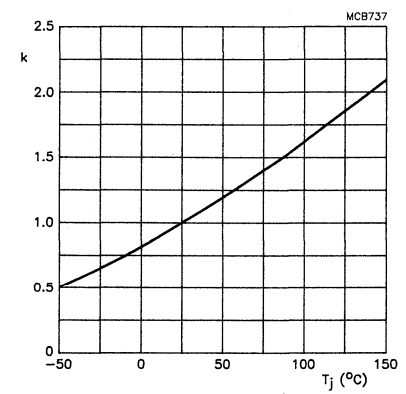


Fig.9 Temperature coefficent of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\,°C}$; typical $R_{DS(on)}$ at –200 mA/–10 V.

P-channel enhancement mode vertical D-MOS transistor

BSP220

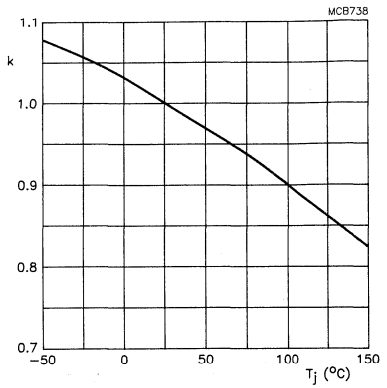
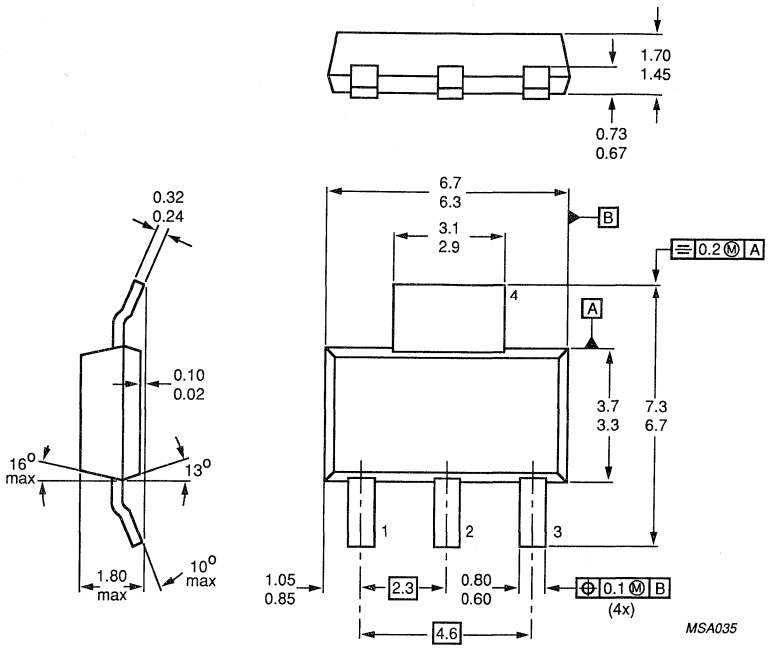


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $-V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP220

PACKAGE OUTLINE



Dimensions in mm.

Marking code: BSP220.

Fig.11 SOT223.

Data sheet	
status	Product specification
date of issue	November 1990

BSP225

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

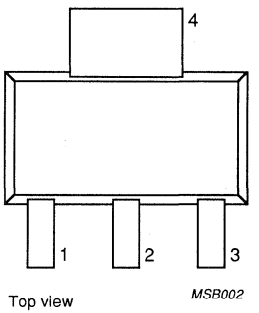


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSP225

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm².

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm².

P-channel enhancement mode vertical D-MOS transistor

BSP225

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSP225

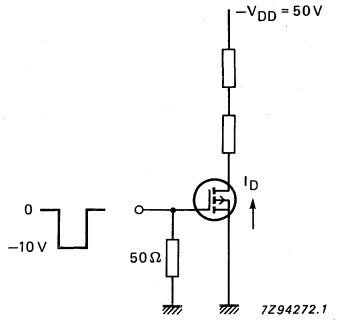


Fig.2 Switching time test circuit.

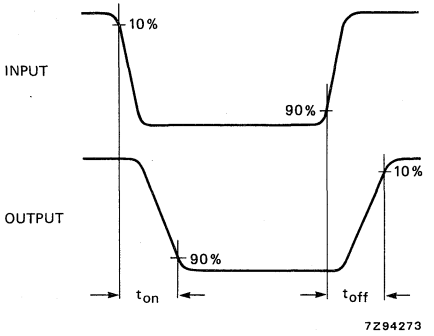


Fig.3 Input and output waveforms.

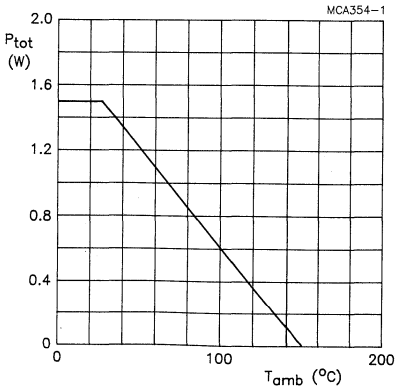


Fig.4 Power derating curve.

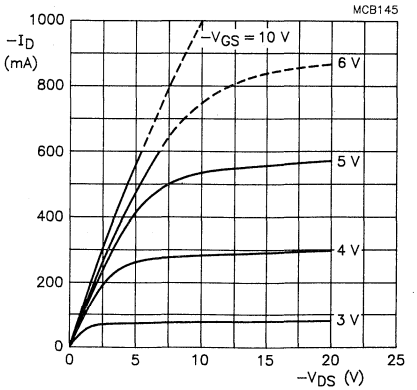


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP225

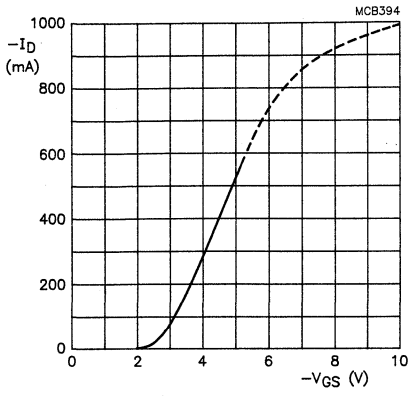


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

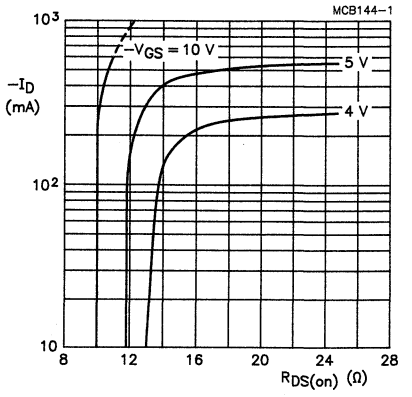


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C; $R_{DS(on)} = f(I_D)$.

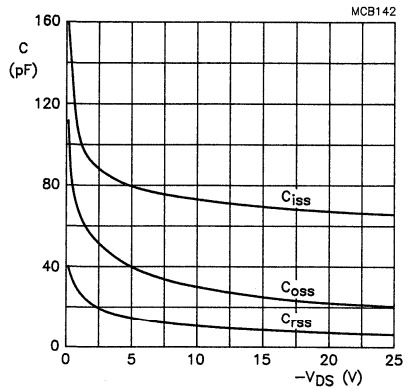


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

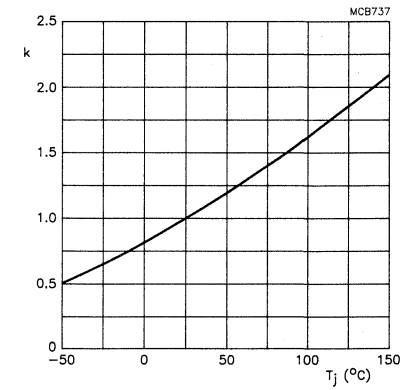


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V.

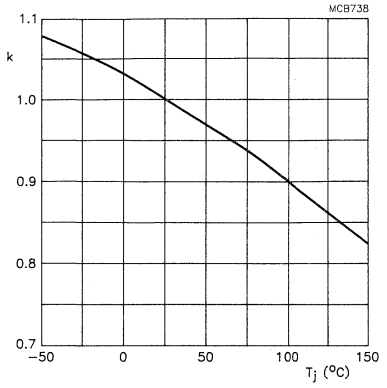
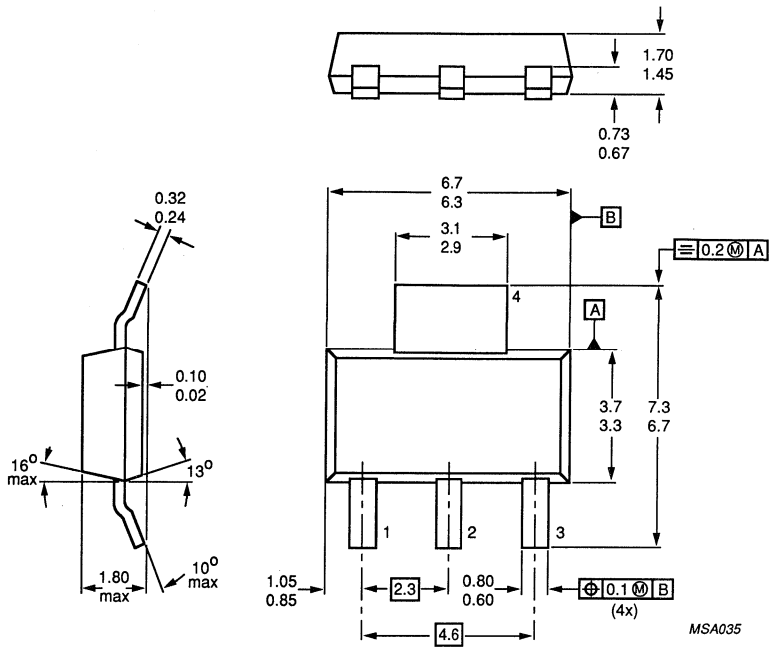


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP225

PACKAGE OUTLINE



Dimensions in mm.

Marking code: BSP225.

Fig.11 SOT223.

Philips Components

Data sheet	
status	Product specification
date of issue	February 1991

BSP254/BSP254A

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

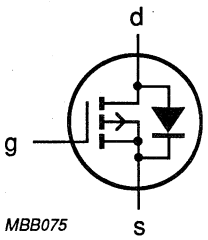


Fig.1 Symbol.

PINNING - TO-92 variant (BSP254)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP254A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain-current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	1	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	20	V
$-I_D$	drain current	DC	-	0.2	A
$-I_{DM}$	drain current	peak value	-	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{thj\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

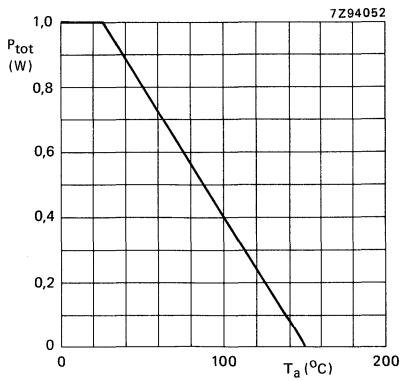


Fig.2 Power derating curve.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 µA	250	-	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	-	-	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	-	-	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	V_{GS} = V_{DS} $-I_D$ = 1 mA	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	-	mS
C_{iss}	input capacitances	note 1	-	65	90	pF
C_{oss}	output capacitance	note 1	-	20	30	pF
C_{rss}	feedback capacitance	note 1	-	6	15	pF
t_{on}	turn-on time	note 2	-	5	10	ns
t_{off}	turn-off time	note 2	-	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

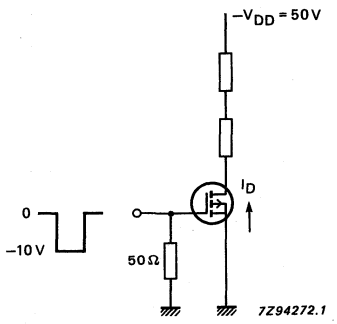


Fig.3 Switching times test circuit.

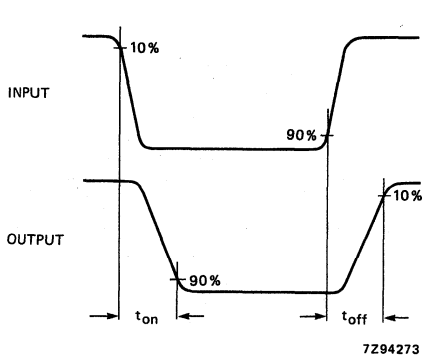


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

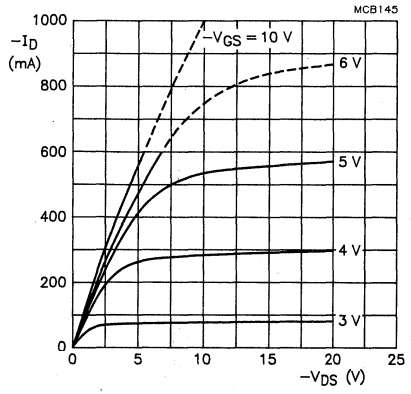


Fig.5 Typical output characteristics; T_j = 25 °C.

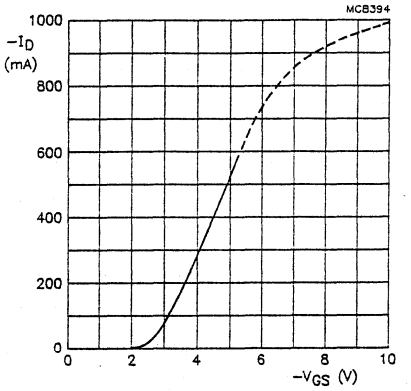


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

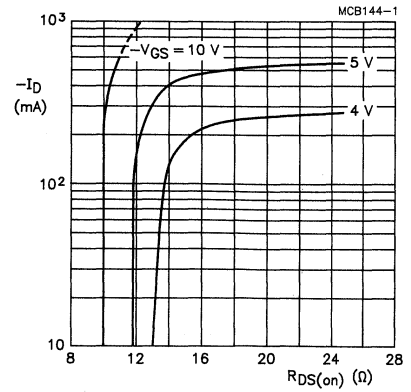


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

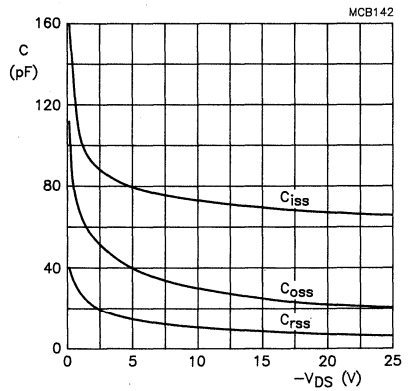


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

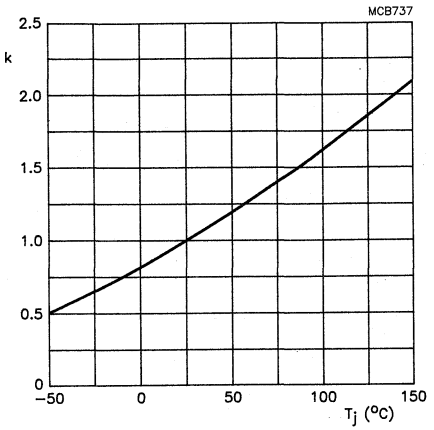


Fig.9 $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at −200 mA/−10 V;

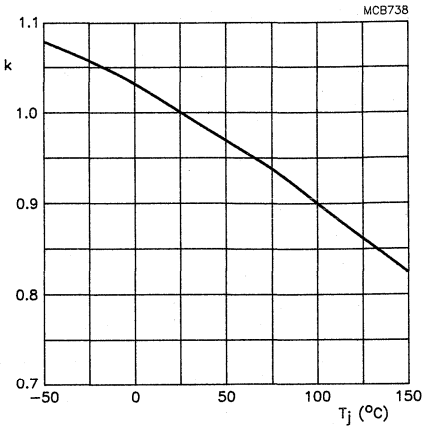


Fig.10 $k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP254/BSP254A

PACKAGE OUTLINE

Dimensions in mm

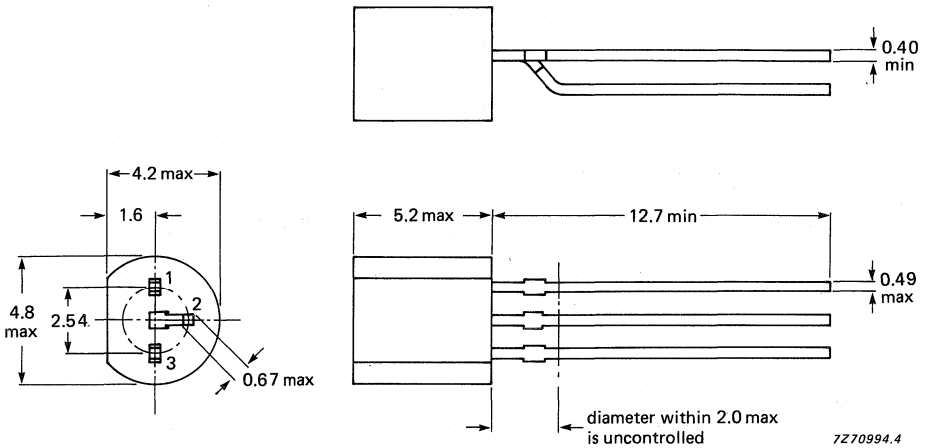


Fig.11 TO-92 variant.

Data sheet	
status	Preliminary specification
date of issue	February 1991

BSS84

P-channel enhancement mode vertical D-MOS FET

DESCRIPTION

Silicon p-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION

Fig.1 Symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	50	V
$-I_D$	drain current	130	mA
$R_{DS(on)}$	drain-source on resistance	10	Ω
$-V_{GS(th)}$	gate-source threshold voltage	2	V

P-channel enhancement mode vertical D-MOS FET

BSS84

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	50	V
$-V_{GSO}$	gate-source voltage	open drain $I_D = 0$	-	20	V
$-I_D$	drain current	average value	-	130	mA
$-I_{DM}$	drain current	peak value	-	520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

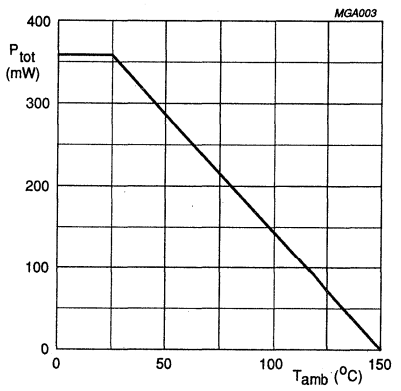


Fig.2 Total power dissipation as a function of ambient temperature.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	500	K/W

P-channel enhancement mode vertical D-MOS FET

BSS84

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

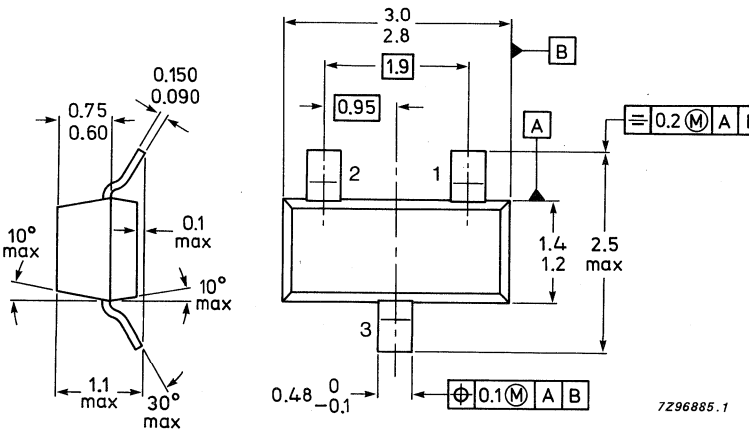
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 $-I_D$ = 250 µA	50	-	-	V
$-I_{DSS}$	drain-source leakage current	V_{GS} = 0 $-V_{DS}$ = 25 V	-	-	0.1	µA
		V_{GS} = 0 $-V_{DS}$ = 50 V	-	-	15	µA
		V_{GS} = 0 $-V_{DS}$ = 50 V T_j = 125 °C	-	-	60	µA
$-I_{GSS}$	gate-source leakage current	V_{DS} = 0 $-V_{GS}$ = 20 V	-	-	60	µA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{DS} = V_{GS}	0.8	-	2	V
$R_{DS(on)}$	drain-source on resistance	$-V_{GS}$ = 5 V $-I_D$ = 100 mA	-	6	10	Ω
$\|y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 100 mA f = 1 kHz	50	70	-	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	40	-	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	15	-	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	-	6	-	pF
t_{on}	turn-on time	$-V_{CC}$ = 30 V $-I_D$ = 0.27 A $-V_{GS}$ = 0/5 V	-	20	-	ns
t_{off}	turn-off time	$-V_{CC}$ = 30 V $-I_D$ = 0.27 A $-V_{GS}$ = 0/5 V	-	43	-	ns

P-channel enhancement mode vertical D-MOS FET

BSS84

PACKAGE OUTLINE

Dimensions in mm



TOP VIEW

Marking: SP

Fig.3 SOT23.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in a SOT89 envelope.
Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	max. typ.	6 Ω 4.5 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ. min.	350 mS 140 mS

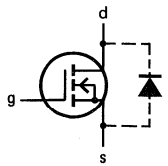
MECHANICAL DATA

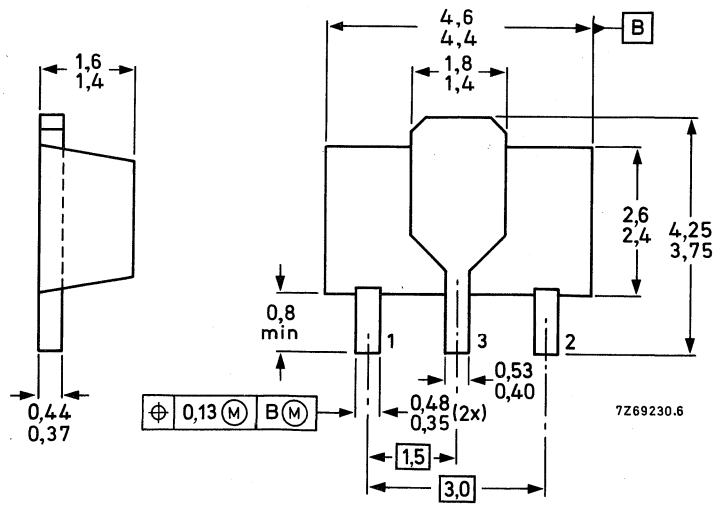
Dimensions in mm

Fig. 1 SOT89.

Pinning

1 = source
2 = gate
3 = drain





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BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	280 mA
Drain current (peak)	I_{DM}	max.	1.1 A
Total power dissipation up to T_{amb} = 25 °C *	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient *	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0 V_{DS} = 200 V; V_{GS} = 0	I_{DSS} I_{DSS}	max. max. typ.	200 nA 60 μA 100 nA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max. typ.	6 Ω 4.5 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	typ. min.	350 mS 140 mS
Input capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max. typ.	60 pF 45 pF
Output capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max. typ.	25 pF 15 pF
Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max. typ.	10 pF 3.5 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10	t_{on} t_{off}	typ. max. typ. max.	5 ns 10 ns 15 ns 25 ns

* Transistor mounted on ceramic substrate area 2.5 cm^2, thickness 0.7 mm.

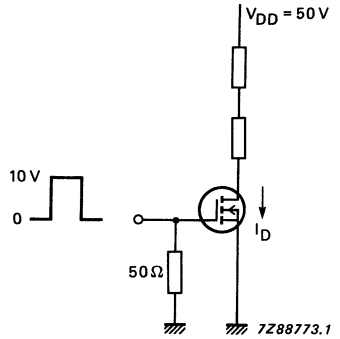


Fig. 2 Switching times test circuit.

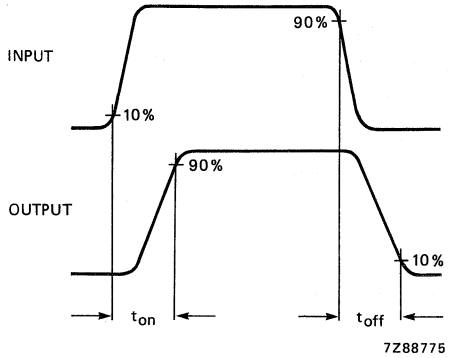


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

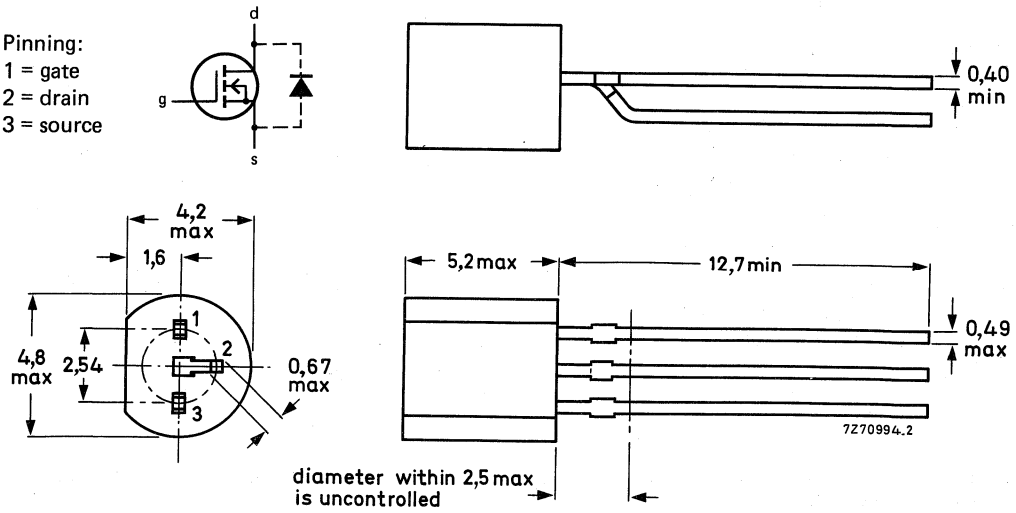
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 mS 350 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−55 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 250 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ. max.	100 60	nA μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 6	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	140 350	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 15	ns ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

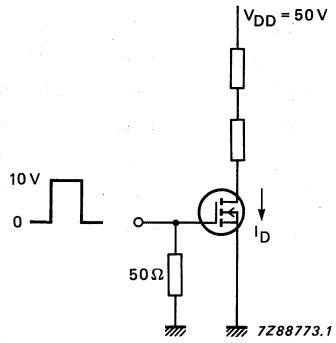


Fig. 2 Switching time test circuit.

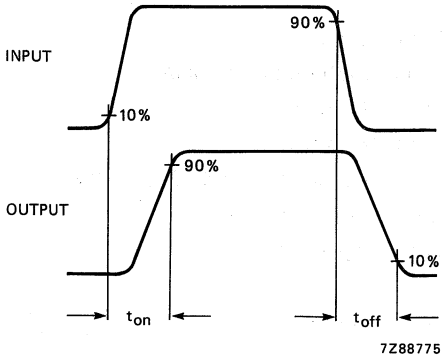


Fig. 3 Input and output waveforms.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-18 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.5 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6.0 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	140 mS 350 mS

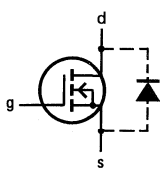
MECHANICAL DATA

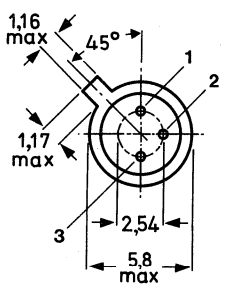
Dimensions in mm

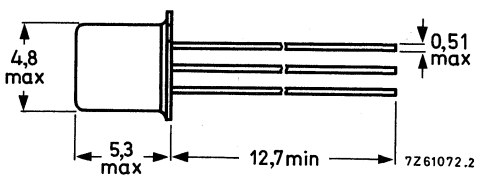
Fig. 1 TO-18.

Pinning

1 = source
2 = gate
3 = drain







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	350 mA
Drain current (peak)	I_{DM}	max.	1.4 A
Total power dissipation up to			
T_{amb} = 25 °C	P_{tot}	max.	0.4 W
T_{case} = 25 °C	P_{tot}	max.	1.5 W
Storage temperature range	T_{stg}	−55 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	310 K/W
From junction to case	$R_{th\ j\text{-}c}$	=	83 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current			
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200 nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	typ.	100 nA
		max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	2.8 V
Drain-source ON-resistance			
I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ.	4.5 Ω
		max.	6.0 Ω
Transfer admittance			
I_D = 400 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	140 mS
		typ.	350 mS
Input capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45 pF
		max.	60 pF
Output capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15 pF
		max.	25 pF
Feedback capacitance at f = 1 MHz;			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	15 ns
	t_{off}	typ.	15 ns
		max.	25 ns

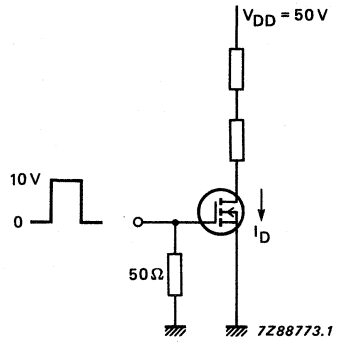


Fig. 2 Switching time test circuit.

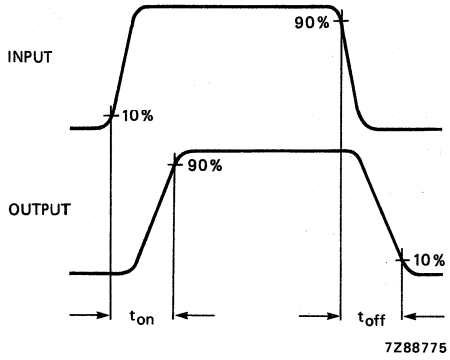


Fig. 3 Input and output waveforms.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

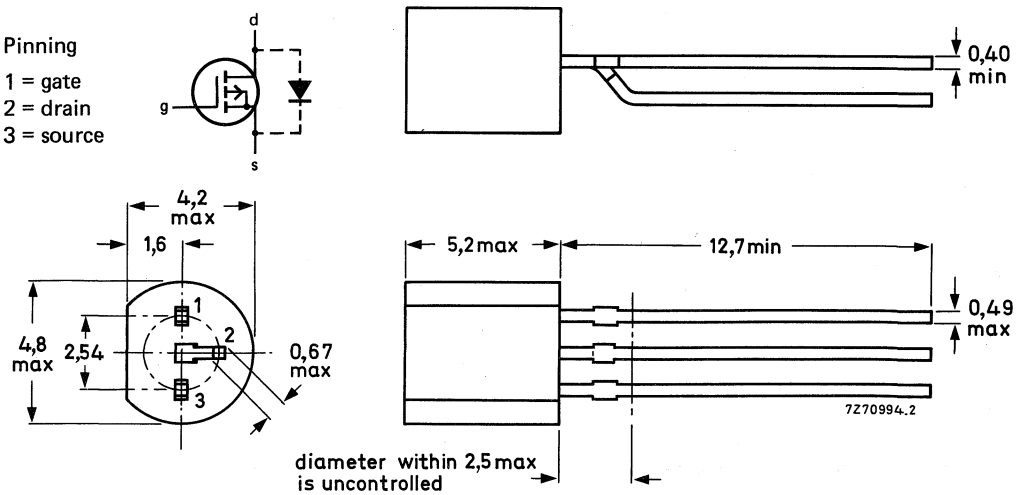
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 mS 200 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Drain current (peak)	$-I_{DM}$	max.	0.6 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−55 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 250 μA; $-V_{GS}$ = 0	$-V_{(BR)DS}$	min.	200 V
Drain-source leakage current $-V_{DS}$ = 60 V; $-V_{GS}$ = 0 $-V_{DS}$ = 200 V; $-V_{GS}$ = 0	$-I_{DSS}$ $-I_{DSS}$	max. max.	0.2 μA 60 μA
Gate-source leakage current $-V_{GS}$ = 20 V; $-V_{DS}$ = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\lvert y_{fs} \rvert$	min. typ.	60 mS 200 mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{iss}	typ.	65 pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{oss}	typ.	20 pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 25 V; $-V_{GS}$ = 0	C_{rss}	typ.	6 pF
Switching times (see Figs 2 and 3) $-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 ns 20 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

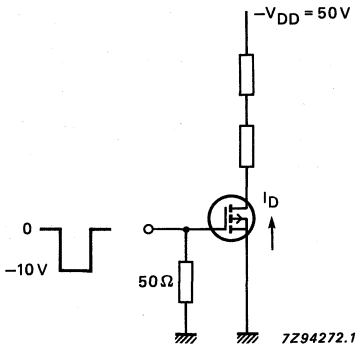


Fig. 2 Switching time test circuit.

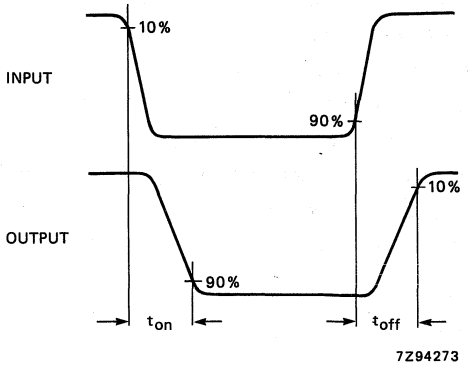


Fig. 3 Input and output waveforms.

Philips Components

Data sheet	
status	Product specification
date of issue	November 1990

BSS100

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION

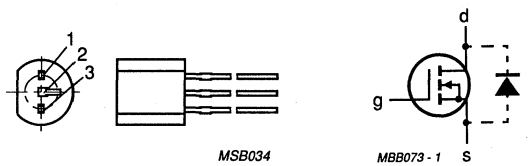


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS100

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	250	mA
I_{DM}	drain current	peak value	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150	K/W

Note

1. Transistor mounted on a printed circuit board, maximum lead length 4 mm, mounting pad for the drain lead 10 mm^2.

N-channel enhancement mode vertical D-MOS transistor

BSS100

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSS100

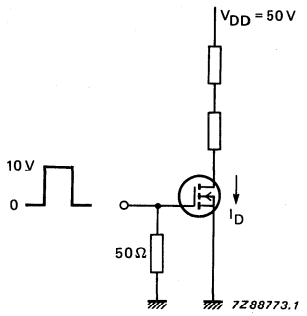


Fig.2 Switching time test circuit.

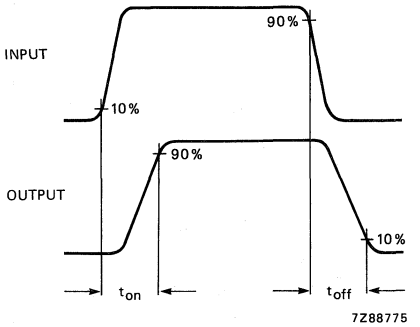
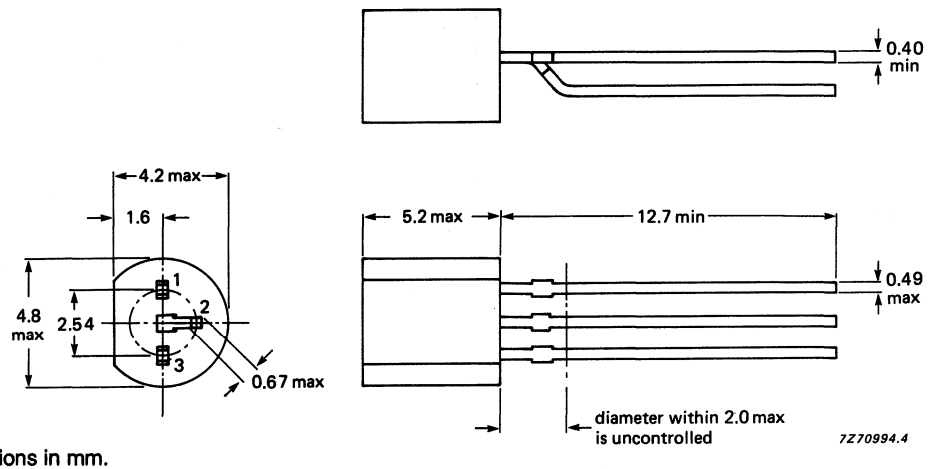


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS100

PACKAGE OUTLINE



Dimensions in mm.

Fig.4 TO-92 variant.

Philips Components

Data sheet	
status	Product specification
date of issue	November 1990

BSS123

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

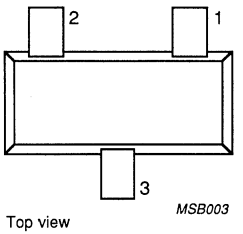
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION



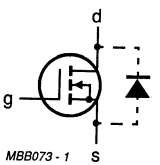


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSS123

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

N-channel enhancement mode vertical D-MOS transistor

BSS123

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSS123

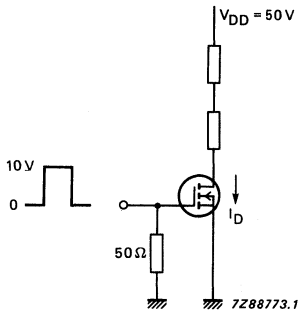


Fig.2 Switching time test circuit.

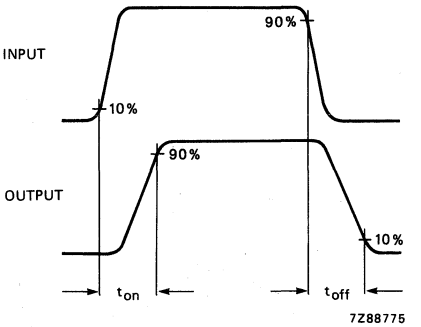
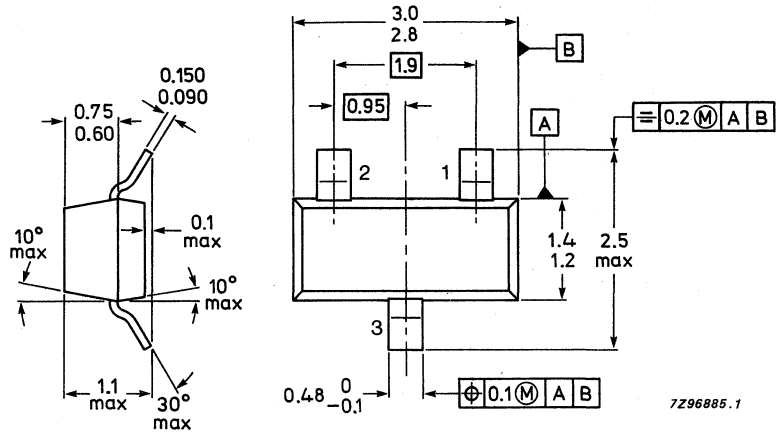


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS123

PACKAGE OUTLINE



TOP VIEW

Dimensions in mm.

Fig.4 SOT23.

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

BSS131

N-channel enhancement mode vertical D-MOS FET

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

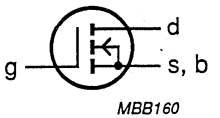
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	100	mA
$R_{DS(on)}$	drain-source on resistance	16	Ω
$-V_{GS(th)}$	gate-source threshold voltage	2.8	V

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

PIN CONFIGURATION



MBB160

Fig.1 Symbol.

N-channel enhancement mode vertical D-MOS FET

BSS131

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	100	mA
I_{DM}	drain current	peak value	-	400	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

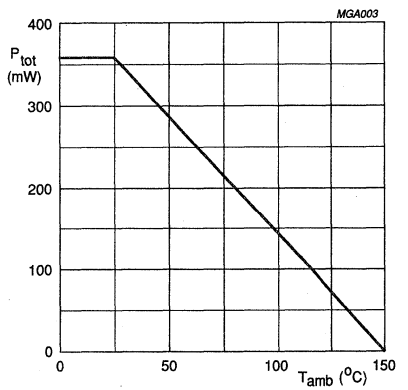


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel enhancement mode vertical D-MOS FET

BSS131

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

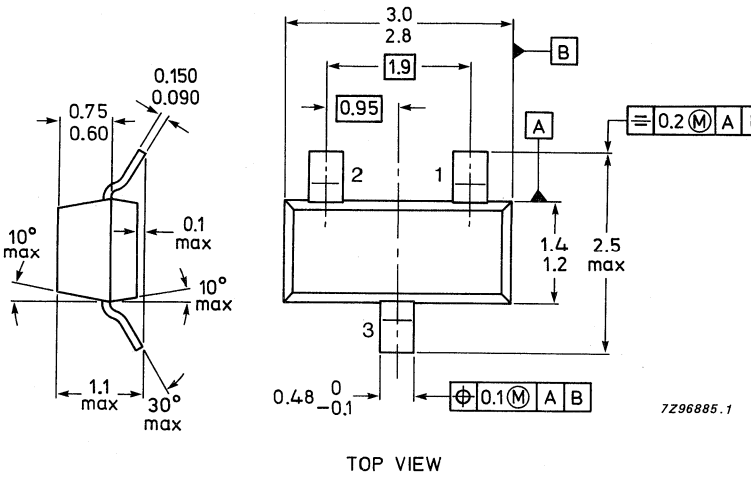
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 µA	240	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 130 V	-	-	30	nA
		V_{GS} = 0 V_{DS} = 240 V	-	-	15	µA
		V_{GS} = 0 V_{DS} = 240 V T_j = 125 °C	-	-	60	µA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	-	2.8	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 10 V I_D = 100 mA	-	-	16	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 100 mA f = 1 kHz	60	100	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	20	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	6	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	2.5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	20	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0-5 V	-	40	-	ns

N-channel enhancement mode vertical D-MOS FET

BSS131

PACKAGE OUTLINE

Dimensions in mm



TOP VIEW

Marking: SR

Fig.3 SOT23.

Data sheet	
status	Preliminary specification
date of issue	September 1990

BSS138

N-channel enhancement mode vertical D-MOS FET

FEATURES

- Low threshold voltage
- CMOS compatible
- Low on-resistance.

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is intended for use in general purpose and high-speed switching applications, such as relays, multiplexers, choppers and line transformer drivers.

PIN CONFIGURATION

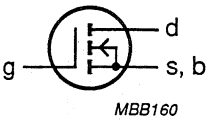


Fig.1 Symbol.

PINNING - SOT223

PIN	DESCRIPTION
1	source, substrate (b)
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	drain current	200	mA
$R_{DS(on)}$	drain-source on resistance	3.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.5	V

N-channel enhancement mode vertical D-MOS FET

BSS138

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	50	V
V_{GSO}	gate-source voltage	open drain $I_D = 0$	-	20	V
I_D	drain current	average value	-	200	mA
I_{DM}	drain current	peak value	-	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	-	360	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	350	K/W

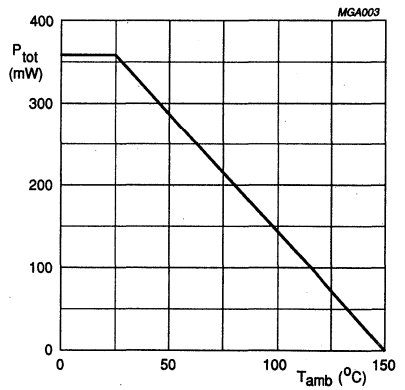


Fig.2 Total power dissipation as a function of ambient temperature.

N-channel enhancement mode vertical D-MOS FET

BSS138

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

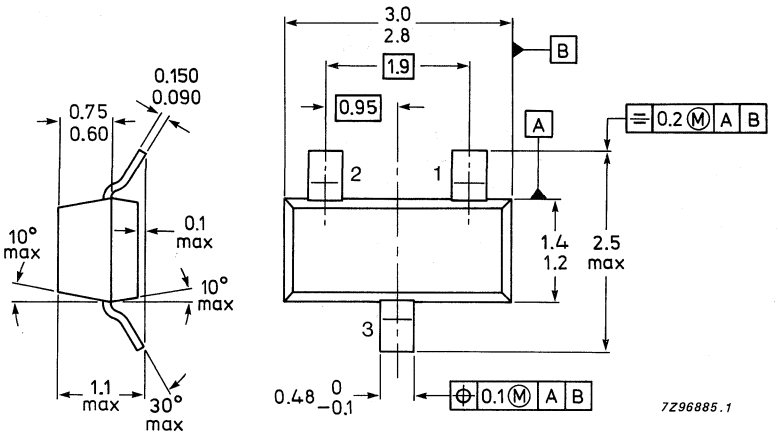
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 250 μA	50	-	-	V
I_{DSS}	drain-source leakage current	V_{GS} = 0 V_{DS} = 25 V	-	-	0.1	μA
		V_{GS} = 0 V_{DS} = 50 V	-	-	0.5	μA
		V_{GS} = 0 V_{DS} = 50 V T_j = 125 °C	-	-	5	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0 V_{GS} = 20 V	-	-	0.1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.5	-	1.5	V
$R_{DS(on)}$	drain-source on resistance	V_{GS} = 5 V I_D = 200 mA	-	2	3.5	Ω
$\|Y_{fs}\|$	transfer admittance	V_{DS} = 25 V I_D = 200 mA f = 1 kHz	100	200	-	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	40	-	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	12	-	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	-	5	-	pF
t_{on}	turn-on time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	16	-	ns
t_{off}	turn-off time	V_{CC} = 30 V I_D = 0.28 A V_{GS} = 0/5 V	-	40	-	ns

N-channel enhancement mode vertical D-MOS FET

BSS138

PACKAGE OUTLINE

Dimensions in mm



TOP VIEW

Marking: SS

Fig.3 SOT23.

Philips Components

Data sheet	
status	Product specification
date of issue	October 1990

BSS192

P-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 envelope, intended for use in relay, high-speed and line transformer drivers, and as a line current interruptor in telephony applications.

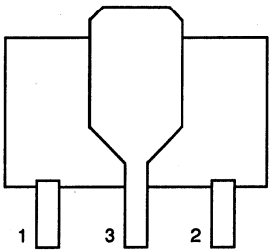
PINNING - SOT89

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 100 mA $-V_{GS}$ = 10 V	20	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION



Bottom view MSB013

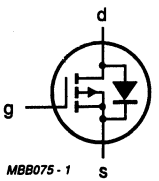


Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BSS192

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	150	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm², thickness 0.7 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on a ceramic substrate, area 2.5 cm², thickness 0.7 mm.

P-channel enhancement mode vertical D-MOS transistor

BSS192

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 60 V V_{GS} = 0	–	–	0.2	μA
		$-V_{DS}$ = 200 V $-V_{GS}$ = 0.2 V	–	0.1	60	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 100 mA $-V_{GS}$ = 10 V	–	10	20	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	60	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

P-channel enhancement mode vertical D-MOS transistor

BSS192

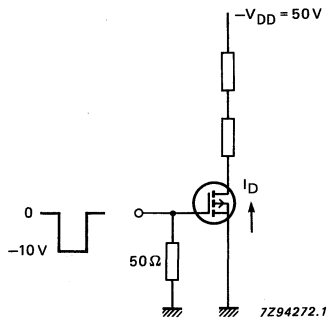


Fig.2 Switching time test circuit.

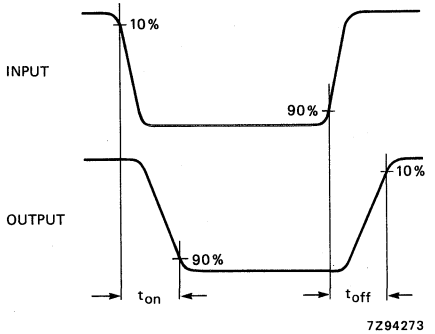


Fig.3 Input and output waveforms.

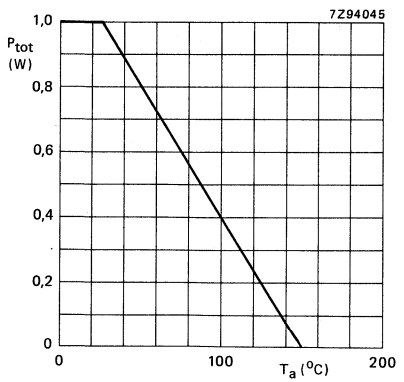


Fig.4 Power derating curve.

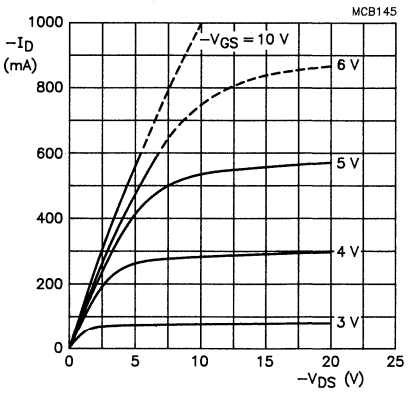


Fig.5 Typical output characteristics; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BSS192

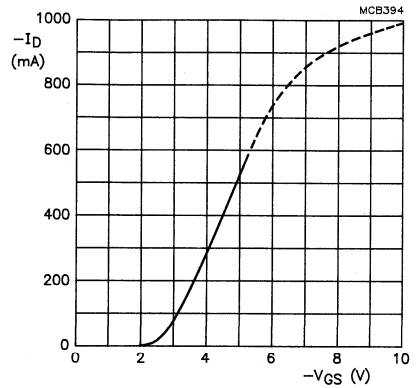


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

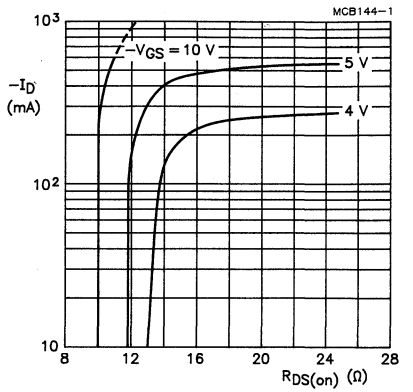


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

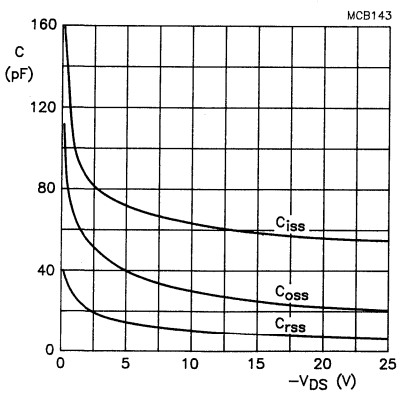


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

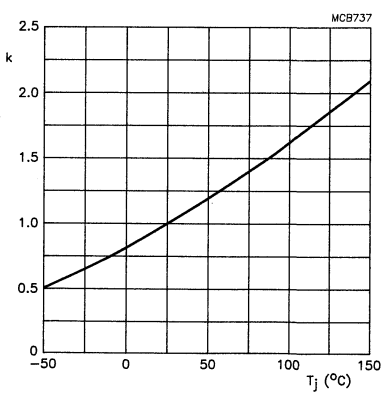


Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$ at –200 mA/–10 V.

P-channel enhancement mode vertical D-MOS transistor

BSS192

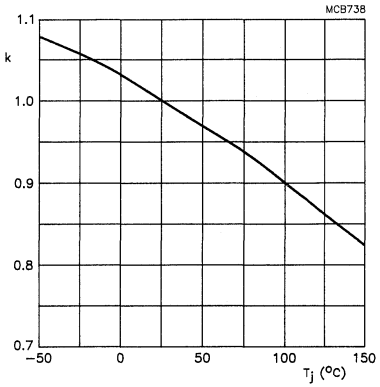
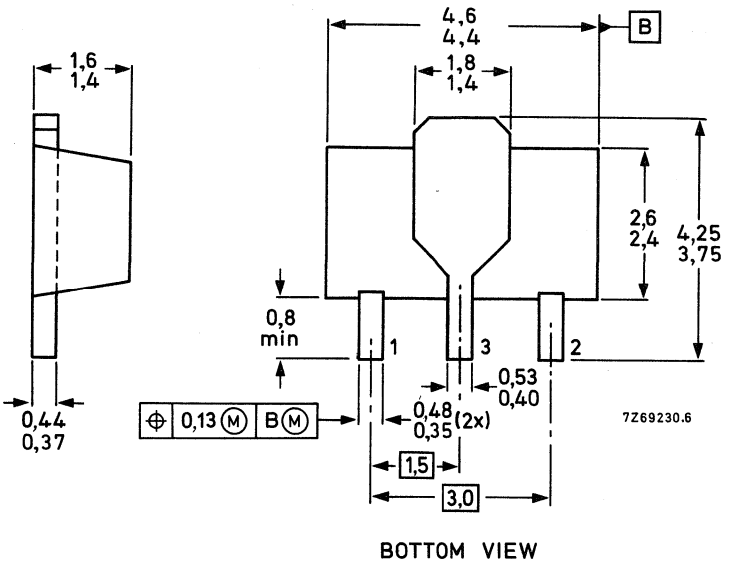


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{-V_{GS(th)}\ at\ T_j}{-V_{GS(th)}\ at\ 25\ °C}$; typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSS192

PACKAGE OUTLINE



Dimensions in mm.

Fig.11 SOT89.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2 Ω 4 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\|y_{fs}\|$	typ.	300 mS

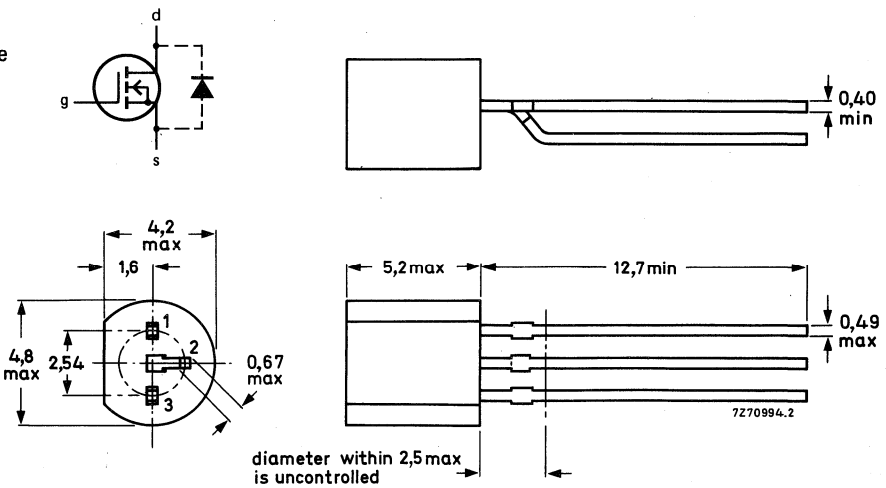
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig. 4) I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

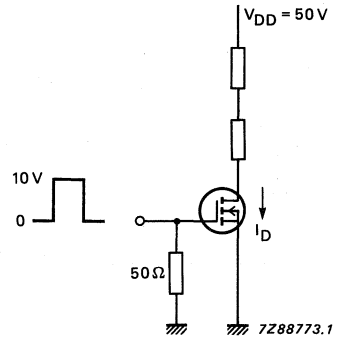


Fig. 2 Switching times test circuit.

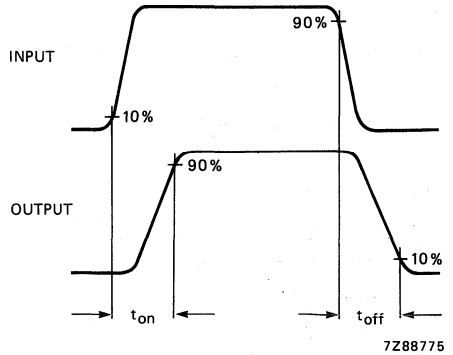


Fig. 3 Input and output waveforms.

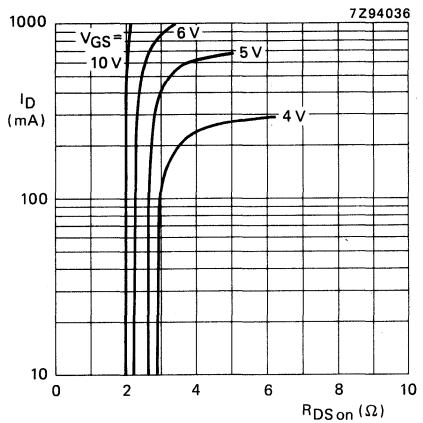


Fig. 4 T_j = 25 °C; typical values.

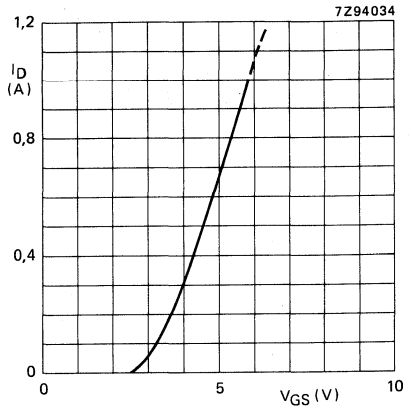


Fig. 5 T_j = 25 °C; typical values at V_{DS} = 10 V.

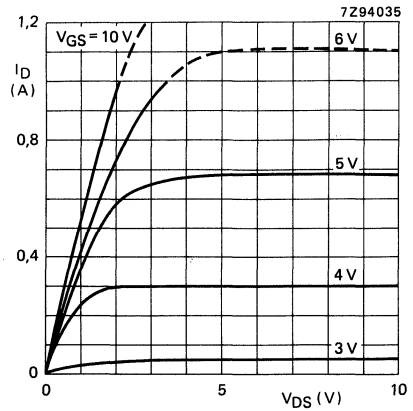


Fig. 6 T_j = 25 °C; typical values.

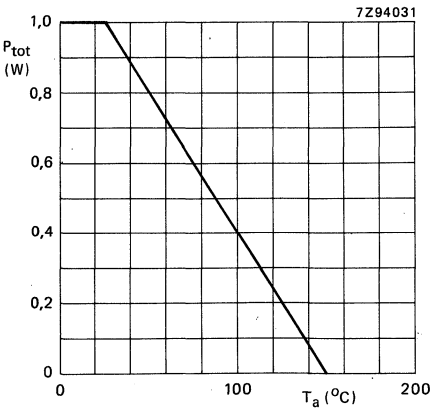


Fig. 7 Power derating curve.

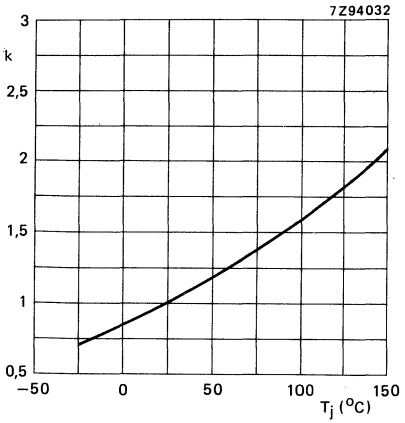


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 500 mA/10 V.

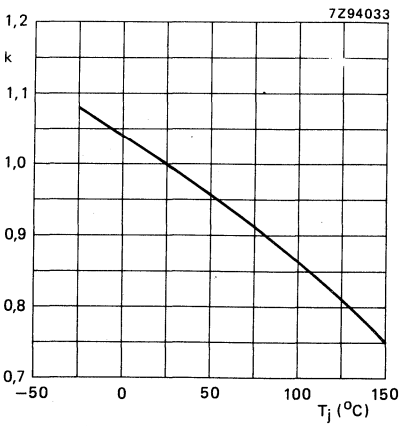


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

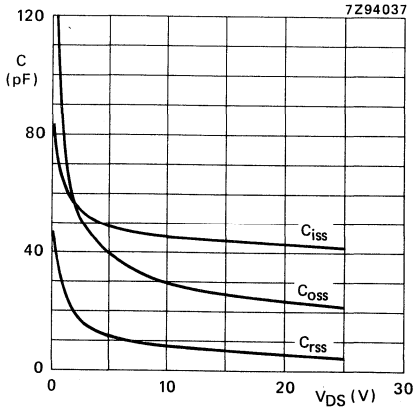


Fig. 10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150	mS

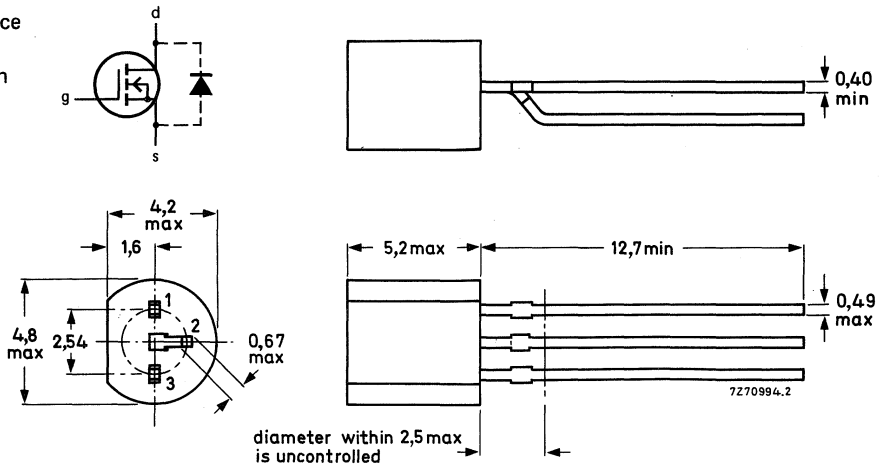
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance (see Fig. 4) I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 pF 6 pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

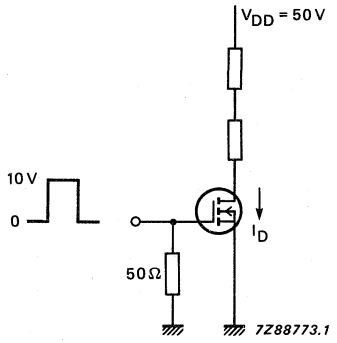


Fig. 2 Switching times test circuit.

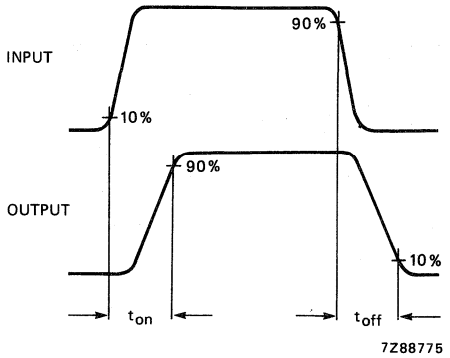


Fig. 3 Input and output waveforms.

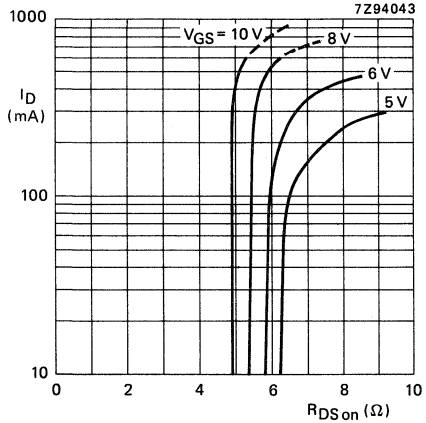


Fig. 4 T_j = 25 °C; typical values.

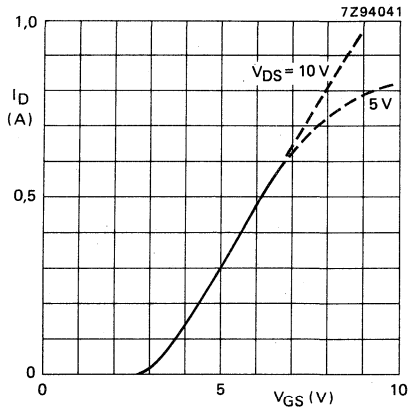


Fig. 5 T_j = 25 °C; typical values.

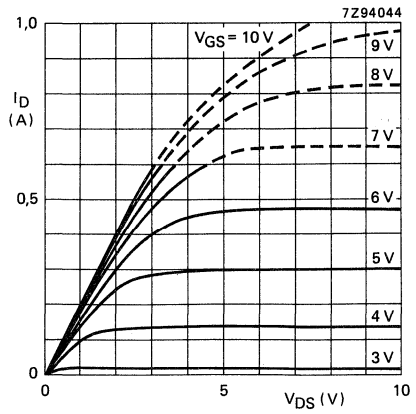


Fig. 6 T_j = 25 °C; typical values.

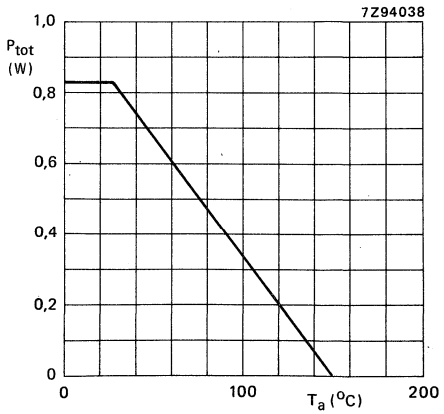


Fig. 7 Power derating curve.

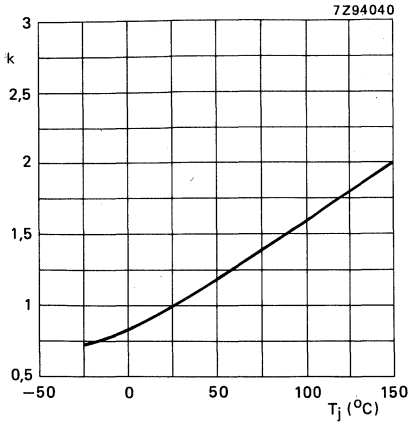


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; typ. values at 150 mA/5 V.

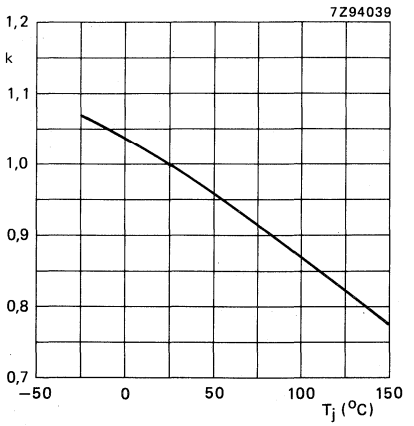


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

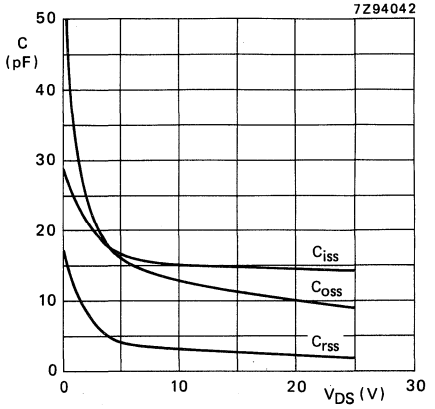


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

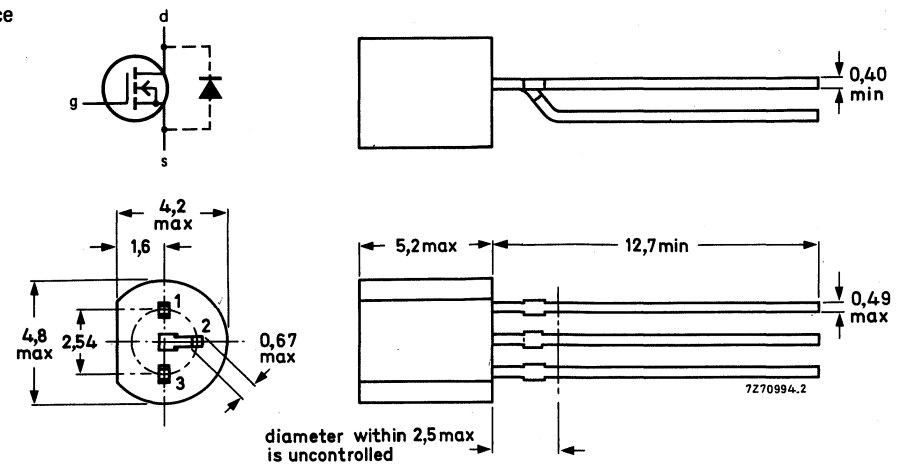
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200 V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 V 2.8 V
Drain-source ON-resistance (see Fig. 4) I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 pF 90 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4 ns
		max.	10 ns
	t_{off}	typ.	15 ns
		max.	25 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm x 10 mm.

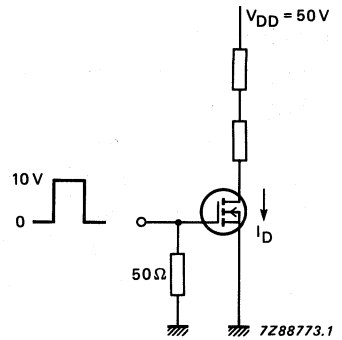


Fig. 2 Switching times test circuit.

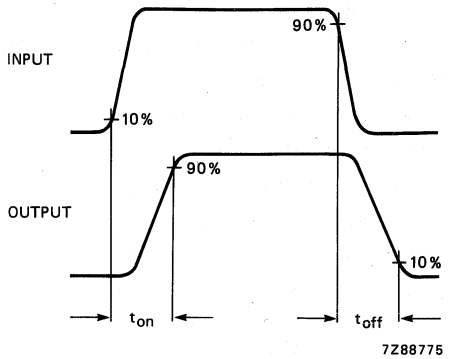


Fig. 3 Input and output waveforms.

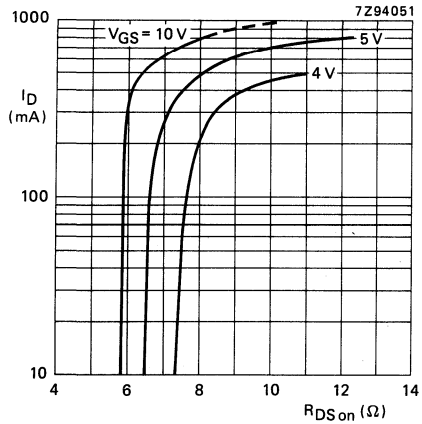


Fig. 4 T_j = 25 °C; typical values.

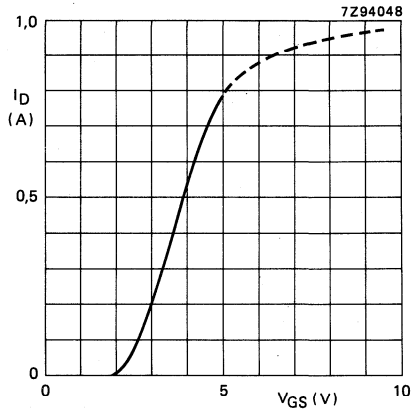


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

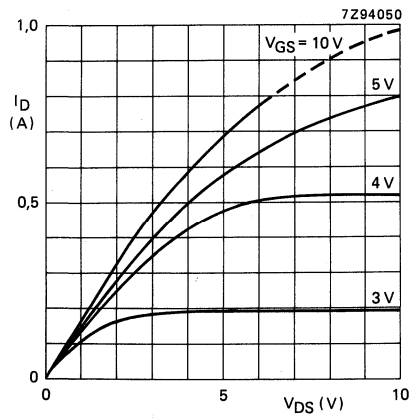


Fig. 6 T_j = 25 °C; typical values.

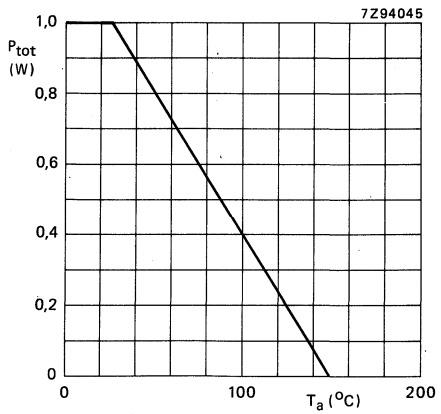


Fig. 7 Power derating curve.

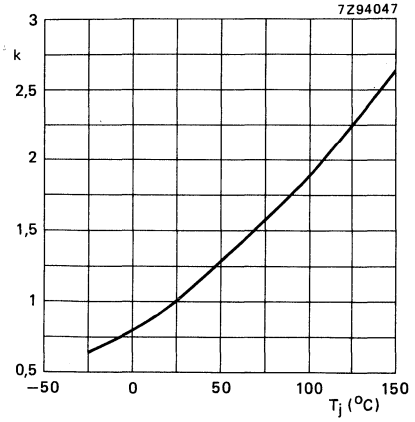


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; at 400 mA/10 V; typical values.

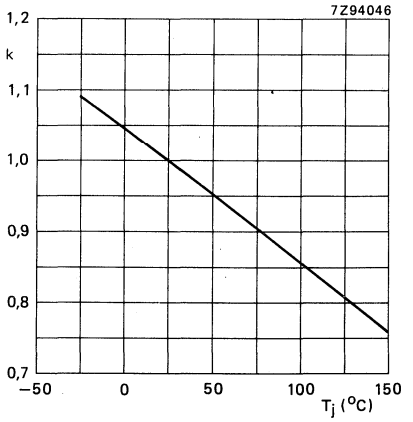


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

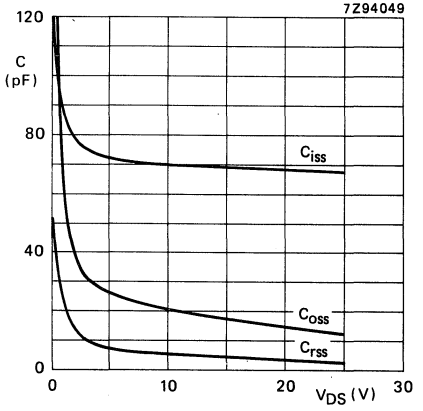


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25\ ^oC$	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250 mS

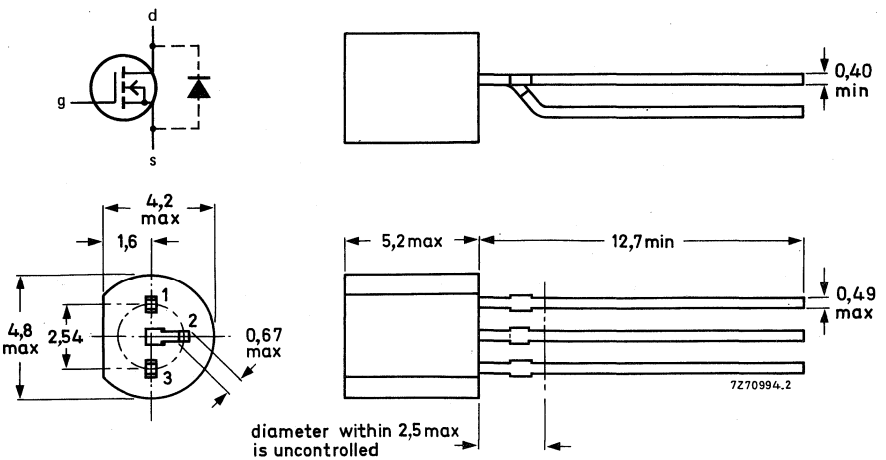
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180 V
Drain-source leakage current V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.7 V 2.4 V
Drain-source ON-resistance (see Fig. 4) I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	50 pF 65 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	6 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

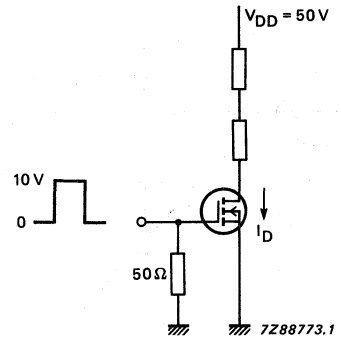


Fig. 2 Switching times test circuit.

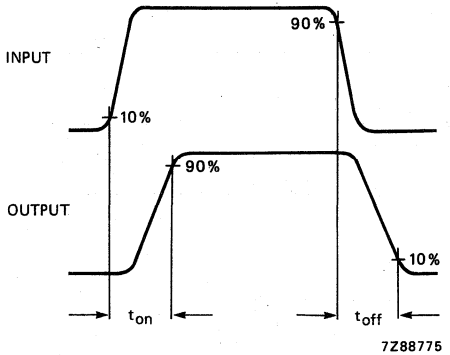


Fig. 3 Input and output waveforms.

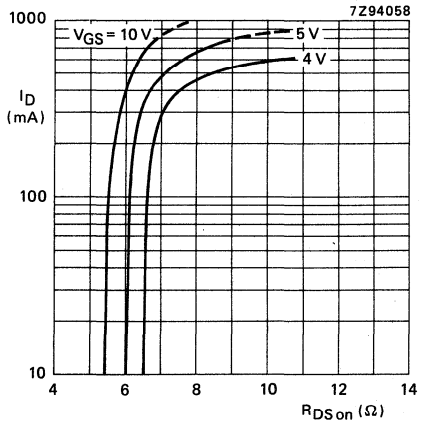


Fig. 4 T_j = 25 °C; typical values.

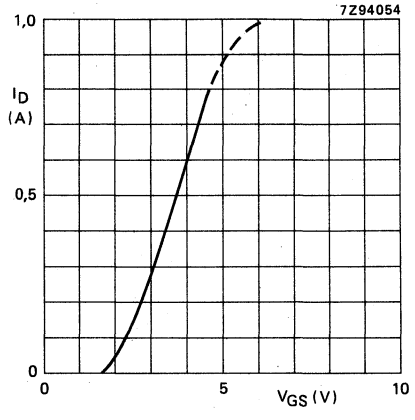


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

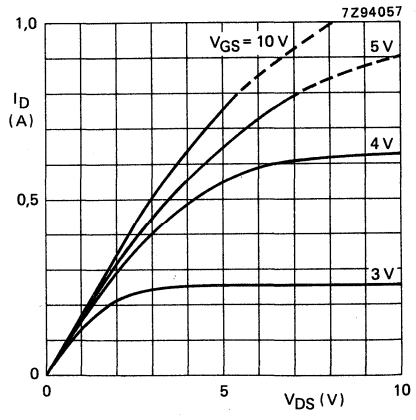


Fig. 6 T_j = 25 °C; typical values.

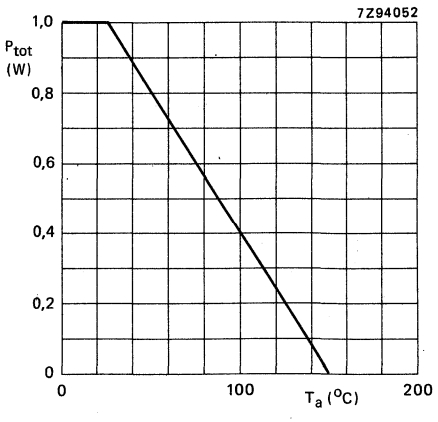


Fig. 7 Power derating curve.

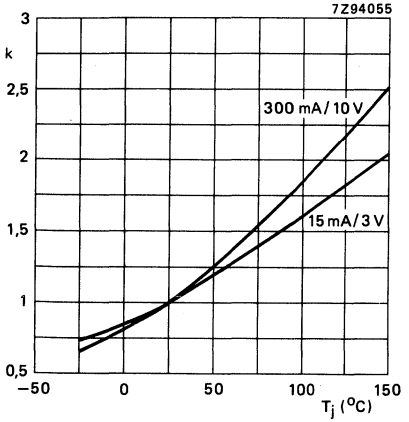


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typical values.

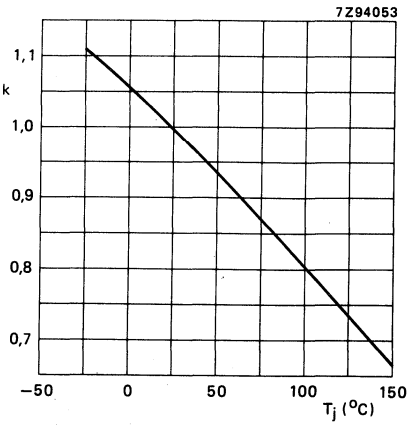


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 0,1 mA; typical values.

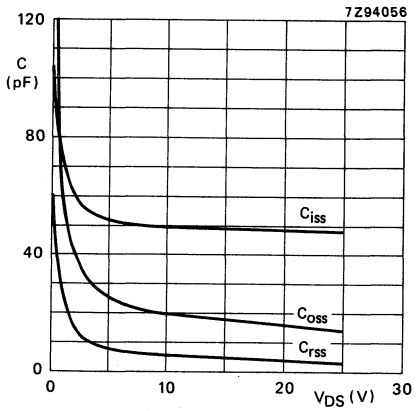


Fig. 10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

HIGH-VOLTAGE N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

High-voltage N-channel vertical D-MOS transistor in plastic TO-126 envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching, low power switching losses
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Drain-source ON-resistance $I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance $I_D = 250$ mA; $V_{DS} = 20$ V; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	400 mS

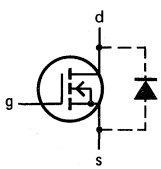
MECHANICAL DATA

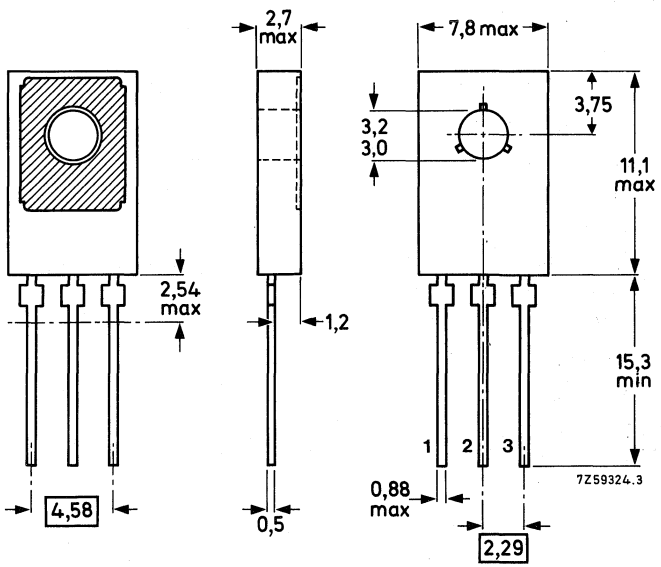
Dimensions in mm

Fig. 1 TO-126.

Drain connected to mounting base.

Pinning;
1 = source
2 = drain
3 = gate





RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	450 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 50\ \mu s$)	$V_{DS(SM)}$	max.	525 V
Gate-source voltage (open drain)	V_{GSO}	max.	20 V
Drain current (d.c.)	I_D	max.	0,75 A
Drain current (peak)	I_{DM}	max.	1,5 A
Total power dissipation up to $T_{mb} = 75\ ^oC$	P_{tot}	max.	15 W
Storage temperature	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$		100 K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$		5 K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

Drain-source breakdown voltage $I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DS}$	>	450 V
Drain-source leakage current $V_{DS} = 350$ V; $V_{GS} = 0$	I_{DSS}	<	25 μA
Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$	I_{GSS}	<	100 nA
Gate-source cut-off voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$	$V_{(P)GS}$	>	2,0 V
		<	4,0 V
Drain-source ON-resistance (see Fig. 4) $I_D = 100$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	10 Ω
		<	14 Ω
$I_D = 500$ mA; $V_{GS} = 10$ V	R_{DSon}	typ.	15 Ω
Transfer admittance at f = 1 kHz $I_D = 250$ mA; $V_{DS} = 20$ V	$\lvert y_{fs} \rvert$	typ.	400 mS
Input capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{is}	typ.	75 pF
		<	100 pF
Output capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{os}	typ.	25 pF
		<	35 pF
Feedback capacitance at f = 1 MHz $V_{DS} = 10$ V; $V_{GS} = 0$	C_{rs}	typ.	3 pF
		<	5 pF
Switching times (see Figs 2 and 3) $I_D = 100$ mA; $V_{DS} = 200$ V; $V_{GS} = 0$ to 10 V	t_{on}	<	10 ns
	t_{off}	<	100 ns

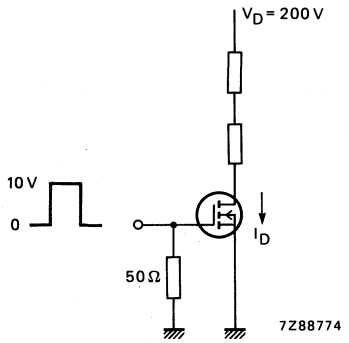


Fig. 2 Switching times test circuit.

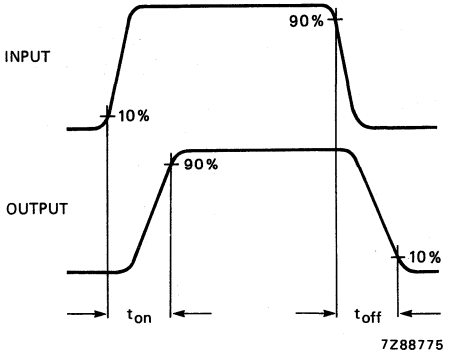


Fig. 3 Input and output waveforms.

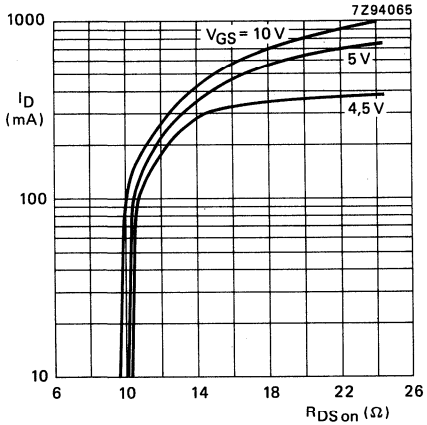


Fig. 4 T_j = 25 °C; typical values.

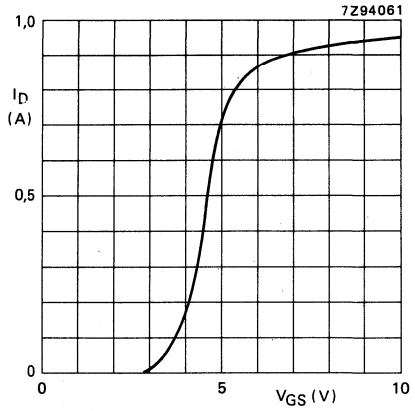


Fig. 5 T_j = 25 °C; V_{DS} = 20 V; typical values.

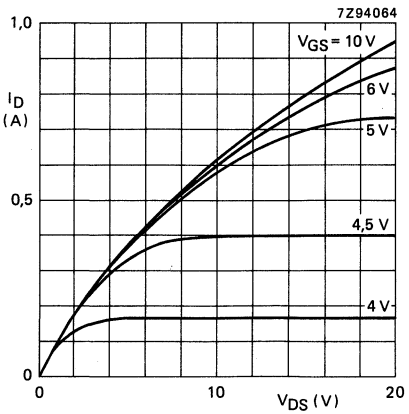


Fig. 6 T_j = 25 °C; typical values.

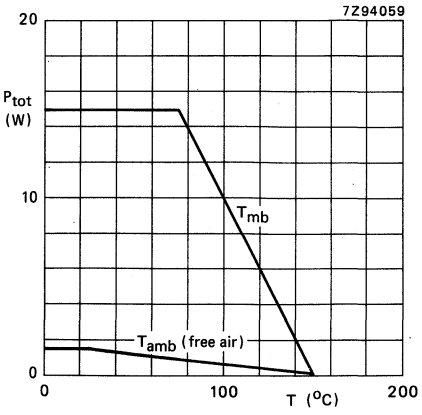


Fig. 7 Power derating curve.

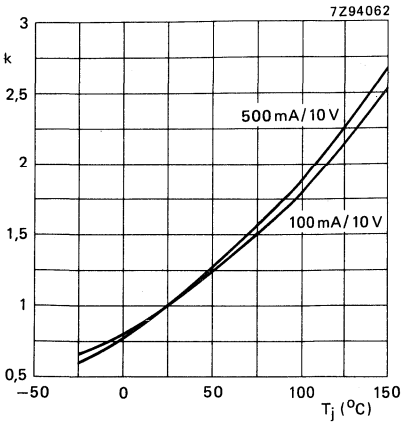


Fig. 8 $k = \frac{R_{DS\ on\ at\ T_j}}{R_{DS\ on\ at\ 25\ ^oC}}$; typical values.

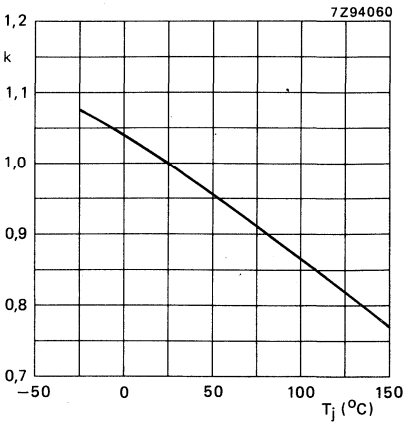


Fig. 9 $k = \frac{V_{GS(th)\ at\ T_j}}{V_{GS(th)\ at\ 25\ ^oC}}$; $V_{GS(th)}$ at 1 mA; typical values.

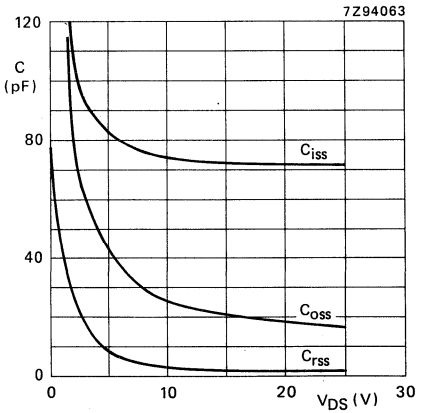


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Low $R_{DS\ on}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS

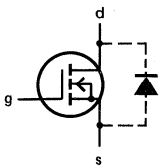
MECHANICAL DATA

Dimensions in mm

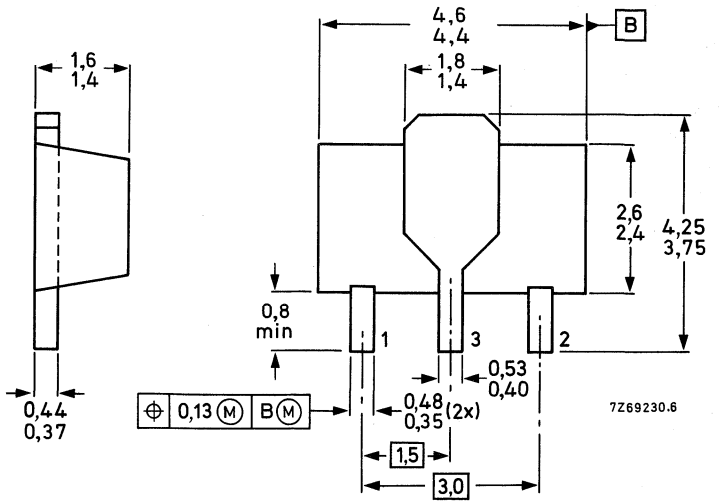
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: KM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	0.5 A
Drain current (peak)	I_{DM}	max.	1.0 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	2.0 Ω 4.0 Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	300 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 pF 60 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 ns 15 ns

Note

1. Transistors mounted on a substrate with surface area of 2.5 cm^2 and thickness of 0.7 mm.

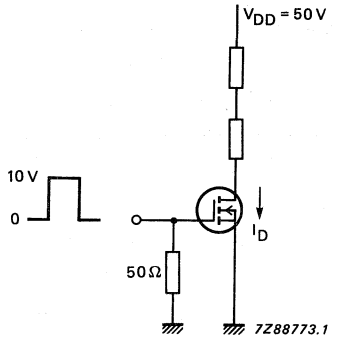


Fig.2 Switching times test circuit.

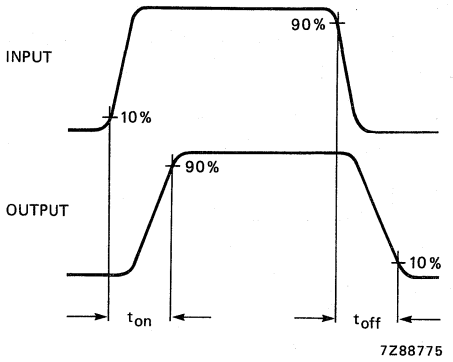


Fig.3 Input and output waveforms.

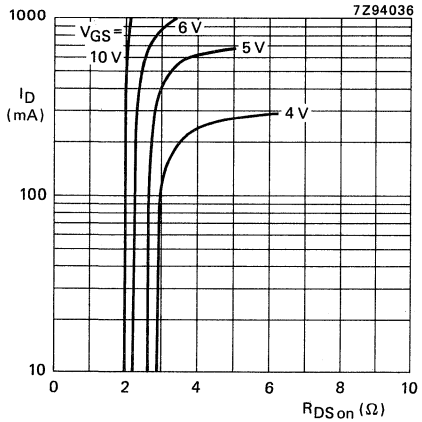


Fig.4 T_j = 25 °C; typical values.

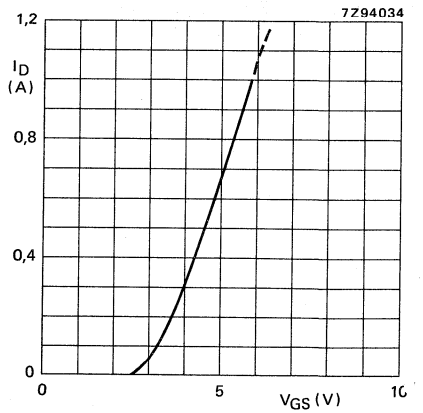


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

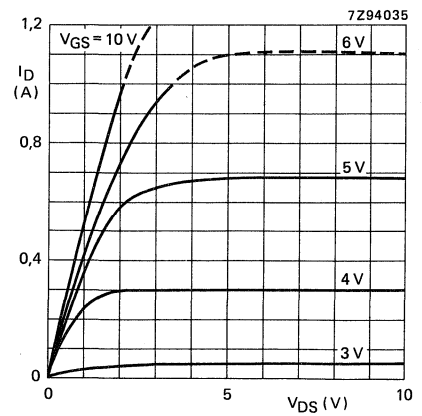


Fig.6 T_j = 25 °C; typical values.

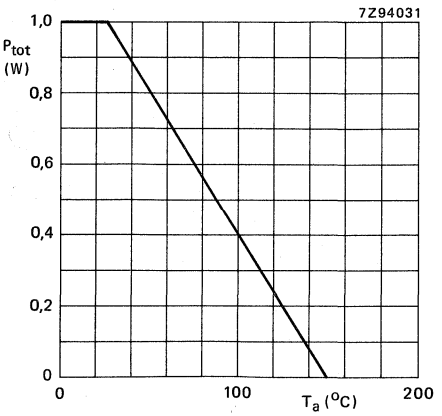


Fig.7 Power derating curve.

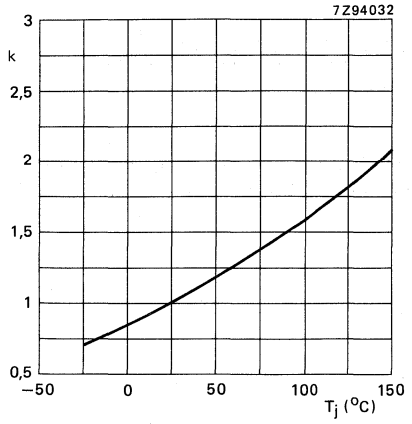


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\ ^oC}$; typ. values. at 500 mA/10 V.

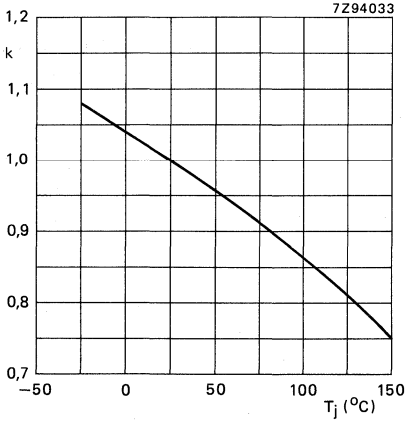


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

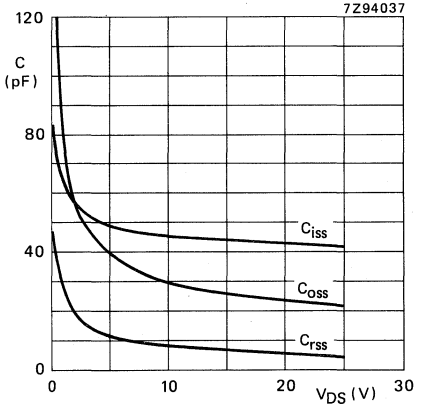


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ on}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS

MECHANICAL DATA

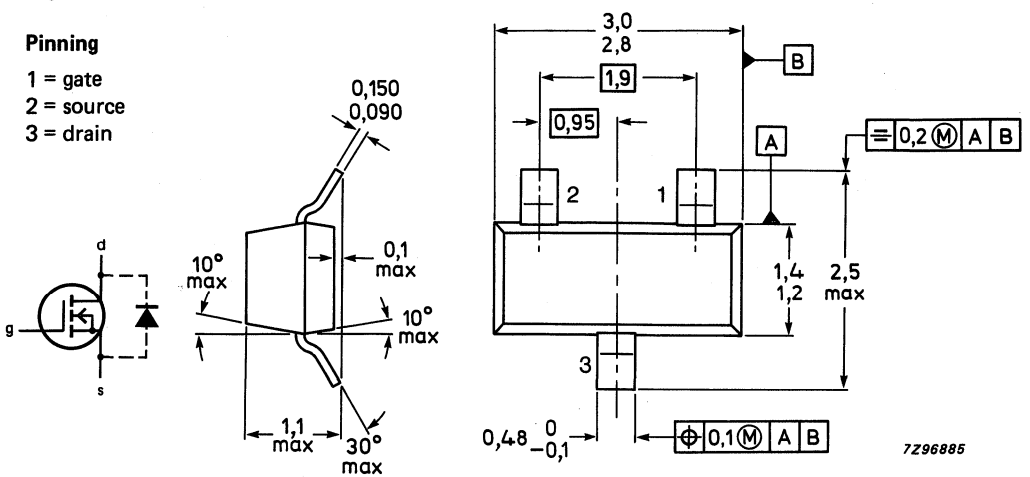
Dimensions in mm

Fig.1 SOT23.

Marking: 02p

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80 V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0 μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\lvert y_{fs} \rvert$	typ.	150 mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 pF 30 pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 pF 20 pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 pF 6 pF
Switching times (see Figs 2 and 3) I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 ns 10 ns
	t_{off}	typ. max.	4 ns 10 ns

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

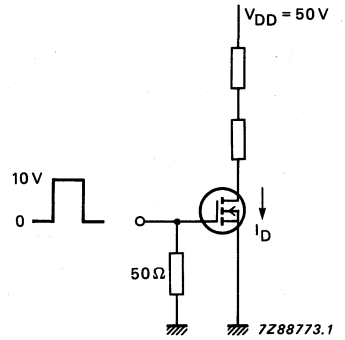


Fig.2 Switching times test circuit.

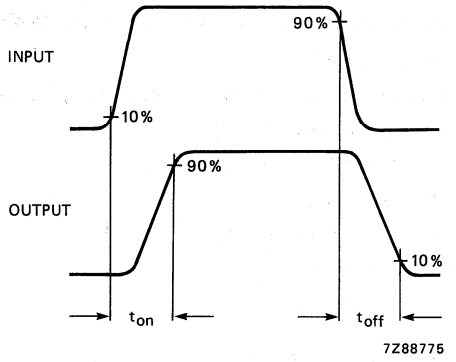


Fig.3 Input and output waveforms.

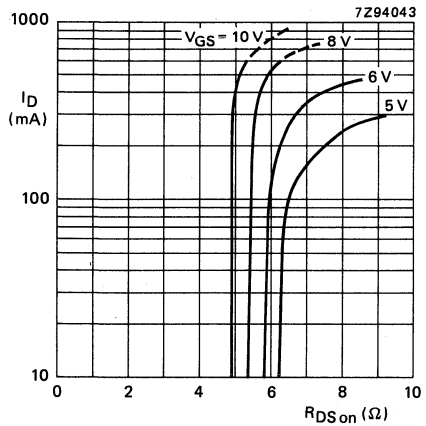


Fig.4 T_j = 25 °C; typical values.

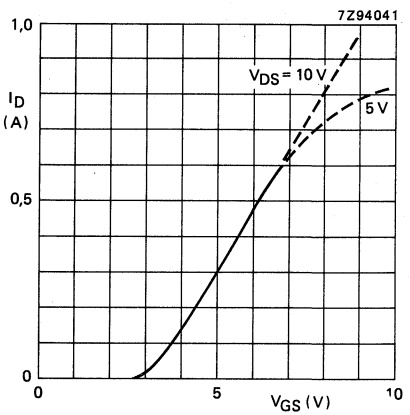


Fig.5 T_j = 25 °C; typical values.

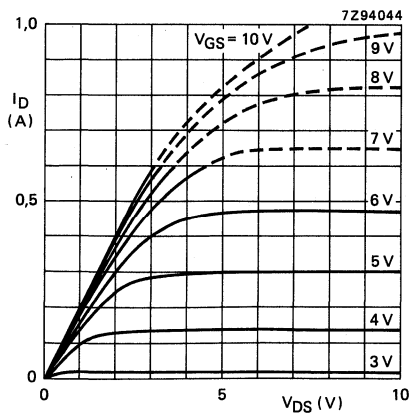


Fig.6 T_j = 25 °C; typical values.

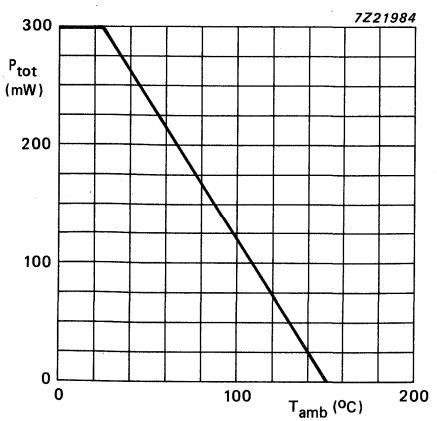


Fig.7 Power derating curve.

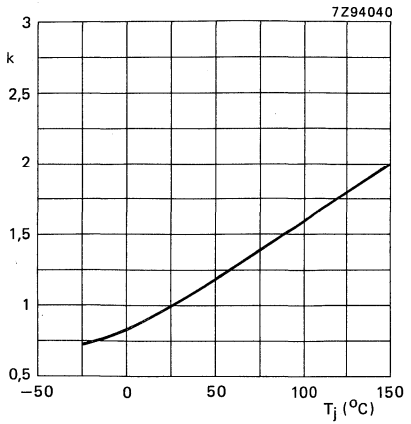


Fig.8 $k = \frac{R_{DS\,on}\text{ at }T_j}{R_{DS\,on}\text{ at }25\,^{o}C}$; typ. values at 150 mA/5 V.

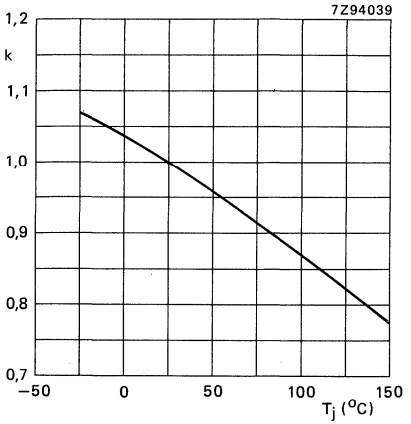


Fig.9 $k = \frac{V_{GS(th)}\text{ at }T_j}{V_{GS(th)}\text{ at }25\,^{o}C}$; $V_{GS(th)}$ at 1 mA; typical values.

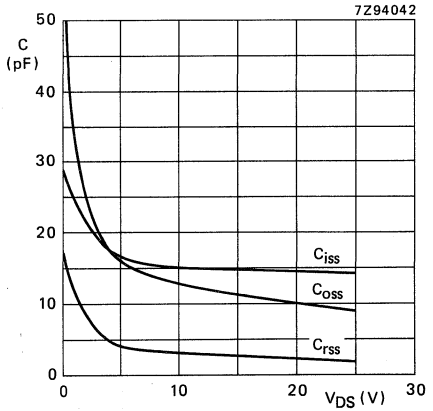


Fig.10 $T_j = 25\,^{o}C$; $V_{GS} = 0$; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

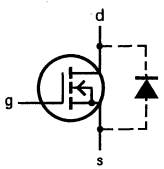
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 12	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS

MECHANICAL DATA

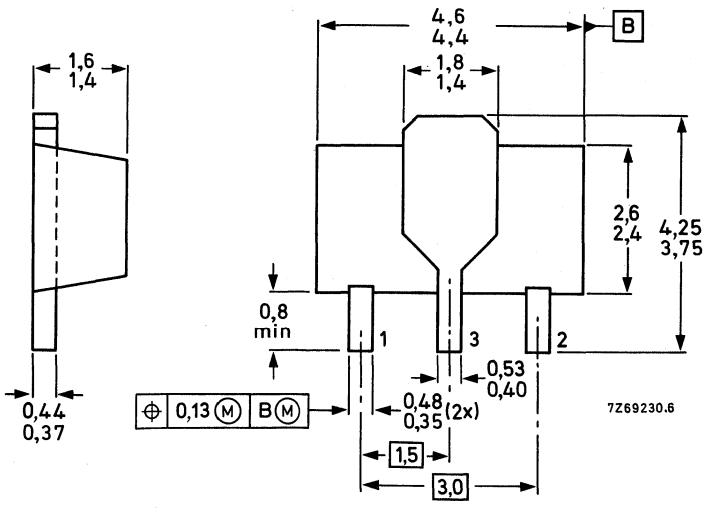
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



Marking: KN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 12	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	70 90	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	15 25	ns ns

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

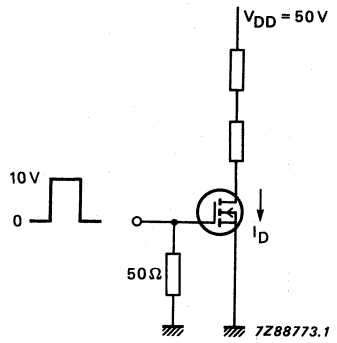


Fig. 2 Switching times test circuit.

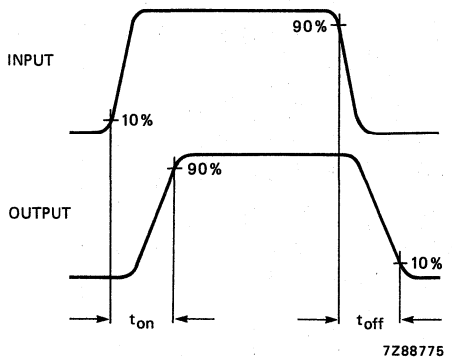


Fig. 3 Input and output waveforms.

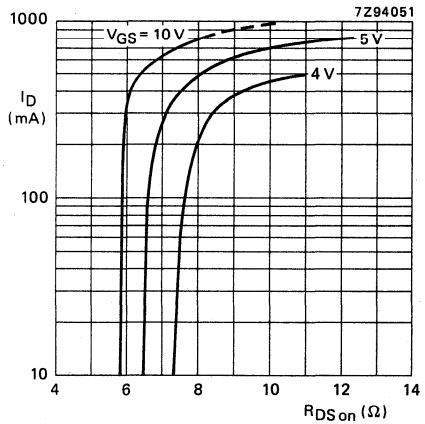


Fig. 4 T_j = 25 °C; typical values.

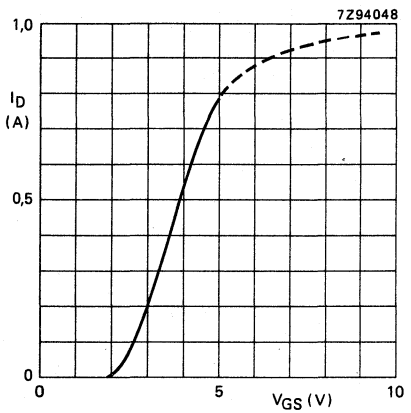


Fig. 5 T_j = 25 °C; V_{DS} = 10 V; typical values.

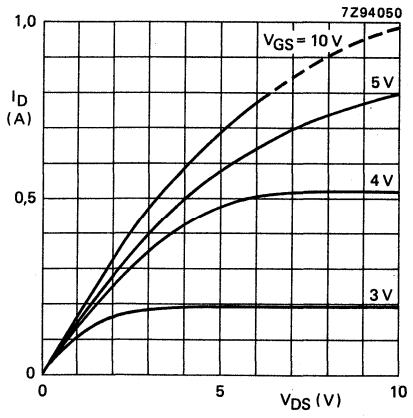


Fig. 6 T_j = 25 °C; typical values.

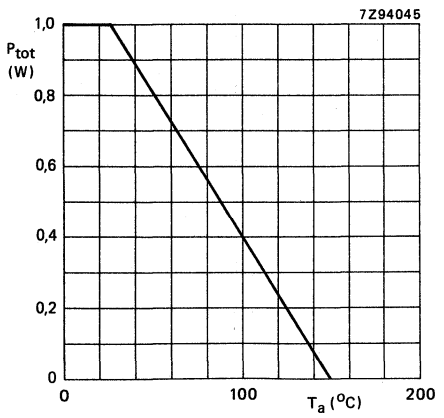


Fig. 7 Power derating curve.

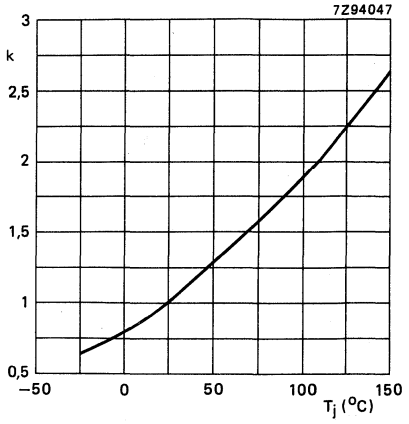


Fig. 8 $k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ ^oC}$; at 400 mA/10 V; typical values.

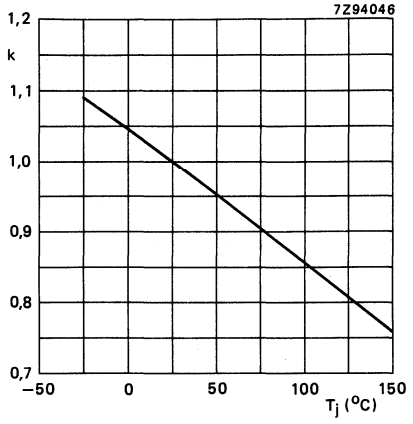


Fig. 9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 1 mA; typical values.

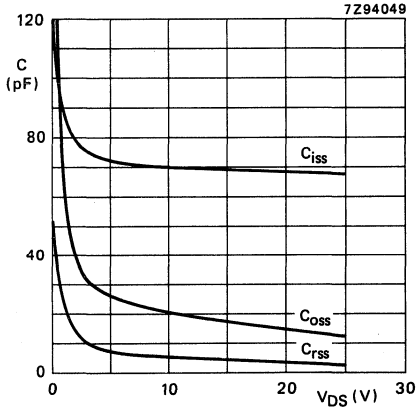


Fig. 10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	1 W
Drain-source ON-resistance $I_D = 15$ mA; $V_{GS} = 3$ V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance $I_D = 300$ mA; $V_{DS} = 15$ V	$\lvert y_{fs} \rvert$	typ.	250 mS

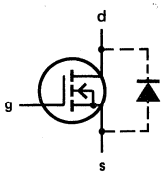
MECHANICAL DATA

Dimensions in mm

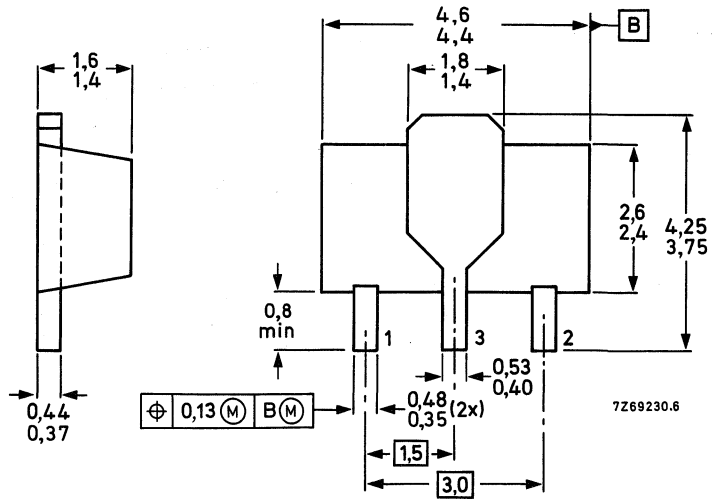
Fig.1 SOT89.

Pinning

1 = source
2 = gate
3 = drain



Marking: K0



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Drain current (peak)	I_{DM}	max.	800 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 100 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	180 V
Drain-source leakage current			
V_{DS} = 120 V; V_{GS} = 0	I_{DSS}	max.	10 μA
Gate-source leakage current			
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100 nA
Gate threshold voltage			
I_D = 100 μA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.7 V
		max.	2.7 V
Drain-source ON-resistance			
I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ.	7 Ω
		max.	10 Ω
I_D = 300 mA; V_{GS} = 10 V	R_{DSon}	typ.	6 Ω
Transfer admittance			
I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS
Input capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	50 pF
		max.	65 pF
Output capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20 pF
		max.	30 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	6 pF
		max.	10 pF
Switching times (see Figs 2 and 3)			
I_D = 300 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	max.	10 ns
	t_{off}	max.	15 ns

1. Transistors mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

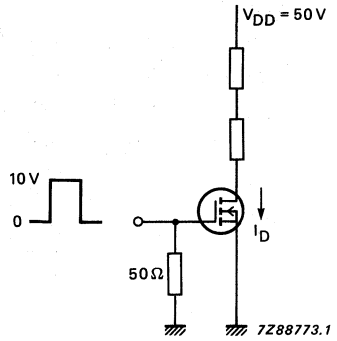


Fig.2 Switching times test circuit.

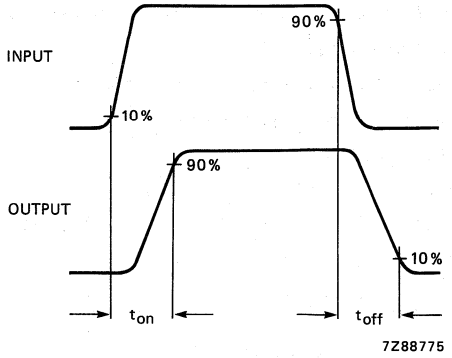


Fig.3 Input and output waveforms.

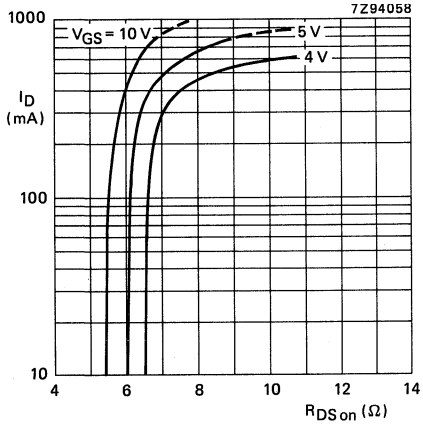


Fig.4 T_j = 25 °C; typical values.

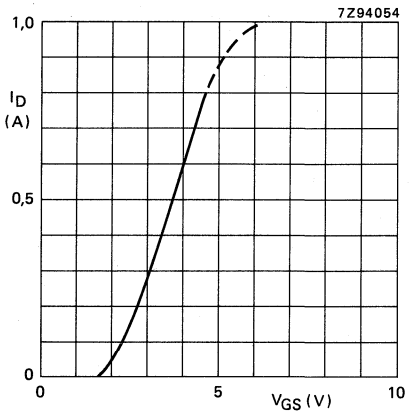


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

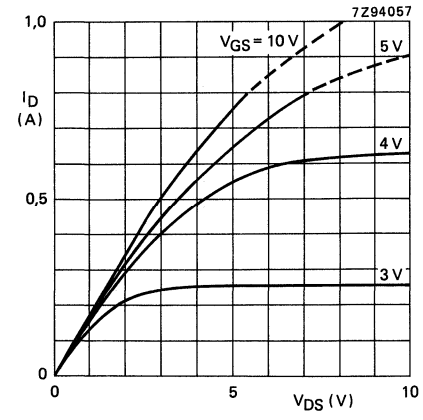


Fig.6 T_j = 25 °C; typical values.

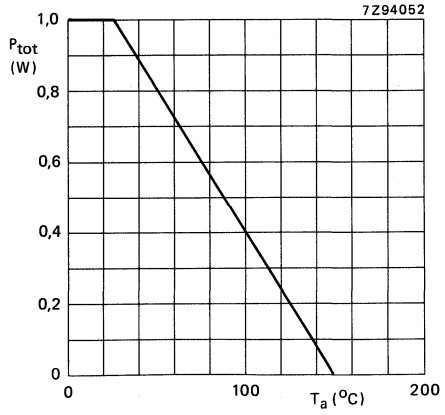


Fig.7 Power derating curve.

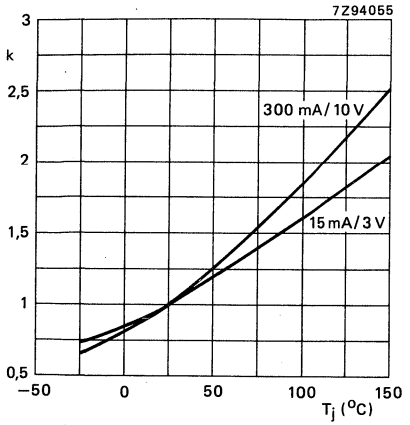


Fig.8 $k = \frac{R_{DS\,on}\ \text{at}\ T_j}{R_{DS\,on}\ \text{at}\ 25\ ^oC}$; typical values.

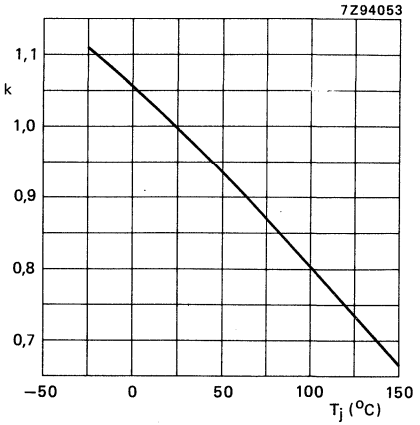


Fig.9 $k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ ^oC}$; $V_{GS(th)}$ at 0.1 mA; typical values.

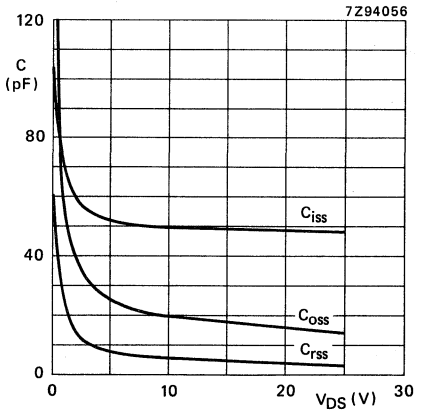


Fig.10 $T_j = 25\ ^oC$; $V_{GS} = 0$; f = 1 MHz; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

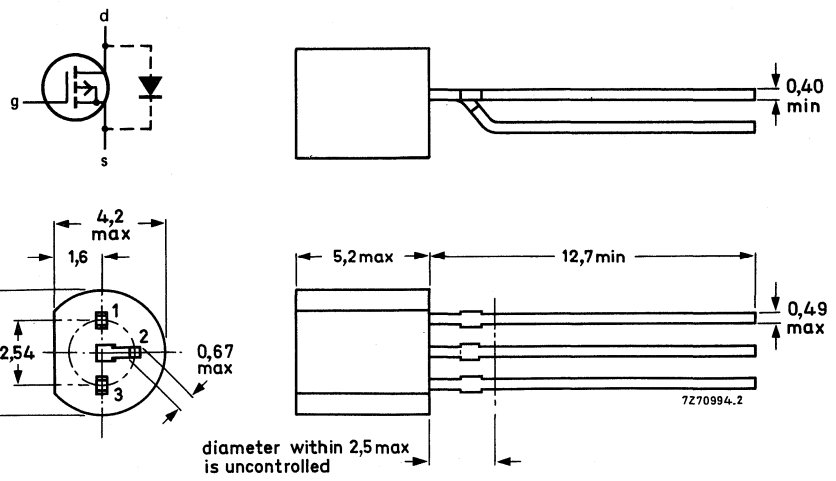
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 45 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

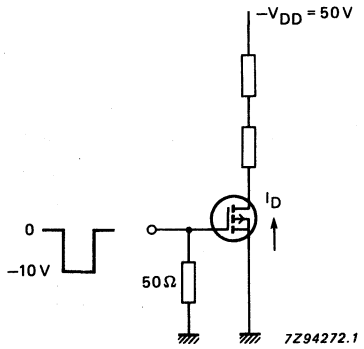


Fig.2 Switching times test circuit.

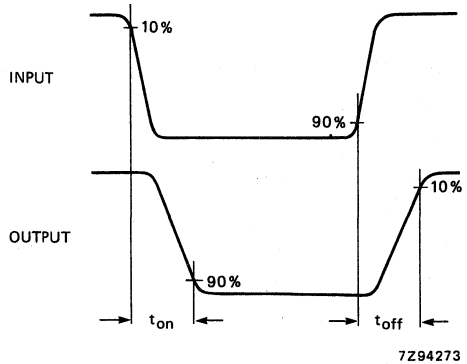


Fig.3 Input and output waveforms.

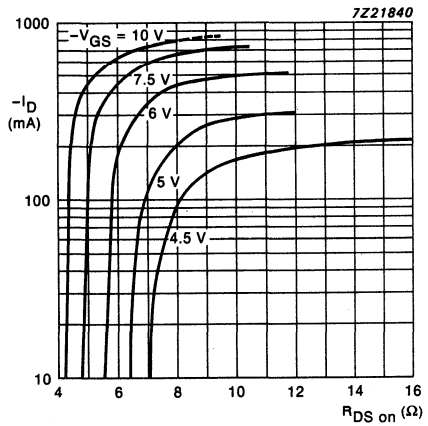


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

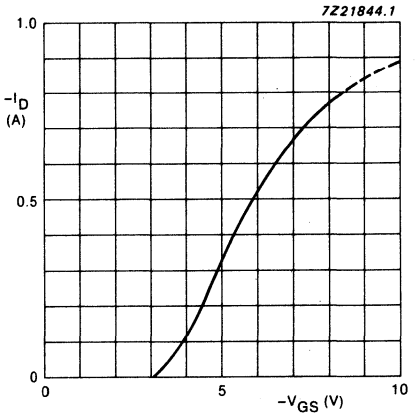


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

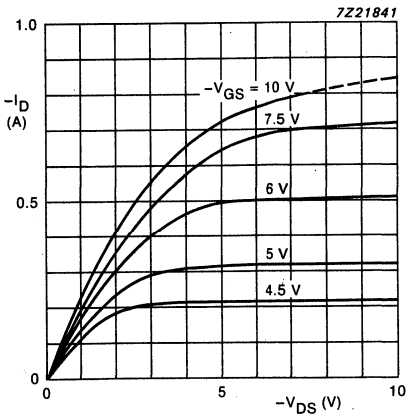


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENCHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125	mS

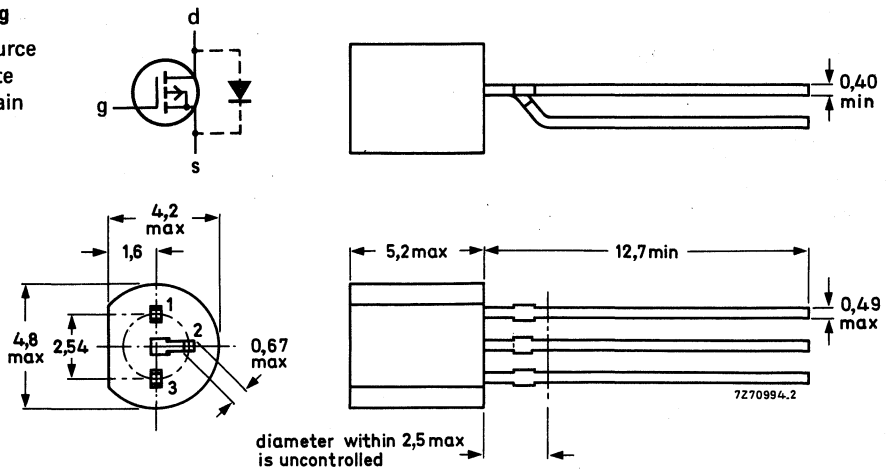
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	50 V
Drain-source leakage current $-V_{DS}$ = 40 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	7.5 Ω 10 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

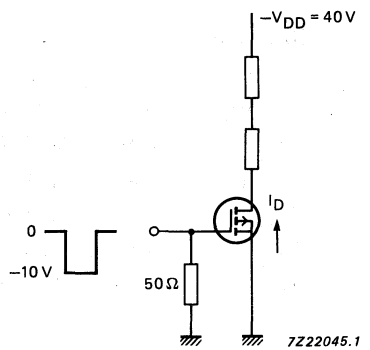


Fig.2 Switching times test circuit.

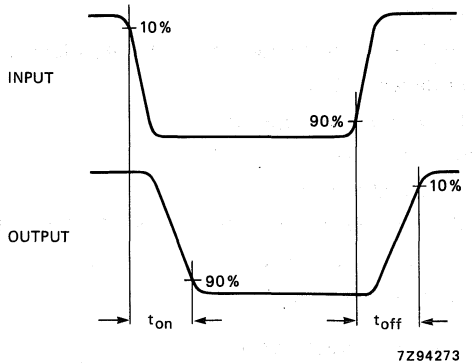


Fig.3 Input and output waveforms.

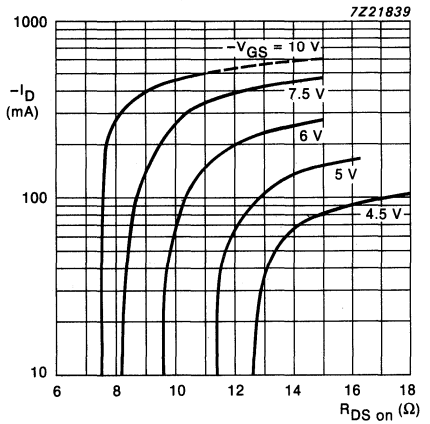


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

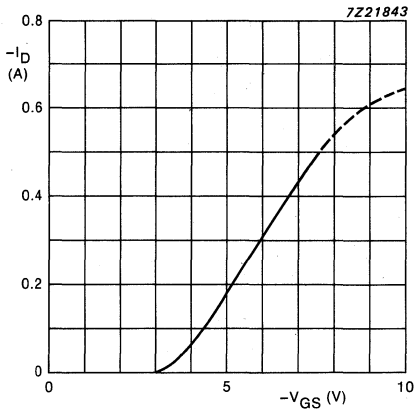


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

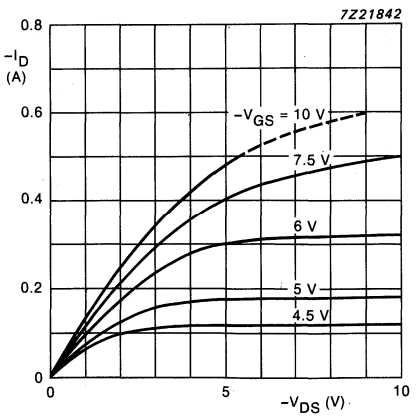


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

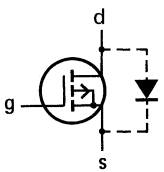
Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,3 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4,5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS

MECHANICAL DATA

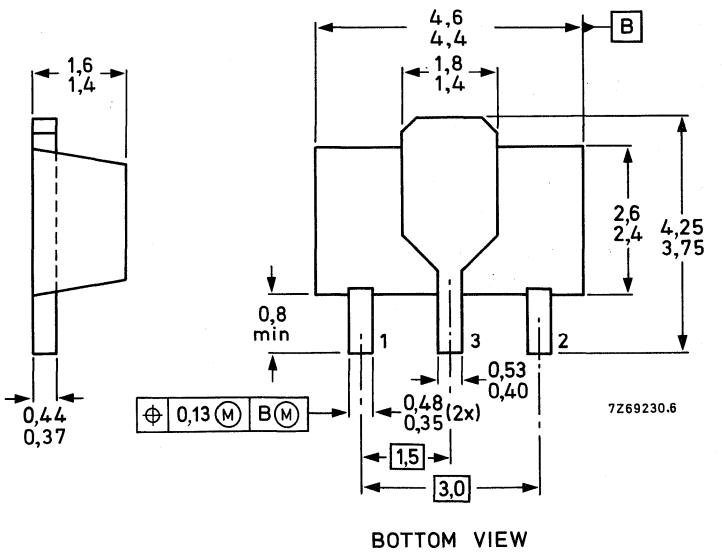
Dimensions in mm

Fig. 1 SOT89.

Pinning:
1 = source
2 = gate
3 = drain



marking: LM



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.3 A
Drain current (peak)	$-I_{DM}$	max.	0.8 A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	60 V
Drain-source leakage current $-V_{DS}$ = 45 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	200 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 pF 70 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 pF 45 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 pF 12 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 20 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

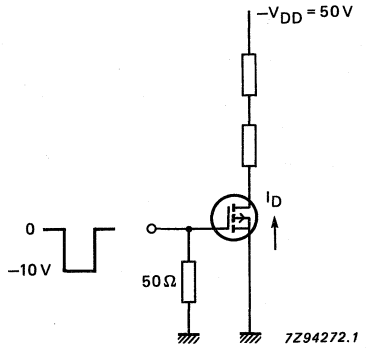


Fig.2 Switching times test circuit.

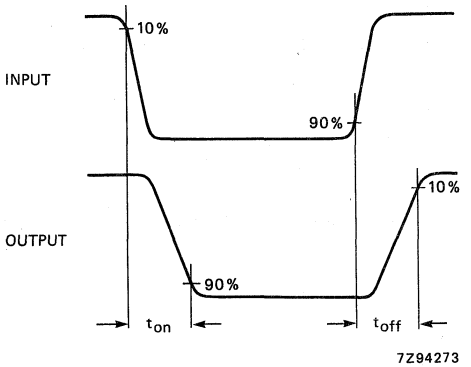


Fig.3 Input and output waveforms.

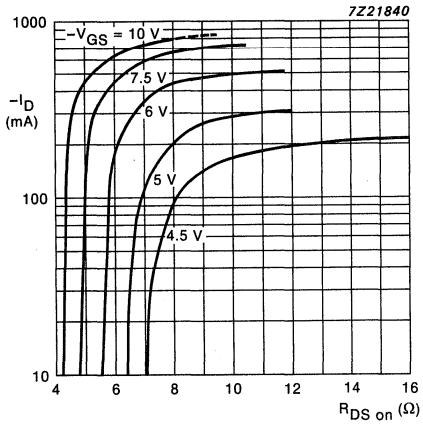


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

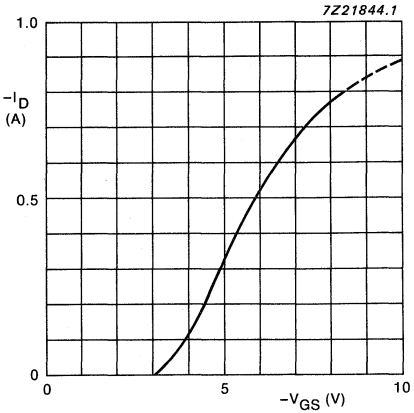


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

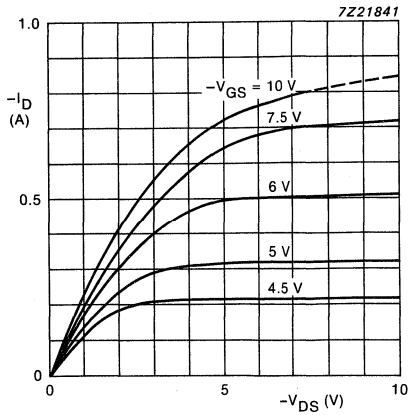


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

Features

- Very low R_{DSon}
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0,25 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ.	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS

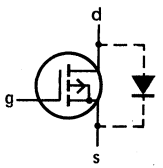
MECHANICAL DATA

Dimensions in mm

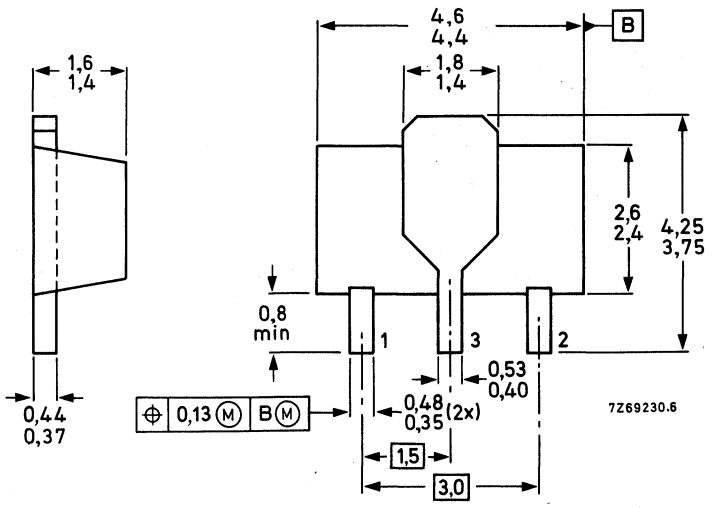
Fig. 1 SOT89.

Pinning:

1 = source
2 = gate
3 = drain



Marking: LN



BOTTOM VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	50 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage $-I_D$ = 100 μA; $-V_{GS}$ = 0	$-V_{(BR)DSS}$	min.	50 V
Drain-source leakage current $-V_{DS}$ = 1 V; V_{GS} = 0	$-I_{DSS}$	max.	10 μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100 nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 V 3.5 V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	R_{DSon}	max. typ..	10 Ω 7.5 Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert y_{fs} \rvert$	typ.	125 mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 ns 10 ns

Note:

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2; thickness = 0,7 mm.

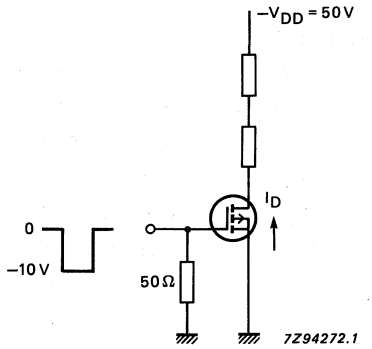


Fig. 2 Switching times test circuit.

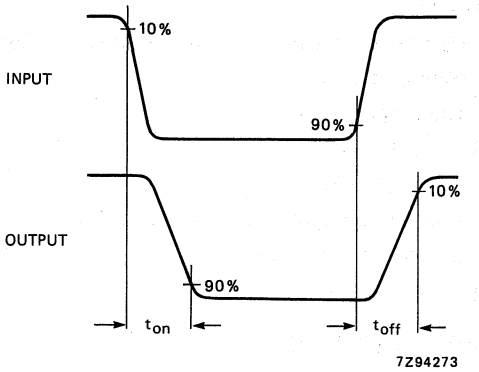


Fig. 3 Input and output waveforms.

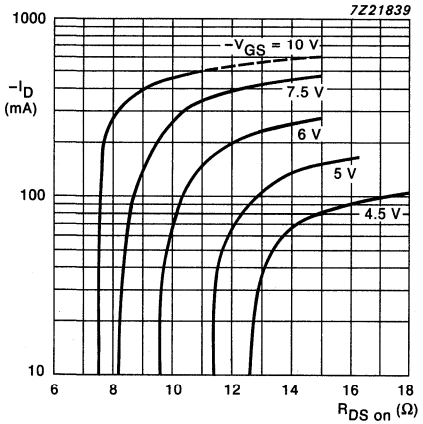


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

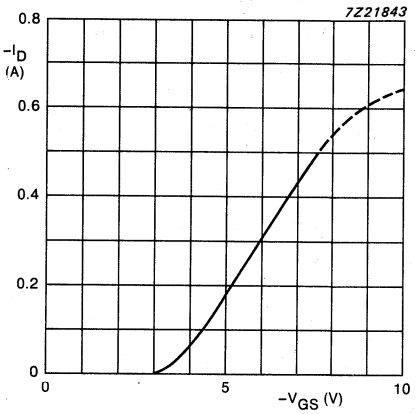


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

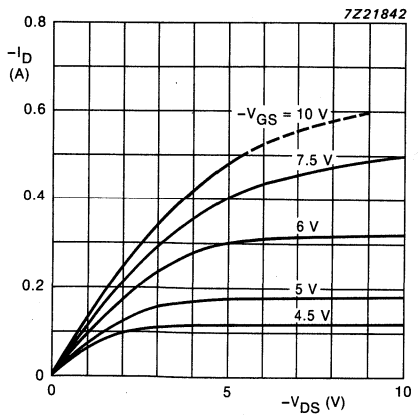


Fig.6 Output characteristics; T_j = 25 °C; typical values.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistors, in TO-92 variant envelopes and designed for application as low power, high-frequency inverters and line drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	20	20	V
Drain current (DC)	I_D	max.	0,75	0,5	0,5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	1	1	W
Drain-source on-state resistance I_D = 1.0 A; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	0.9 1.8	1.4 3.0	1.9 4.0	Ω Ω
Transfer admittance I_D = 0.5 A; V_{DS} = 25 V	$\|y_{fs}\|$	min.	170	170	170	mS

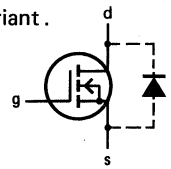
MECHANICAL DATA

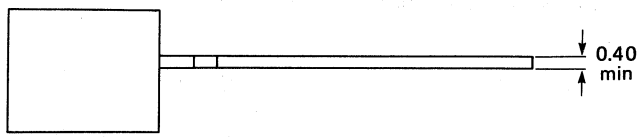
Dimensions in mm

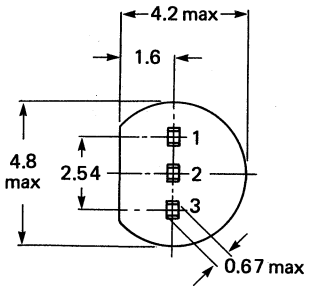
Fig. 1 TO-92 variant.

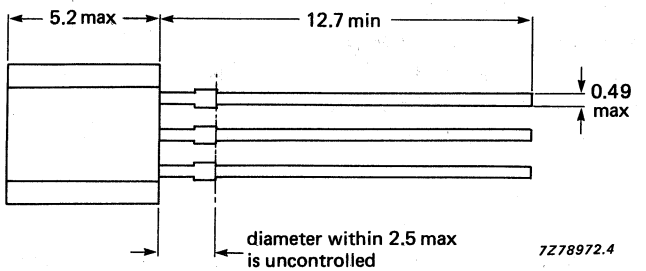
Pinning:

1 = Drain
2 = Gate
3 = Source









Note: Various pinout configurations available.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			PH6659	PH6660	PH6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	20	20	V
Drain current (DC)	I_D	max.	0.75	0.5	0.5	A
Drain current (peak)	I_{DM}	max.		1.0		A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		1		W
Storage temperature range	T_{stg}			−65 to +150		°C
Junction temperature	T_j	max.		150		°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=		125		K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

			PH6659	PH6660	PH6661	
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	35	60	90	V
Drain-source leakage current at V_{DS} = V_{DS} max; V_{GS} = 0	I_{DSS}	max.	10	10	10	μA
Gate-source leakage current at V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	100	100	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	0.8	0.8	V
		max.	2.0	2.0	2.0	V
On-state drain current V_{DS} = 25 V; V_{GS} = 10 V	$I_{D(ON)}$	min.	1.0	1.0	1.0	A
		typ.	2.0	2.0	2.0	A
Drain-source on-state resistance I_D = 0.3 A; V_{GS} = 5 V	$R_{DS\ on}$	typ.	1.5	1.8	2.4	Ω
		max.	5.0	5.0	5.3	Ω
I_D = 1.0 A; V_{GS} = 10 V	$R_{DS\ on}$	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance I_D = 0.5 A; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min.	170	170	170	mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	50	50	50	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	50	40	40	pF

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

			PH6659	PH6660	PH6661
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	15	15	15 pF
Switching times I_D = 0,5 A; V_{DD} = 25 V; V_{GS} = 0 to 10 V	t_{on}	max.	10	10	10 ns
	t_{off}	max.	15	15	15 ns

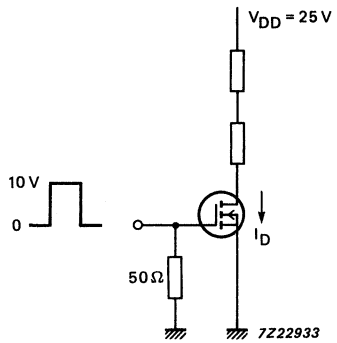


Fig. 2 Switching times test circuit.

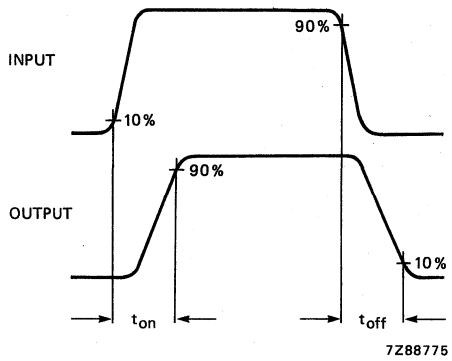


Fig. 3 Input and output waveforms.

Philips Components

Data sheet	
status	Product specification
date of issue	November 1990

PMBF107
N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

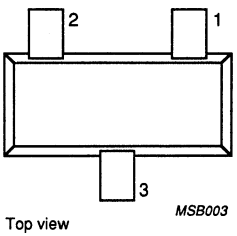
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.4	V

PIN CONFIGURATION



Top view

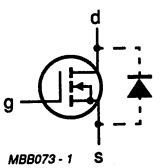


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printboard.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printboard.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain cut-off current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
		I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

PMBF107

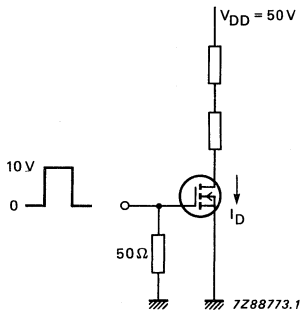


Fig.2 Switching time test circuit.

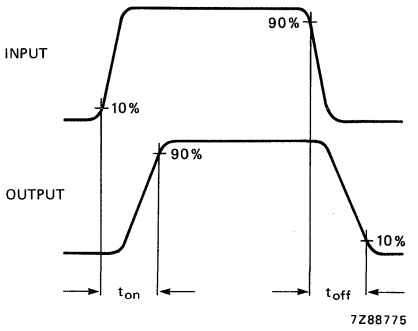


Fig.3 Input and output waveforms.

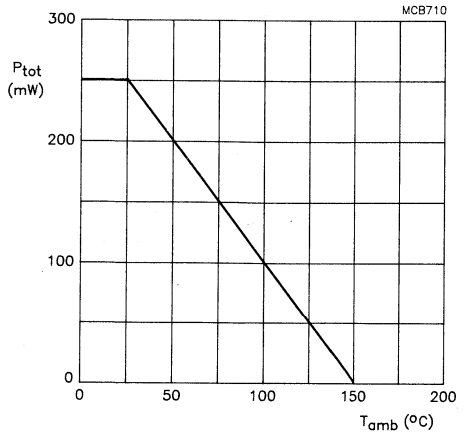


Fig.4 Power derating curve.

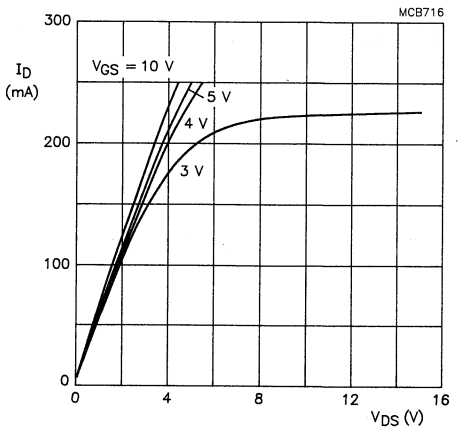


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

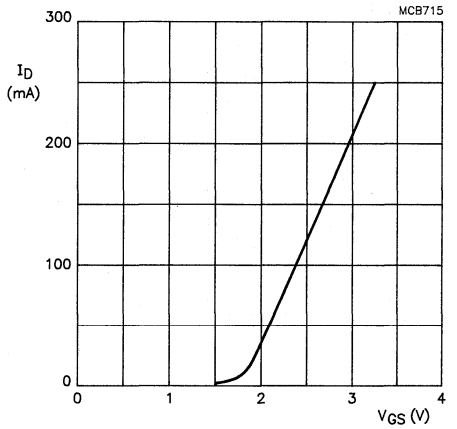


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

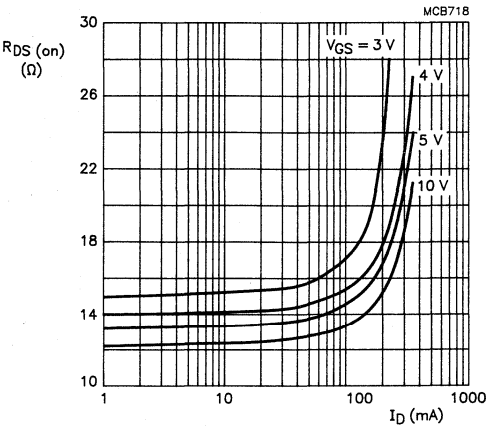


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

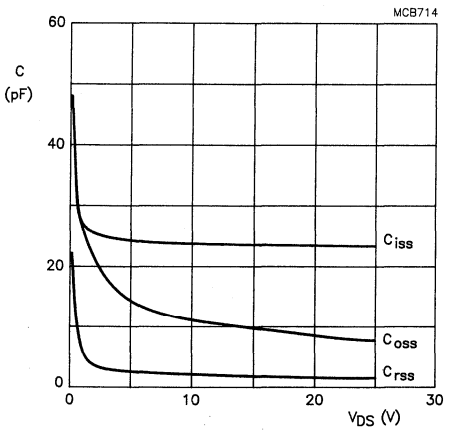
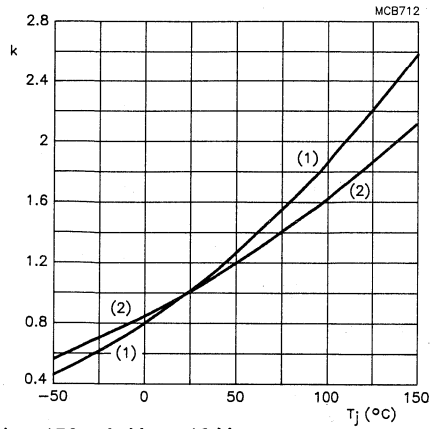


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

PMBF107



(1) I_D = 150 mA; V_{GS} = 10 V.
(2) I_D = 20 mA; V_{GS} = 2.6 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)}\ at\ T_j}{R_{DS(on)}\ at\ 25\ °C}$; typical $R_{DS(on)}$.

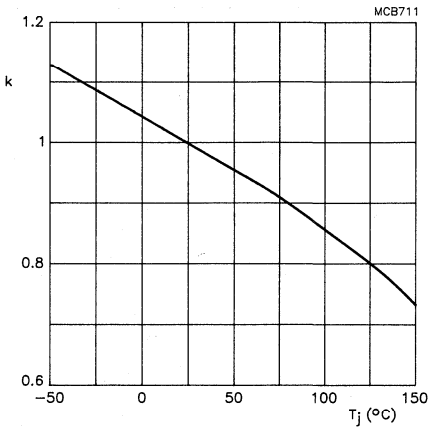
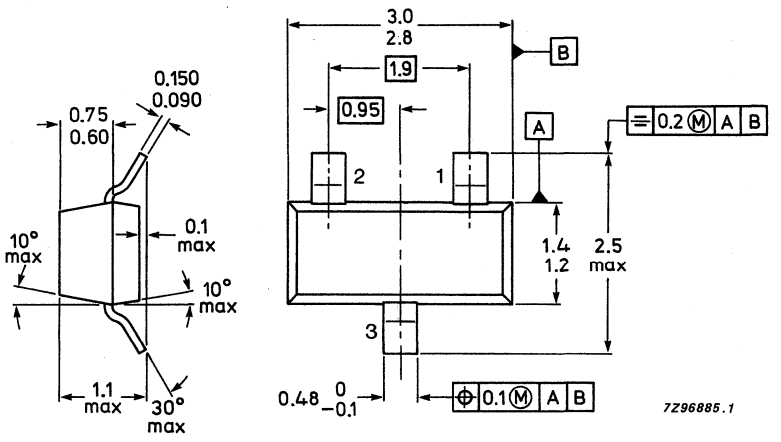


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)}\ at\ T_j}{V_{GS(th)}\ at\ 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

PACKAGE OUTLINE



TOP VIEW

Dimensions in mm.

Marking code: PMBF107 = pKZ.

Fig.11 SOT23.

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300 mW
Drain-source on-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS\,on}$	typ. max.	2.5 Ω 5.0 Ω
Transfer admittance I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min. typ.	100 mS 200 mS

MECHANICAL DATA

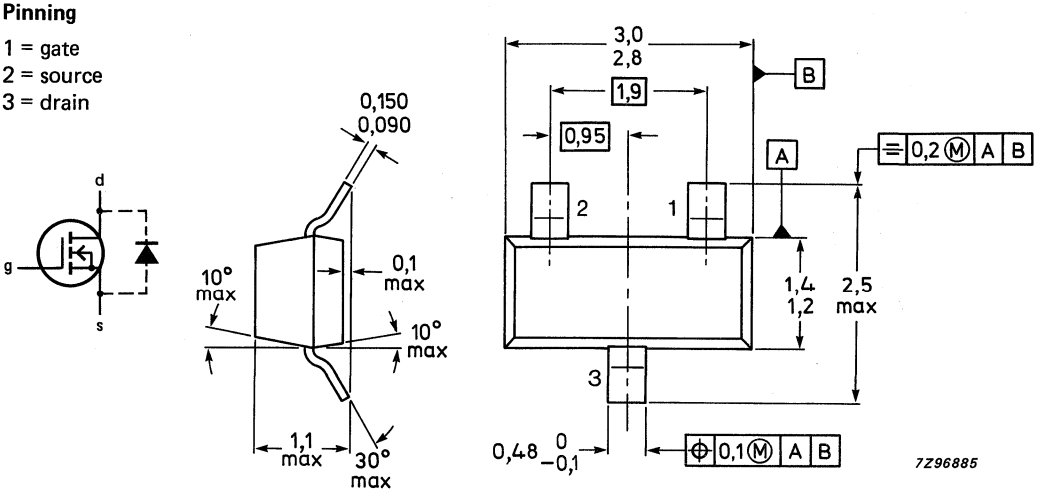
Fig.1 SOT23.

Dimensions in mm

Marking code:
PMBF170 = pKX

Pinning

1 = gate
2 = source
3 = drain



TOP VIEW

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Drain current (peak)	I_{DM}	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300 mW (note 1)
		max.	250 mW (note 2)
Storage temperature range	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430 K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage			
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	60 V
		typ.	90 V
Drain-source leakage current			
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500 nA
V_{DS} = 48V; V_{GS} = 0	I_{DSS}	max.	1 μA
Gate-source leakage current			
V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10 nA
Gate-source cut-off voltage			
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8 V
		max.	3.0 V
Drain-source on-resistance			
I_D = 200 mA; V_{GS} = 10 V	$R_{DS\ on}$	typ.	2.5 Ω
		max.	5.0 Ω
Transfer admittance			
I_D = 200 mA; V_{DS} = 10 V	$\lvert y_{fs} \rvert$	min.	100 mS
		typ.	200 mS
Input capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ.	25 pF
		max.	40 pF
Output capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ.	22 pF
		max.	30 pF
Feedback capacitance			
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ.	6 pF
		max.	10 pF

Notes

1. Mounted on ceramic substrate measuring 10 mm x 8 mm x 0.7 mm.
2. Mounted on printed-circuit board.

Switching times

V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V

t_{on}	max.	10 ns
t_{off}	max.	15 ns

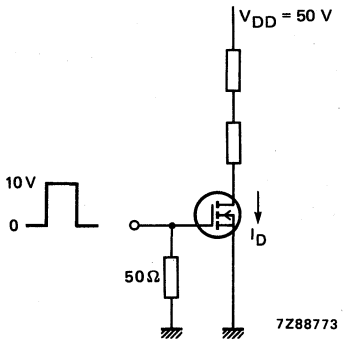


Fig.2 Switching times test circuit.

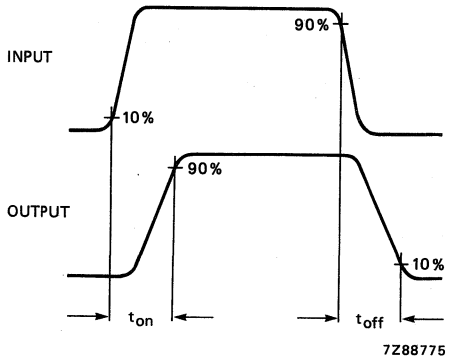


Fig.3 Input and output waveforms.

Data sheet	
status	Preliminary specification
date of issue	October 1990

VN2406L

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

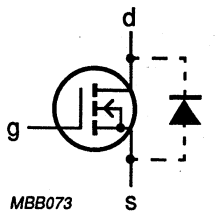


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	210	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

VN2406L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	210	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100\ \mu A$ $V_{GS} = 0$	240	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V $V_{GS} = 0$	-	-	10	μA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20$ V	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1$ mA $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500$ mA $V_{GS} = 10$ V	-	-	6	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 100$ mA $V_{GS} = 2.5$ V	-	-	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$I_D = 300$ mA $V_{DS} = 25$ V	200	400	-	mS
C_{iss}	input capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	20	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ $f = 1$ MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	5	10	ns
t_{off}	turn-off time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

VN2406L

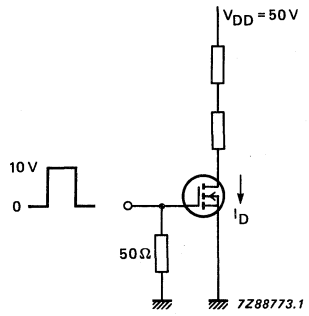


Fig.2 Switching time test circuit.

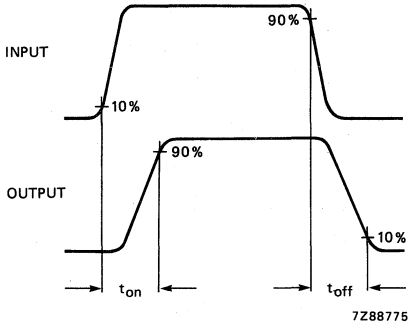


Fig.3 Input and output waveforms.

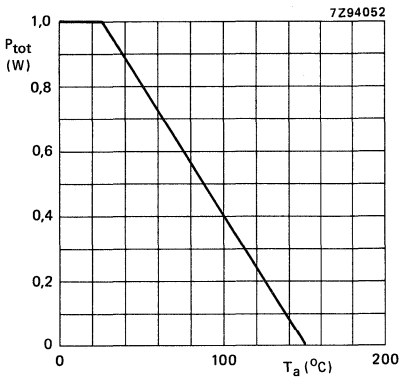


Fig.4 Power derating curve.

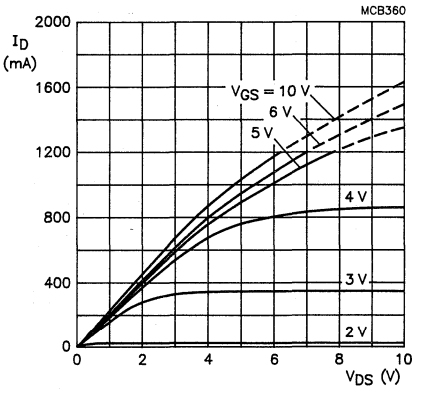


Fig.5 Typical output characteristics; T_j = 25 °C;.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

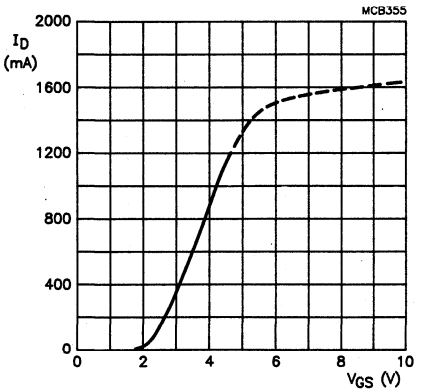


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

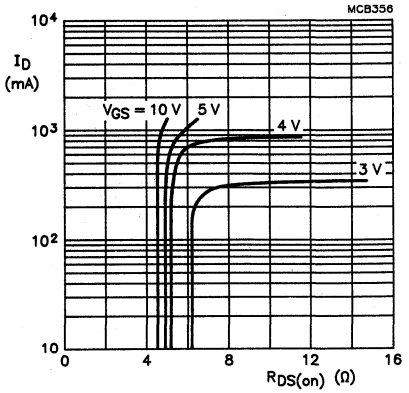


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

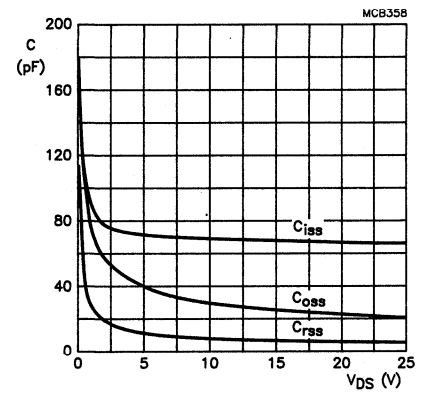


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

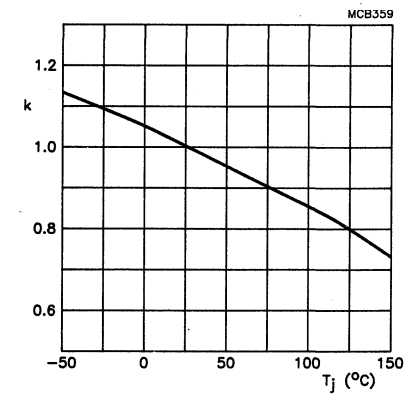


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$$; $V_{GS(th)}$ at 1 mA; typical values.

N-channel enhancement mode vertical D-MOS transistor

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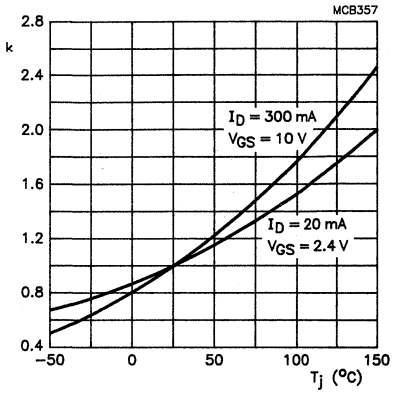


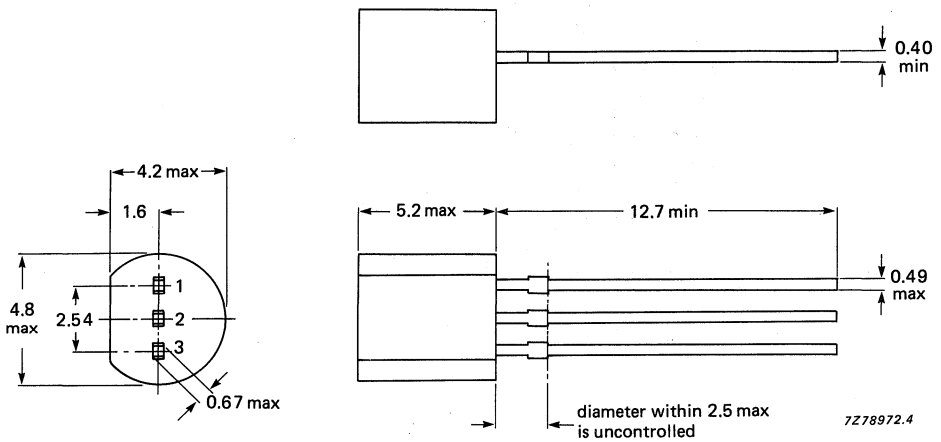
Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

N-channel enhancement mode vertical D-MOS transistor

VN2406L

MECHANICAL DATA



Dimensions in mm

Fig.11 TO-92 variant.

Data sheet	
status	Preliminary specification
date of issue	October 1990

VN2410L

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

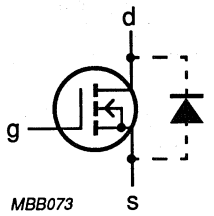


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	10	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

N-channel enhancement mode vertical D-MOS transistor

VN2410L

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	40	V
I_D	drain current	DC value	-	150	mA
I_{DM}	drain current	peak value	-	1.2	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	-	1	W
T_{stg}	storage temperature range		−65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

CHARACTERISTICS

$T_j = 25$ °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 100\ \mu A$ $V_{GS} = 0$	240	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V $V_{GS} = 0$	-	-	10	μA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 20$ V	-	-	100	nA
$V_{GS(th)}$	gate threshold voltage	$I_D = 1$ mA $V_{DS} = V_{GS}$	0.8	-	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 500$ mA $V_{GS} = 10$ V	-	-	10	Ω
$R_{DS(on)}$	drain-source on-resistance	$I_D = 100$ mA $V_{GS} = 2.5$ V	-	-	10	Ω
$\|Y_{fs}\|$	transfer admittance	$I_D = 300$ mA $V_{DS} = 25$ V	200	400	-	mS
C_{iss}	input capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ f = 1 MHz	-	65	90	pF
C_{oss}	output capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ f = 1 MHz	-	20	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25$ V $V_{GS} = 0$ f = 1 MHz	-	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	5	10	ns
t_{off}	turn-off time	$I_D = 250$ mA $V_{DD} = 50$ V $V_{GS} = 0$-10 V	-	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

VN2410L

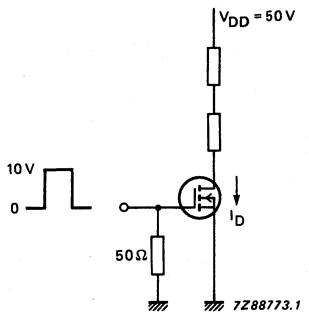


Fig.2 Switching time test circuit.

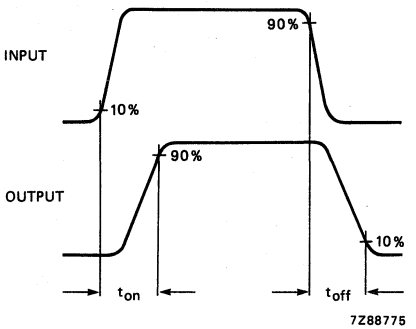


Fig.3 Input and output waveforms.

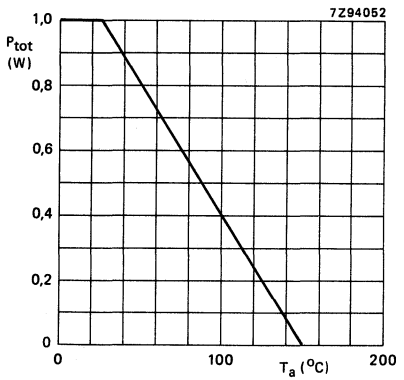


Fig.4 Power derating curve.

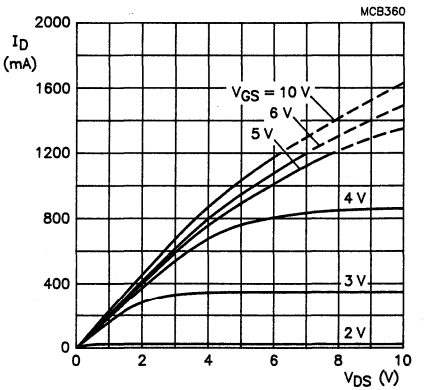


Fig.5 Typical output characteristics; T_j = 25 °C;.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

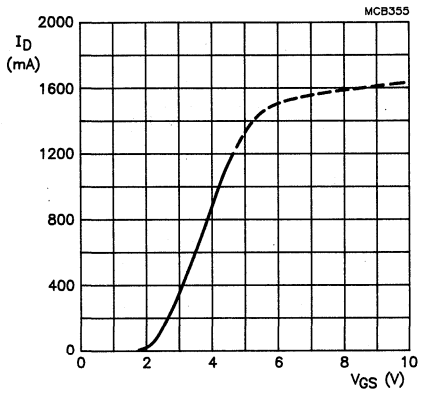


Fig.6 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25 °C;.

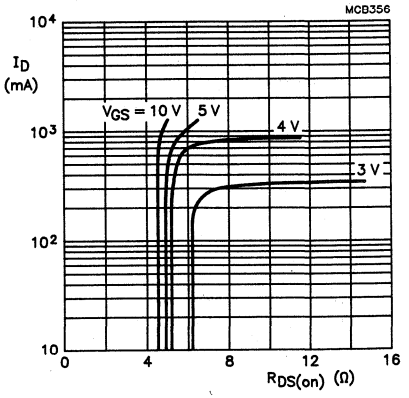


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C;.

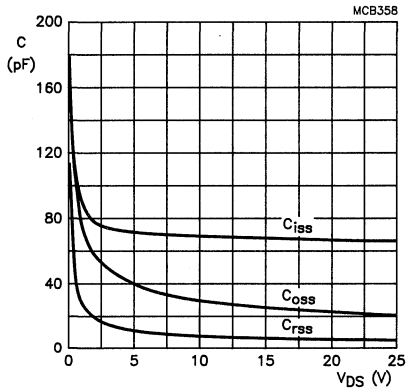


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C;.

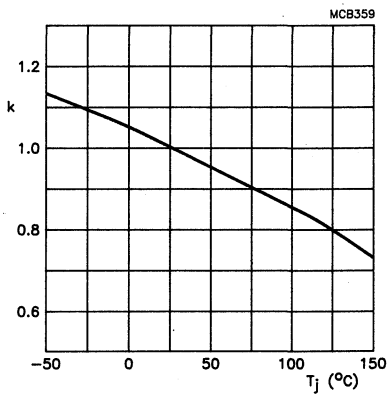


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{+V_{GS(th)} \text{ at } T_j}{+V_{GS(th)} \text{ at } 25\ °C}$$; $V_{GS(th)}$ at 1 mA; typical values.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

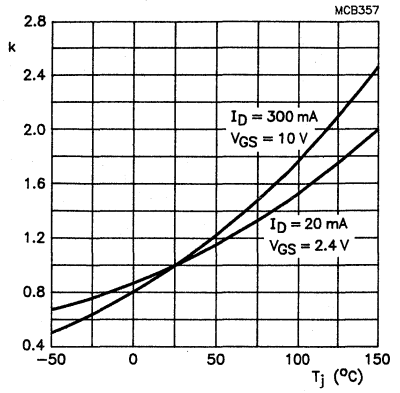


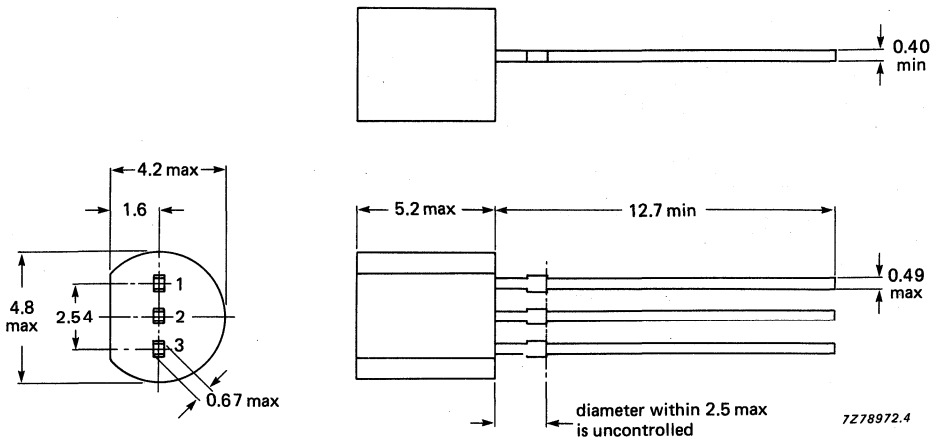
Fig.10 Temperature coefficient of drain-source on-resistance;

$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical values.

N-channel enhancement mode vertical D-MOS transistor

VN2410L

MECHANICAL DATA



Dimensions in mm

Fig.11 TO-92 variant.

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Total power dissipation up to T_c = 25 °C	P_{tot}	max.	6.25	6.25	6.25	W
Drain-source ON-resistance I_D = 1.0 A; V_{GS} = 10 V	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance at f = 1 kHz I_D = 0.5 A; V_{DS} = 25 V	$\|y_{fs}\|$	max.	170	170	170	mS

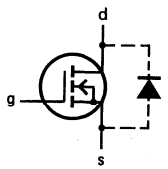
MECHANICAL DATA

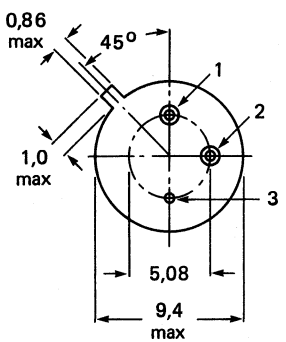
Dimensions in mm

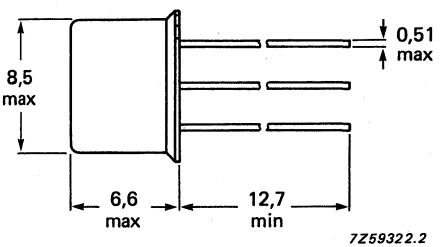
Fig. 1 TO-39.

Pinning:

1 = Source
2 = Gate
3 = Drain







Maximum lead diameter is guaranteed only for 12.7 mm

Accessories: 56245 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N6659	2N6660	2N6661	
Drain-source voltage	V_{DS}	max.	35	60	90	V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30	V
Drain current (DC)	I_D	max.	1.4	1.1	0.9	A
Drain current (peak) (note 1)	I_{DM}	max.		3,0		A
Total power dissipation up to $T_c = 25\ ^oC$	P_{tot}	max.		6.25		W
Storage temperature range	T_{stg}			−65 to + 150		^oC
Junction temperature	T_j	max.		150		^oC

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=		20		K/W

CHARACTERISTICS

$T_j = 25\ ^oC$ unless otherwise specified

			2N6659	2N6660	2N6661	
Drain-source breakdown voltage $I_D = 10\ \mu A; V_{GS} = 0$	$V_{(BR)DSS}$	min.	35	60	90	V
Drain-source leakage current at $V_{DS} = V_{DSmax}; V_{GS} = 0$	I_{DSS}	max.	10	10	10	μA
Gate-source leakage current at $V_{GS} = 15\ V; V_{DS} = 0$	I_{GSS}	max.	100	100	100	nA
Gate threshold voltage $I_D = 1\ mA; V_{DS} = V_{GS}$	$V_{GS(th)}$	min.	0.8	0.8	0.8	V
		max.	2.0	2.0	2.0	V
ON-state drain current $V_{DS} = 25\ V; V_{GS} = 10\ V$	$I_{D(on)}$	min.	1.0	1.0	1.0	A
		typ.	2.0	2.0	2.0	A
Drain-source ON-resistance $I_D = 0.3\ A; V_{GS} = 5\ V$	R_{DSon}	typ.	1.5	1.8	2.4	Ω
		max.	5.0	5.0	5.3	Ω
$I_D = 1.0\ A; V_{GS} = 10\ V$	R_{DSon}	typ.	0.9	1.4	1.9	Ω
		max.	1.8	3.0	4.0	Ω
Transfer admittance at f = 1 kHz $I_D = 0.5\ A; V_{DS} = 25\ V$	$\lvert y_{fs} \rvert$	min.	170	170	170	mS
Input capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{iss}	max.	50	50	50	pF
Output capacitance at f = 1 MHz $V_{DS} = 25\ V; V_{GS} = 0$	C_{oss}	max.	50	40	40	pF

Note

1. Pulse conditions: $t_p \leqslant 300\ \mu s; \delta = 0.01$.

		2N6659	2N6660	2N6661	
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss} max.	15	15	15	pF
Switching times I_D = 1.0 A; V_D = 25 V; V_{GS} = 0 to 10 V	t_{on} typ.	5	5	5	ns
	t_{on} max.	10	10	10	ns
	t_{off} typ.	5	5	5	ns
	t_{off} max.	10	10	10	ns

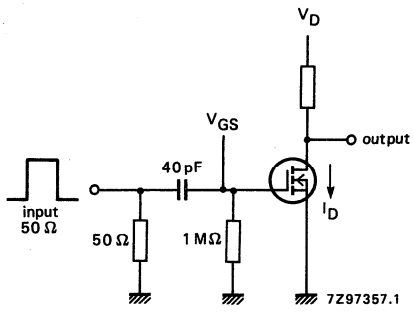


Fig. 2 Switching times test circuit.

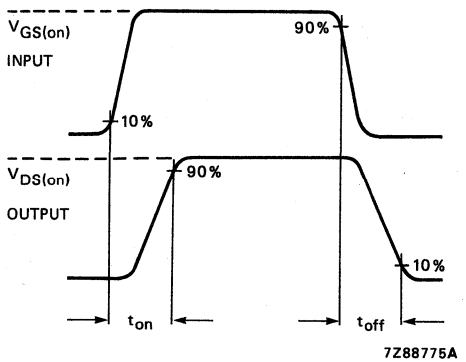


Fig. 3 Input and output waveforms.

Data sheet	
status	Product specification
date of issue	October 1990

2N7000

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

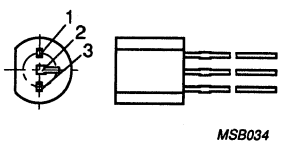
PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION



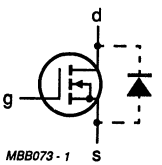


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

2N7000

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	280	mA
I_{DM}	drain current	peak value	–	1.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

N-channel enhancement mode vertical D-MOS transistor

2N7000

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	2.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns

N-channel enhancement mode vertical D-MOS transistor

2N7000

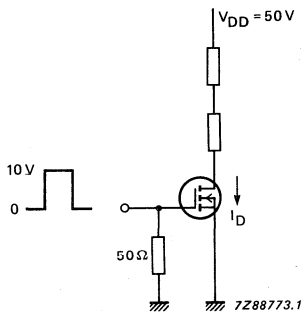


Fig.2 Switching time test circuit.

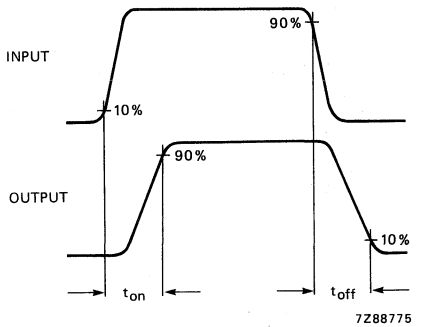


Fig.3 Input and output waveforms.

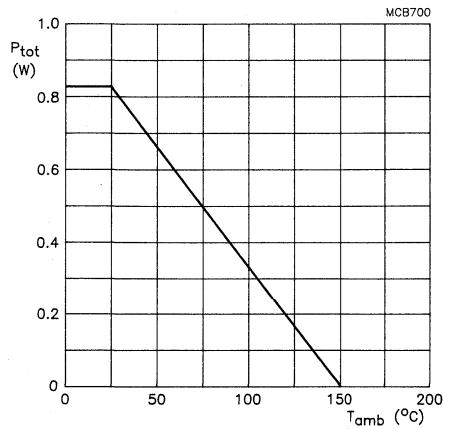


Fig.4 Power derating curve.

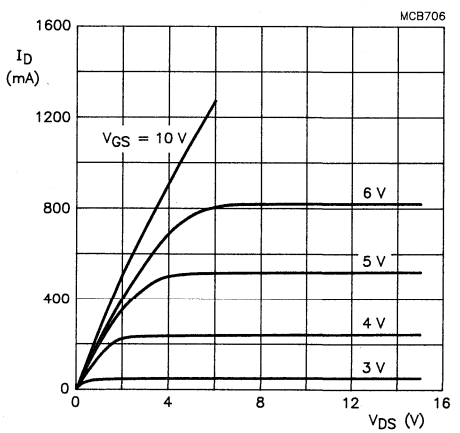


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

2N7000

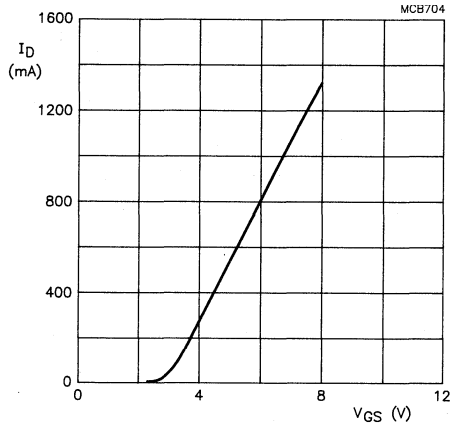


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

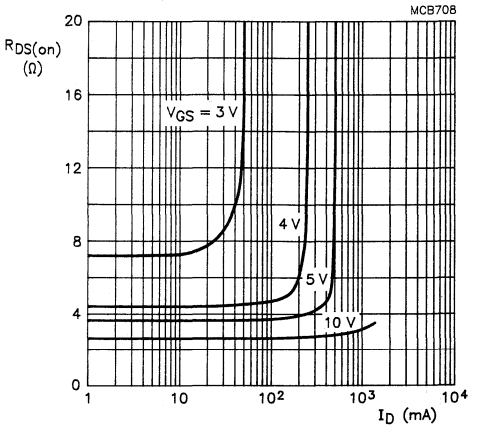


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

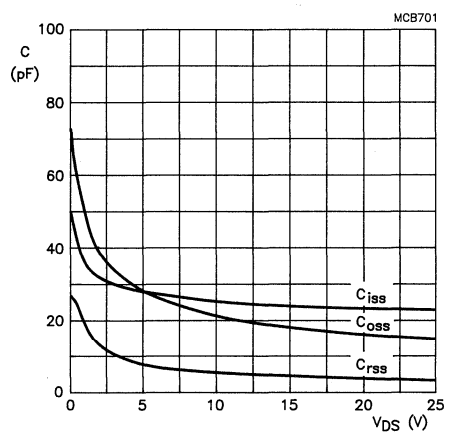
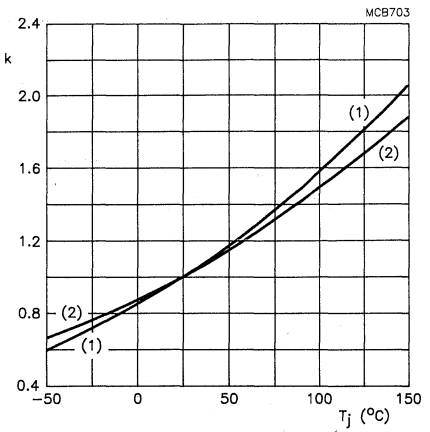


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

2N7000



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$.

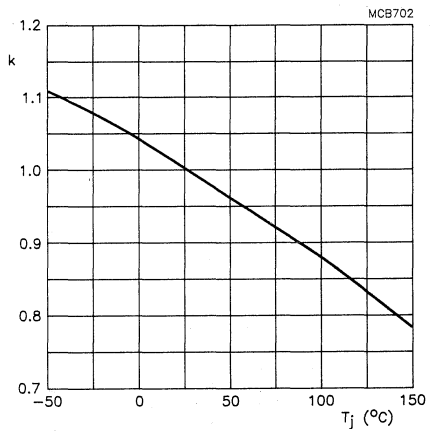
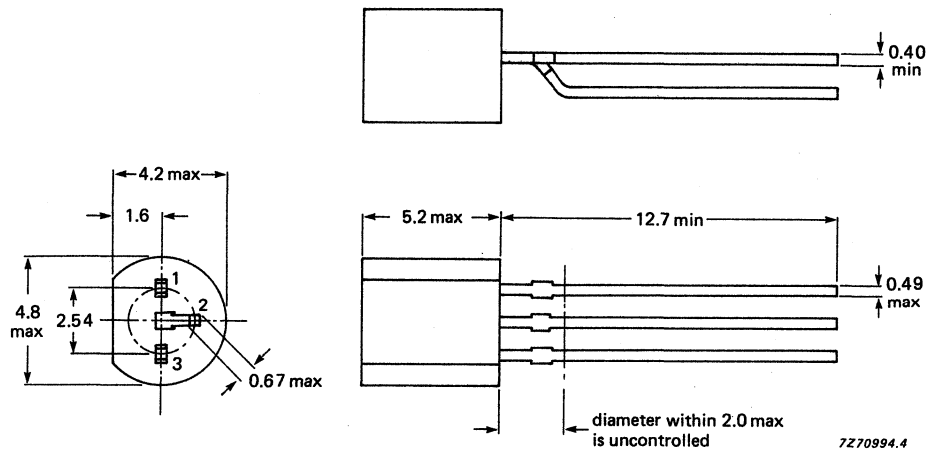


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

2N7000

PACKAGE OUTLINE



Dimensions in mm.

Fig.11 TO-92 variant.

Philips Components

Data sheet	
status	Product specification
date of issue	October 1990

2N7002
N-channel vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

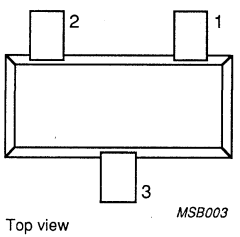
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION



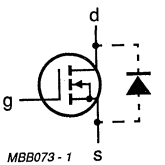


Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor

2N7002

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring 10 x 8 x 0.7 mm.
2. Mounted on a printed circuit board.

N-channel vertical D-MOS transistor

2N7002

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	2.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns

N-channel vertical D-MOS transistor

2N7002

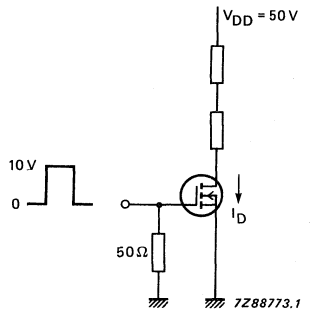


Fig.2 Switching time test circuit.

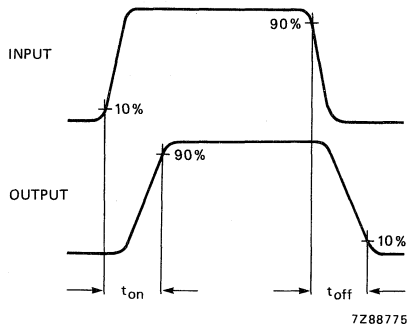
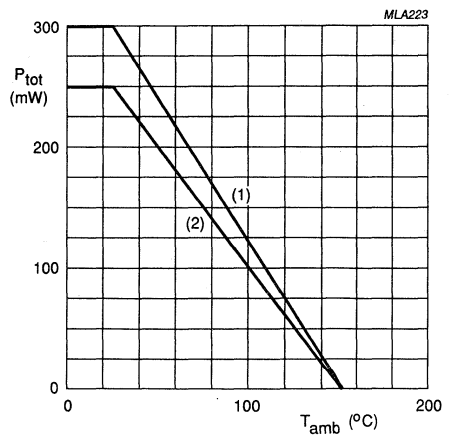


Fig.3 Input and output waveforms.



(1) On ceramic substrate.

(2) On printed circuit board.

Fig.4 Power derating curve.

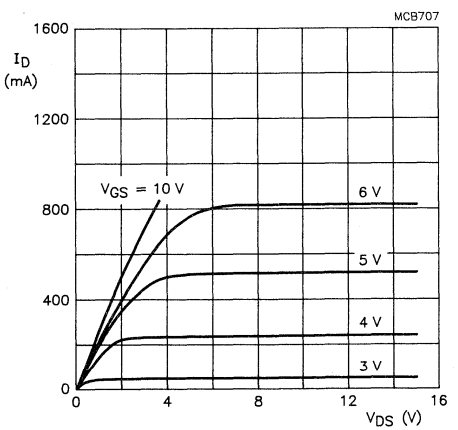


Fig.5 Typical output characteristics; T_j = 25 °C.

N-channel vertical D-MOS transistor

2N7002

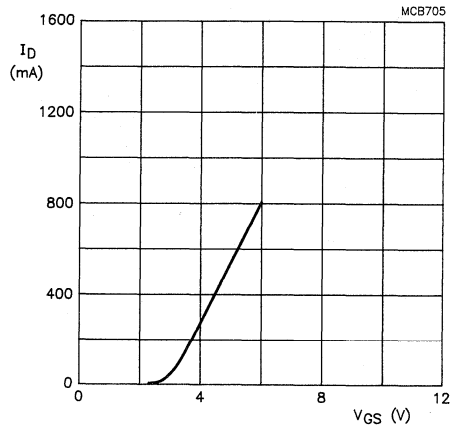


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

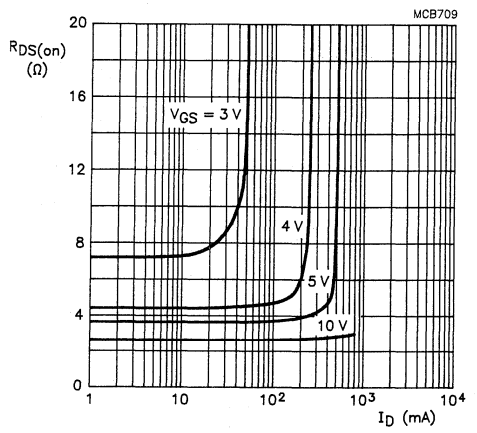


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

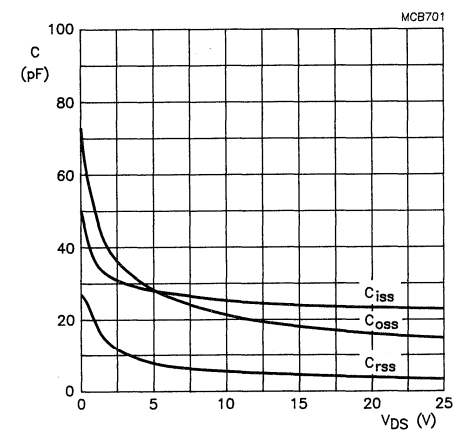
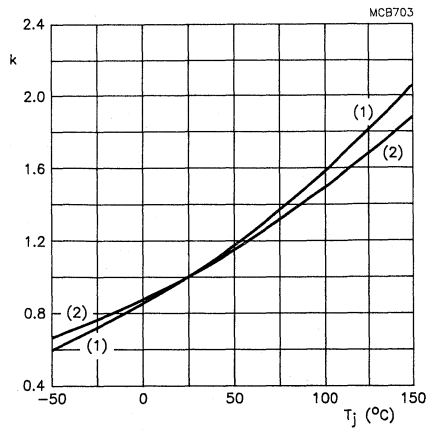


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel vertical D-MOS transistor

2N7002



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance; $k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$; typical $R_{DS(on)}$.

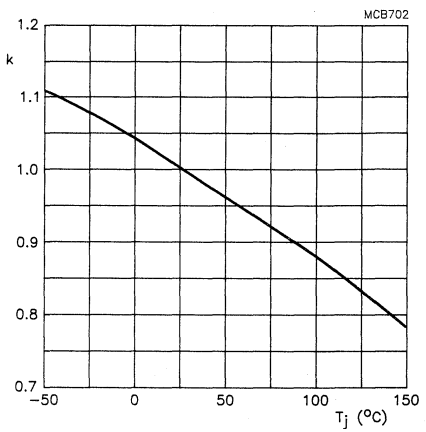
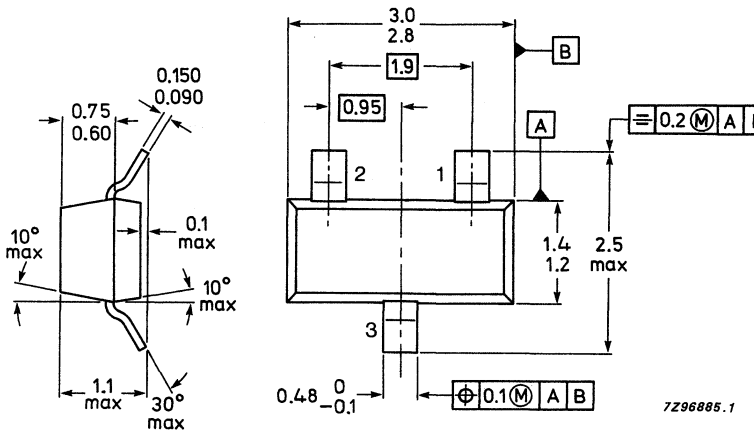


Fig.10 Temperature coefficient of gate-source threshold voltage; $k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$; typical $V_{GS(th)}$ at 1 mA.

N-channel vertical D-MOS transistor

2N7002

PACKAGE OUTLINE



TOP VIEW

Dimensions in mm.

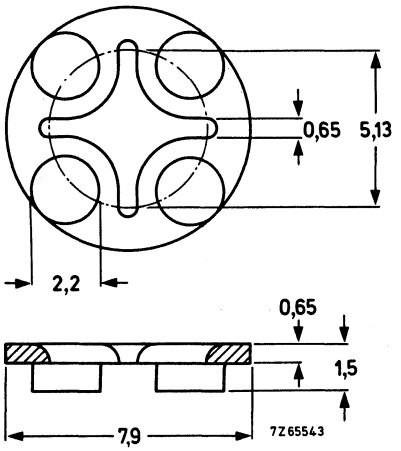
Marking code: 2N7002 = 702.

Fig.11 SOT23.

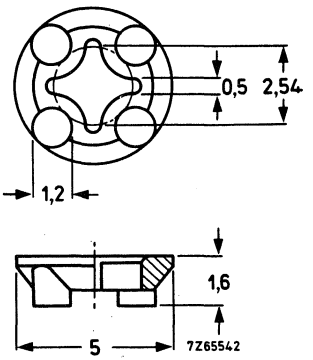
ACCESSORIES

MECHANICAL DATA

Dimensions in mm



Distance disc 56245 for TO-5 or TO-39; insulating material.

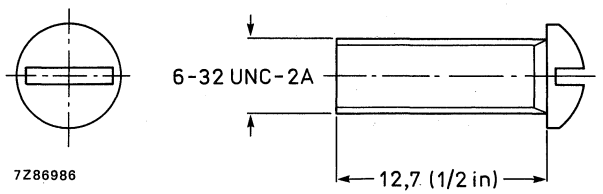


Distance disc 56246 for TO-18 or TO-72; insulating material.

Maximum permissible temperature: 100 °C.

ROUND HEAD SCREW 6-32 UNC-2A

Available, upon request, under type number 56396 or 12 NC code number 9390 298 10xx0.



INDEX

INDEX OF TYPE NUMBERS

The inclusion of a type number in this publication does not necessarily imply its availability.

Key to handbook sections

A	=	Accessories
FET	=	Field-effect transistors
I	=	Infrared devices
LED	=	Light-emitting diodes
LCD	=	Liquid crystal displays
Mm	=	Surface-mounted devices
M	=	Microwave transistors
P	=	Low-frequency power transistors and modules
PDT	=	Photodiodes or transistors
Ph	=	Photoconductive devices
PhC	=	Photocouplers
PM	=	Power MOS transistors
R	=	Rectifier diodes
RFP	=	RF power transistors and modules
RT	=	Triplers
Sen	=	Semiconductor sensors
SD	=	Small-signal diodes
Sm	=	Small-signal transistors
Sp	=	Special diodes
SP	=	Low-frequency switching power diodes
St	=	Rectifier stacks
T	=	Tuner diodes
Th	=	Thyristors
Tri	=	Triacs
TS	=	Transient suppressor diodes
Vrf	=	Voltage reference diodes
Vrg	=	Voltage regulator diodes
WBT	=	Wideband hybrid IC transistors
WBM	=	Wideband hybrid IC modules.

* series.

TYPE NUMBER	BOOK	SECTION
BA220	SC01	SD
BA221	SC01	SD
BA223	SC01	T
BA281	SC01	SD
BA314	SC01	Vrg
BA315	SC01	Vrg
BA316	SC01	SD
BA317	SC01	SD
BA318	SC01	SD
BA423	SC01	T
BA423L	SC01/10	T/Mm
BA480	SC01	T
BA481	SC01	T
BA482	SC01	T
BA483	SC01	T
BA484	SC01	T
BA682	SC01/10	T/Mm
BA683	SC01/10	T/Mm
BAS11	SC01	SD
BAS15	SC01	SD
BAS16	SC01/10	SD/Mm
BAS17	SC01/10	Vrg/Mm
BAS19	SC01/10	SD/Mm
BAS20	SC01/10	SD/Mm
BAS21	SC01/10	SD/Mm
BAS28	SC01/10	SD/Mm
BAS29	SC01/10	SD/Mm
BAS31	SC01/10	SD/Mm
BAS32	SC01/10	SD/Mm
BAS32L	SC01/10	SD/Mm
BAS35	SC01/10	SD/Mm
BAS45	SC01	SD
BAS45L	SC01/10	SD/Mm
BAS56	SC01/10	SD/Mm
BAS85	SC01/10	SD/Mm
BAS86	SC01/10	SD/Mm
BAT17	SC01/10	T/Mm
BAT18	SC01/10	T/Mm
BAT54	SC01/10	SD/Mm
BAT54A	SC01/10	SD/Mm

TYPE NUMBER	BOOK	SECTION
BAT54C	SC01/10	SD/Mm
BAT54S	SC01/10	SD/Mm
BAT74	SC01/10	SD/Mm
BAT81	SC01	T
BAT82	SC01	T
BAT83	SC01	T
BAT85	SC01	T
BAT86	SC01	T
BAV10	SC01	SD
BAV18	SC01	SD
BAV19	SC01	SD
BAV20	SC01	SD
BAV21	SC01	SD
BAV23	SC01/10	SD/Mm
BAV45	SC01	Sp
BAV70	SC01/10	SD/Mm
BAV74	SC01/10	SD/Mm
BAV99	SC01/10	SD/Mm
BAV100	SC01/10	SD/Mm
BAV101	SC01/10	SD/Mm
BAV102	SC01/10	SD/Mm
BAV103	SC01/10	SD/Mm
BAV105	SC01/10	SD/Mm
BAW56	SC01/10	SD/Mm
BAW62	SC01	SD
BAX12	SC01	SD
BAX14	SC01	SD
BAX18	SC01	SD
BAY80	SC01	SD
BB112	SC01	T
BB119	SC01	T
BB130	SC01	T
BB204B	SC01	T
BB204G	SC01	T
BB212	SC01	T
BB215	SC01/10	SD/Mm
BB219	SC01/10	SD/Mm
BB240	SC01/10	T/Mm
BB241	SC01/10	T/Mm
BB249	SC01/10	T/Mm

TYPE NUMBER	BOOK	SECTION
BB405B	SC01	T
BB417	SC01	T
BB804	SC01/10	T/Mm
BB809	SC01	T
BB909A	SC01	T
BB909B	SC01	T
BB910	SC01	T
BB911	SC01	T
BBY31	SC01/10	T/Mm
BBY39	SC01/10	T/Mm
BBY40	SC01/10	T/Mm
BBY42	SC01/10	T/Mm
BBY62	SC01/10	T/Mm
BC107	SC04	Sm
BC108	SC04	Sm
BC109	SC04	Sm
BC140	SC04	Sm
BC141	SC04	Sm
BC160	SC04	Sm
BC161	SC04	Sm
BC177	SC04	Sm
BC178	SC04	Sm
BC179	SC04	Sm
BC264A	SC07	FET
BC264B	SC07	FET
BC246C	SC07	FET
BC264D	SC07	FET
BC327	SC04	Sm
BC327A	SC04	Sm
BC328	SC04	Sm
BC337	SC04	Sm
BC337A	SC04	Sm
BC338	SC04	Sm
BC368	SC04	Sm
BC369	SC04	Sm
BC375	SC04	Sm
BC376	SC04	Sm
BC516	SC04	Sm
BC517	SC04	Sm
BC546	SC04	Sm

TYPE NUMBER	BOOK	SECTION
BC547	SC04	Sm
BC548	SC04	Sm
BC549	SC04	Sm
BC550	SC04	Sm
BC556	SC04	Sm
BC557	SC04	Sm
BC558	SC04	Sm
BC559	SC04	Sm
BC560	SC04	Sm
BC617	SC04	Sm
BC618	SC04	Sm
BC635	SC04	Sm
BC636	SC04	Sm
BC637	SC04	Sm
BC638	SC04	Sm
BC639	SC04	Sm
BC640	SC04	Sm
BC807	SC10	Mm
BC808	SC10	Mm
BC817	SC10	Mm
BC818	SC10	Mm
BC846	SC10	Mm
BC847	SC10	Mm
BC848	SC10	Mm
BC849	SC10	Mm
BC850	SC10	Mm
BC856	SC10	Mm
BC857	SC10	Mm
BC858	SC10	Mm
BC859	SC10	Mm
BC860	SC10	Mm
BC868	SC10	Mm
BC869	SC10	Mm
BC875	SC04	Sm
BC876	SC04	Sm
BC877	SC04	Sm
BC878	SC04	Sm
BC879	SC04	Sm
BC880	SC04	Sm
BCF29	SC10	Mm

TYPE NUMBER	BOOK	SECTION
BCF29R	SC10	Mm
BCF30	SC10	Mm
BCF30R	SC10	Mm
BCF32	SC10	Mm
BCF32R	SC10	Mm
BCF33	SC10	Mm
BCF33R	SC10	Mm
BCF70	SC10	Mm
BCF70R	SC10	Mm
BCF81	SC10	Mm
BCF81R	SC10	Mm
BCP51	SC10	Mm
BCP52	SC10	Mm
BCP53	SC10	Mm
BCP54	SC10	Mm
BCP55	SC10	Mm
BCP56	SC10	Mm
BCP68	SC10	Mm
BCP69	SC10	Mm
BCV26	SC10	Mm
BCV27	SC10	Mm
BCV28	SC10	Mm
BCV29	SC10	Mm
BCV46	SC10	Mm
BCV47	SC10	Mm
BCV48	SC10	Mm
BCV49	SC10	Mm
BCV61	SC10	Mm
BCV62	SC10	Mm
BCV63	SC10	Mm
BCV64	SC10	Mm
BCV65	SC10	Mm
BCV71	SC10	Mm
BCV71R	SC10	Mm
BCV72	SC10	Mm
BCV72R	SC10	Mm
BCW29	SC10	Mm
BCW29R	SC10	Mm
BCW30	SC10	Mm
BCW30R	SC10	Mm

TYPE NUMBER	BOOK	SECTION
BCW31	SC10	Mm
BCW31R	SC10	Mm
BCW32	SC10	Mm
BCW32R	SC10	Mm
BCW33	SC10	Mm
BCW33R	SC10	Mm
BCW60*	SC10	Mm
BCW61*	SC10	Mm
BCW69	SC10	Mm
BCW69R	SC10	Mm
BCW70	SC10	Mm
BCW70R	SC10	Mm
BCW71	SC10	Mm
BCW71R	SC10	Mm
BCW72	SC10	Mm
BCW72R	SC10	Mm
BCW81	SC10	Mm
BCW81R	SC10	Mm
BCW89	SC10	Mm
BCW89R	SC10	Mm
BCX17	SC10	Mm
BCX17R	SC10	Mm
BCX18	SC10	Mm
BCX18R	SC10	Mm
BCX19	SC10	Mm
BCX19R	SC10	Mm
BCX20	SC10	Mm
BCX20R	SC10	Mm
BCX22	SC04	Sm
BCX23	SC04	Sm
BCX51	SC10	Mm
BCX52	SC10	Mm
BCX53	SC10	Mm
BCX54	SC10	Mm
BCX55	SC10	Mm
BCX56	SC10	Mm
BCX58	SC04	Sm
BCX59	SC04	Sm
BCX70*	SC10	Mm
BCX71*	SC10	Mm

TYPE NUMBER	BOOK	SECTION
BCX78	SC04	Sm
BCX79	SC04	Sm
BCY56	SC04	Sm
BCY57	SC04	Sm
BCY58	SC04	Sm
BCY59	SC04	Sm
BCY65	SC04	Sm
BCY70	SC04	Sm
BCY71	SC04	Sm
BCY72	SC04	Sm
BCY78	SC04	Sm
BCY79	SC04	Sm
BCY87	SC04	Sm
BCY88	SC04	Sm
BCY89	SC04	Sm
BD131	SC05	P
BD132	SC05	P
BD135	SC05	P
BD136	SC05	P
BD137	SC05	P
BD138	SC05	P
BD139	SC05	P
BD140	SC05	P
BD201	SC05	P
BD201F	SC05	P
BD202	SC05	P
BD202F	SC05	P
BD203	SC05	P
BD203F	SC05	P
BD204	SC05	P
BD204F	SC05	P
BD226	SC05	P
BD227	SC05	P
BD228	SC05	P
BD229	SC05	P
BD230	SC05	P
BD231	SC05	P
BD233	SC05	P
BD234	SC05	P
BD235	SC05	P

TYPE NUMBER	BOOK	SECTION
BD236	SC05	P
BD237	SC05	P
BD238	SC05	P
BD239	SC05	P
BD239A	SC05	P
BD239B	SC05	P
BD239C	SC05	P
BD240	SC05	P
BD240A	SC05	P
BD240B	SC05	P
BD240C	SC05	P
BD241	SC05	P
BD241A	SC05	P
BD241B	SC05	P
BD241C	SC05	P
BD242	SC05	P
BD242A	SC05	P
BD242B	SC05	P
BD242C	SC05	P
BD243	SC05	P
BD243A	SC05	P
BD243B	SC05	P
BD243C	SC05	P
BD244	SC05	P
BD244A	SC05	P
BD244B	SC05	P
BD244C	SC05	P
BD329	SC05	P
BD330	SC05	P
BD331	SC05	P
BD332	SC05	P
BD333	SC05	P
BD334	SC05	P
BD335	SC05	P
BD336	SC05	P
BD337	SC05	P
BD338	SC05	P
BD433	SC05	P
BD434	SC05	P
BD435	SC05	P

TYPE NUMBER	BOOK	SECTION
BD436	SC05	P
BD437	SC05	P
BD438	SC05	P
BD643	SC05	P
BD643F	SC05	P
BD644	SC05	P
BD644F	SC05	P
BD645	SC05	P
BD645F	SC05	P
BD646	SC05	P
BD646F	SC05	P
BD647	SC05	P
BD647F	SC05	P
BD648	SC05	P
BD648F	SC05	P
BD649	SC05	P
BD649F	SC05	P
BD650	SC05	P
BD650F	SC05	P
BD651	SC05	P
BD651F	SC05	P
BD652	SC05	P
BD652F	SC05	P
BD675	SC05	P
BD676	SC05	P
BD677	SC05	P
BD678	SC05	P
BD679	SC05	P
BD680	SC05	P
BD681	SC05	P
BD682	SC05	P
BD683	SC05	P
BD684	SC05	P
BD719	SC05	P
BD720	SC05	P
BD721	SC05	P
BD722	SC05	P
BD723	SC05	P
BD724	SC05	P
BD725	SC05	P

TYPE NUMBER	BOOK	SECTION
BD726	SC05	P
BD825	SC05	P
BD826	SC05	P
BD827	SC05	P
BD828	SC05	P
BD829	SC05	P
BD830	SC05	P
BD839	SC05	P
BD840	SC05	P
BD841	SC05	P
BD842	SC05	P
BD843	SC05	P
BD844	SC05	P
BD933	SC05	P
BD933F	SC05	P
BD934	SC05	P
BD934F	SC05	P
BD935	SC05	P
BD935F	SC05	P
BD936	SC05	P
BD936F	SC05	P
BD937	SC05	P
BD937F	SC05	P
BD938	SC05	P
BD938F	SC05	P
BD939	SC05	P
BD939F	SC05	P
BD940	SC05	P
BD940F	SC05	P
BD941	SC05	P
BD941F	SC05	P
BD942	SC05	P
BD942F	SC05	P
BD943	SC05	P
BD943F	SC05	P
BD944	SC05	P
BD944F	SC05	P
BD945	SC05	P
BD945F	SC05	P
BD946	SC05	P

TYPE NUMBER	BOOK	SECTION
BD946F	SC05	P
BD947	SC05	P
BD947F	SC05	P
BD948	SC05	P
BD948F	SC05	P
BD949	SC05	P
BD949F	SC05	P
BD950	SC05	P
BD950F	SC05	P
BD951	SC05	P
BD951F	SC05	P
BD952	SC05	P
BD952F	SC05	P
BD953	SC05	P
BD953F	SC05	P
BD954	SC05	P
BD954F	SC05	P
BD955	SC05	P
BD955F	SC05	P
BD956	SC05	P
BD956F	SC05	P
BDS60	SC05/10	P/Mm
BDS60A	SC05/10	P/Mm
BDS60B	SC05/10	P/Mm
BDS60C	SC05/10	P/Mm
BDS61	SC05/10	P/Mm
BDS61A	SC05/10	P/Mm
BDS61B	SC05/10	P/Mm
BDS61C	SC05/10	P/Mm
BDX77	SC05/10	P/Mm
BDX78	SC05/10	P/Mm
BDS201	SC05/10	P/Mm
BDS202	SC05/10	P/Mm
BDS203	SC05/10	P/Mm
BDS204	SC05/10	P/Mm
BDS643	SC05/10	P/Mm
BDS644	SC05/10	P/Mm
BDS645	SC05/10	P/Mm
BDS646	SC05/10	P/Mm
BDS647	SC05/10	P/Mm

TYPE NUMBER	BOOK	SECTION
BDS648	SC05/10	P/Mm
BDS649	SC05/10	P/Mm
BDS650	SC05/10	P/Mm
BDS651	SC05/10	P/Mm
BDS652	SC05/10	P/Mm
BDS933	SC05/10	P/Mm
BDS934	SC05/10	P/Mm
BDS935	SC05/10	P/Mm
BDS936	SC05/10	P/Mm
BDS937	SC05/10	P/Mm
BDS938	SC05/10	P/Mm
BDS939	SC05/10	P/Mm
BDS940	SC05/10	P/Mm
BDS941	SC05/10	P/Mm
BDS942	SC05/10	P/Mm
BDS943	SC05/10	P/Mm
BDS944	SC05/10	P/Mm
BDS945	SC05/10	P/Mm
BDS946	SC05/10	P/Mm
BDS947	SC05/10	P/Mm
BDS948	SC05/10	P/Mm
BDS950	SC05/10	P/Mm
BDS951	SC05/10	P/Mm
BDS952	SC05/10	P/Mm
BDT29	SC05/10	P/Mm
BDT29F	SC05	P
BDT29A	SC05	P
BDT29AF	SC05	P
BDT29B	SC05	P
BDT29BF	SC05	P
BDT29C	SC05	P
BDT29CF	SC05	P
BDT30	SC05	P
BDT30F	SC05	P
BDT30A	SC05	P
BDT30AF	SC05	P
BDT30B	SC05	P
BDT30BF	SC05	P
BDT30C	SC05	P
BDT30CF	SC05	P

TYPE NUMBER	BOOK	SECTION
BDT31	SC05	P
BDT31F	SC05	P
BDT31A	SC05	P
BDT31AF	SC05	P
BDT31B	SC05	P
BDT31BF	SC05	P
BDT31C	SC05	P
BDT31CF	SC05	P
BDT31D	SC05	P
BDT31DF	SC05	P
BDT32	SC05	P
BDT32F	SC05	P
BDT32A	SC05	P
BDT32AF	SC05	P
BDT32B	SC05	P
BDT32BF	SC05	P
BDT32C	SC05	P
BDT32CF	SC05	P
BDT32D	SC05	P
BDT32DF	SC05	P
BDT41A	SC05	P
BDT41AF	SC05	P
BDT41B	SC05	P
BDT41BF	SC05	P
BDT41C	SC05	P
BDT41CF	SC05	P
BDT42	SC05	P
BDT42F	SC05	P
BDT42A	SC05	P
BDT42AF	SC05	P
BDT42B	SC05	P
BDT42BF	SC05	P
BDT42C	SC05	P
BDT42CF	SC05	P
BDT60	SC05	P
BDT60F	SC05	P
BDT60A	SC05	P
BDT60AF	SC05	P
BDT60B	SC05	P
BDT60BF	SC05	P

TYPE NUMBER	BOOK	SECTION
BDT60C	SC05	P
BDT60CF	SC05	P
BDT61	SC05	P
BDT61F	SC05	P
BDT61A	SC05	P
BDT61AF	SC05	P
BDT61B	SC05	P
BDT61BF	SC05	P
BDT61C	SC05	P
BDT61CF	SC05	P
BDT62	SC05	P
BDT62F	SC05	P
BDT62A	SC05	P
BDT62AF	SC05	P
BDT62B	SC05	P
BDT62BF	SC05	P
BDT62C	SC05	P
BDT62CF	SC05	P
BDT63	SC05	P
BDT63F	SC05	P
BDT63A	SC05	P
BDT63AF	SC05	P
BDT63B	SC05	P
BDT63BF	SC05	P
BDT63C	SC05	P
BDT63CF	SC05	P
BDT64	SC05	P
BDT64F	SC05	P
BDT64A	SC05	P
BDT64AF	SC05	P
BDT64B	SC05	P
BDT64BF	SC05	P
BDT64C	SC05	P
BDT64CF	SC05	P
BDT65	SC05	P
BDT65F	SC05	P
BDT65A	SC05	P
BDT65AF	SC05	P
BDT65B	SC05	P
BDT65BF	SC05	P

TYPE NUMBER	BOOK	SECTION
BDT65C	SC05	P
BDT65CF	SC05	P
BDT81	SC05	P
BDT81F	SC05	P
BDT82	SC05	P
BDT82F	SC05	P
BDT83	SC05	P
BDT83F	SC05	P
BDT84	SC05	P
BDT84F	SC05	P
BDT85	SC05	P
BDT85F	SC05	P
BDT86	SC05	P
BDT86F	SC05	P
BDT87	SC05	P
BDT87F	SC05	P
BDT88	SC05	P
BDT88F	SC05	P
BDT91	SC05	P
BDT91F	SC05	P
BDT92	SC05	P
BDT92F	SC05	P
BDT93	SC05	P
BDT93F	SC05	P
BDT94	SC05	P
BDT94F	SC05	P
BDT95	SC05	P
BDT95F	SC05	P
BDT96	SC05	P
BDT96F	SC05	P
BDV64	SC05	P
BDV64A	SC05	P
BDV64B	SC05	P
BDV64C	SC05	P
BDV65	SC05	P
BDV65A	SC05	P
BDV65B	SC05	P
BDV65C	SC05	P
BDV66A	SC05	P
BDV66B	SC05	P

TYPE NUMBER	BOOK	SECTION
BDV66C	SC05	P
BDV66D	SC05	P
BDV67A	SC05	P
BDV67B	SC05	P
BDV67C	SC05	P
BDV67D	SC05	P
BDV91	SC05	P
BDV92	SC05	P
BDV93	SC05	P
BDV94	SC05	P
BDV95	SC05	P
BDV96	SC05	P
BDX35	SC05	P
BDX36	SC05	P
BDX37	SC05	P
BDX42	SC05	P
BDX43	SC05	P
BDX44	SC05	P
BDX45	SC05	P
BDX46	SC05	P
BDX47	SC05	P
BDX62	SC05	P
BDX62A	SC05	P
BDX62B	SC05	P
BDX62C	SC05	P
BDX63	SC05	P
BDX63A	SC05	P
BDX63B	SC05	P
BDX63C	SC05	P
BDX64	SC05	P
BDX64A	SC05	P
BDX64B	SC05	P
BDX64C	SC05	P
BDX65	SC05	P
BDX65A	SC05	P
BDX65B	SC05	P
BDX65C	SC05	P
BDX66	SC05	P
BDX66A	SC05	P
BDX66B	SC05	P

TYPE NUMBER	BOOK	SECTION
BDX66C	SC05	P
BDX67	SC05	P
BDX67A	SC05	P
BDX67B	SC05	P
BDX67C	SC05	P
BDX68	SC05	P
BDX68A	SC05	P
BDX68B	SC05	P
BDX68C	SC05	P
BDX69	SC05	P
BDX69A	SC05	P
BDX69B	SC05	P
BDX69C	SC05	P
BDX77	SC05	P
BDX77F	SC05	P
BDX78	SC05	P
BDX78F	SC05	P
BDX91	SC05	P
BDX92	SC05	P
BDX93	SC05	P
BDX94	SC05	P
BDX95	SC05	P
BDX96	SC05	P
BDY90	SC05	P
BDY91	SC05	P
BDY92	SC05	P
BF198	SC04	Sm
BF199	SC04	Sm
BF240	SC04	Sm
BF241	SC04	Sm
BF245A	SC07	FET
BF245B	SC07	FET
BF245C	SC07	FET
BF246A	SC07	FET
BF246B	SC07	FET
BF246C	SC07	FET
BF247A	SC07	FET
BF247B	SC07	FET
BF247C	SC07	FET
BF256A	SC07	FET

TYPE NUMBER	BOOK	SECTION
BF256B	SC07	FET
BF256C	SC07	FET
BF324	SC04	Sm
BF370	SC04	Sm
BF410A	SC07	FET
BF410B	SC07	FET
BF410C	SC07	FET
BF410D	SC07	FET
BF420	SC04	Sm
BF421	SC04	Sm
BF422	SC04	Sm
BF423	SC04	Sm
BF450	SC04	Sm
BF451	SC04	Sm
BF483	SC04	Sm
BF485	SC04	Sm
BF486	SC04	Sm
BF487	SC04	Sm
BF488	SC04	Sm
BF494	SC04	Sm
BF495	SC04	Sm
BF496	SC04	Sm
BF510	SC07/10	FET/Mm
BF511	SC07/10	FET/Mm
BF512	SC07/10	FET/Mm
BF513	SC07/10	FET/Mm
BF550	SC10	Mm
BF550R	SC10	Mm
BF569	SC10	Mm
BF570	SC10	Mm
BF579	SC10	Mm
BF620	SC10	Mm
BF621	SC10	Mm
BF622	SC10	Mm
BF623	SC10	Mm
BF660	SC10	Mm
BF660R	SC10	Mm
BF689K	SC14	WBT
BF720	SC10	Mm
BF721	SC10	Mm

TYPE NUMBER	BOOK	SECTION
BF722	SC10	Mm
BF723	SC10	Mm
BF747	SC14/10	WBT/Mm
BF763	SC14	WBT
BF820	SC10	Mm
BF821	SC10	Mm
BF822	SC10	Mm
BF823	SC10	Mm
BF824	SC10	Mm
BF840	SC10	Mm
BF841	SC10	Mm
BF926	SC04	Sm
BF960	SC07	FET
BF964S	SC07	FET
BF965	SC07	FET
BF966S	SC07	FET
BF970	SC04	Sm
BF970A	SC04	Sm
BF979	SC04	Sm
BF980A	SC07	FET
BF981	SC07	FET
BF982	SC07	FET
BF988	SC07/10	FET/Mm
BF989	SC07/10	FET/Mm
BF990A	SC07/10	FET/Mm
BF990AR	SC07/10	FET/Mm
BF991	SC07/10	FET/Mm
BF992	SC07/10	FET/Mm
BF992R	SC07/10	FET/Mm
BF994S	SC07/10	FET/Mm
BF996S	SC07/10	FET/Mm
BF997	SC07/10	FET/Mm
BF998	SC07/10	FET/Mm
BF998R	SC07/10	FET/Mm
BFG16A	SC14/10	WBT/Mm
BFG17A	SC14/10	WBT/Mm
BFG23	SC14	WBT
BFG25AX	SC14/10	WBT/Mm
BFG31	SC14/10	WBT/Mm
BFG32	SC14	WBT

TYPE NUMBER	BOOK	SECTION
BFG33	SC14/10	WBT/Mm
BFG33X	SC14/10	WBT/Mm
BFG34	SC14	WBT
BFG35	SC14/10	WBT/Mm
BFG51	SC14	WBT
BFG65	SC14	WBT
BFG67	SC14/10	WBT/Mm
BFG67X	SC14/10	WBT/Mm
BFG90A	SC14	WBT
BFG91A	SC14	WBT
BFG92A	SC14/10	WBT/Mm
BFG92AX	SC14/10	WBT/Mm
BFG93A	SC14/10	WBT/Mm
BFG93AX	SC14/10	WBT/Mm
BFG94	SC14/10	WBT/Mm
BFG96	SC14	WBT
BFG97	SC14/10	WBT/Mm
BFG135	SC14/10	WBT/Mm
BFG195	SC14	WBT
BFG197	SC14/10	WBT/Mm
BFG197X	SC14/10	WBT/Mm
BFG198	SC14/10	WBT/Mm
BFP90A	SC14	WBT
BFP91A	SC14	WBT
BFP96	SC14	WBT
BFQ10	SC07	FET
BFQ11	SC07	FET
BFQ12	SC07	FET
BFQ13	SC07	FET
BFQ14	SC07	FET
BFQ15	SC07	FET
BFQ16	SC07	FET
BFQ17	SC14/10	WBT/Mm
BFQ18A	SC14/10	WBT/Mm
BFQ19	SC14/10	WBT/Mm
BFQ22S	SC14	WBT
BFQ23	SC14	WBT
BFQ23C	SC14	WBT
BFQ24	SC14	WBT
BFQ32	SC14	WBT

TYPE NUMBER	BOOK	SECTION
BFQ32C	SC14	WBT
BFQ32M	SC14	WBT
BFQ32S	SC14	WBT
BFQ33	SC14	WBT
BFQ33C	SC14	WBT
BFQ34	SC14	WBT
BFQ34T	SC14	WBT
BFQ42	SC08a	RFP
BFQ43	SC08a	RFP
BFQ43S	SC08a	RFP
BFQ51	SC14	WBT
BFQ51C	SC14	WBT
BFQ52	SC14	WBT
BFQ53	SC14	WBT
BFQ63	SC14	WBT
BFQ65	SC14	WBT
BFQ66	SC14	WBT
BFQ67	SC14/10	WBT/Mm
BFQ68	SC14	WBT
BFQ135	SC14	WBT
BFQ136	SC14	WBT
BFQ149	SC14/10	WBT/Mm
BFQ161	SC14	WBT
BFQ162	SC14	WBT
BFQ163	SC14	WBT
BFQ231	SC14	WBT
BFQ231A	SC14	WBT
BFQ232	SC14	WBT
BFQ232A	SC14	WBT
BFQ233	SC14	WBT
BFQ233A	SC14	WBT
BFQ234	SC14	WBT
BFQ235	SC14	WBT
BFQ235A	SC14	WBT
BFQ251	SC14	WBT
BFQ251A	SC14	WBT
BFQ252	SC14	WBT
BFQ252A	SC14	WBT
BFQ253	SC14	WBT
BFQ253A	SC14	WBT

TYPE NUMBER	BOOK	SECTION
BFQ254	SC14	WBT
BFQ255	SC14	WBT
BFQ255A	SC14	WBT
BFQ262	SC14	WBT
BFQ262A	SC14	WBT
BFQ263	SC14	WBT
BFQ263A	SC14	WBT
BFQ265	SC14	WBT
BFQ265A	SC14	WBT
BFQ268	SC14	WBT
BFQ270	SC14	WBT
BFR29	SC07	FET
BFR30	SC07/10	FET/Mm
BFR31	SC07/10	FET/Mm
BFR49	SC14	WBT
BFR53	SC14/10	WBT/Mm
BFR54	SC04	Sm
BFR64	SC14	WBT
BFR65	SC14	WBT
BFR84	SC07	FET
BFR90	SC14	WBT
BFR90A	SC14	WBT
BFR91	SC14	WBT
BFR91A	SC14	WBT
BFR92	SC14/10	WBT/Mm
BFR92A	SC14/10	WBT/Mm
BFR93	SC14/10	WBT/Mm
BFR93A	SC14/10	WBT/Mm
BFR94	SC14	WBT
BFR95	SC14	WBT
BFR96	SC14	WBT
BFR96S	SC14	WBT
BFR106	SC14/10	WBT/Mm
BFR101A	SC07/10	FET/Mm
BFR101B	SC07/10	FET/Mm
BFR134	SC14	WBT
BFR200	SC07/10	FET/Mm
BFS17	SC14/10	WBT
BFS17A	SC14	WBT
BFS18	SC10	Mm

TYPE NUMBER	BOOK	SECTION
BFS18R	SC10	Mm
BFS19	SC10	Mm
BFS19R	SC10	Mm
BFS20	SC10	Mm
BFS20R	SC10	Mm
BFS21	SC07	FET
BFS21A	SC07	FET
BFS22A	SC08a	RFP
BFS23A	SC08a	RFP
BFT24	SC14	WBT
BFT25	SC14/10	WBT/Mm
BFT25A	SC14	WBT
BFT44	SC04	Sm
BFT45	SC04	Sm
BFT46	SC07/10	FET/Mm
BFT92	SC14/10	WBT/Mm
BFT93	SC14/10	WBT/Mm
BFW10	SC07	FET
BFW11	SC07	FET
BFW12	SC07	FET
BFW13	SC07	FET
BFW16A	SC14	WBT
BFW17A	SC14	WBT
BFW30	SC14	WBT
BFW61	SC07	FET
BFW92	SC14	WBT
BFW92A	SC14	WBT
BFW93	SC14	WBT
BFX29	SC04	Sm
BFX30	SC04	Sm
BFX34	SC04	Sm
BFX84	SC04	Sm
BFX85	SC04	Sm
BFX87	SC04	Sm
BFX88	SC04	Sm
BFX89	SC14	WBT
BFY50	SC04	Sm
BFY51	SC04	Sm
BFY52	SC04	Sm
BFY55	SC04	Sm

TYPE NUMBER	BOOK	SECTION
BFY90	SC14	WBT
BG2000	SC01	RT
BG2097	SC01	RT
BGD102	SC14	WBM
BGD102E	SC14	WBM
BGD104	SC14	WBM
BGD104E	SC14	WBM
BGD106	SC14	WBM
BGD108	SC14	WBM
BGD502	SC14	WBM
BGD504	SC14	WBM
BGD506	SC14	WBM
BGD508	SC14	WBM
BGE85A	SC14	WBM
BGE88	SC14	WBM
BGE88-01	SC14	WBM
BGE885	SC14	WBM
BGE887	SC14	WBM
BGX885	SC14	WBM
BGY22	SC09	RFP
BGY22A	SC09	RFP
BGY23	SC09	RFP
BGY23A	SC09	RFP
BGY32	SC09	RFP
BGY33	SC09	RFP
BGY35	SC09	RFP
BGY36	SC09	RFP
BGY40A	SC09	RFP
BGY40B	SC09	RFP
BGY41A	SC09	RFP
BGY41B	SC09	RFP
BGY43	SC09	RFP
BGY45A	SC09	RFP
BGY45B	SC09	RFP
BGY45C	SC09	RFP
BGY46A	SC09	RFP
BGY46B	SC09	RFP
BGY47A	SC09	RFP
BGY47F	SC09	RFP
BGY48A	SC09	RFP

TYPE NUMBER	BOOK	SECTION
BGY48B	SC09	RFP
BGY48C	SC09	RFP
BGY49A	SC09	RFP
BGY49B	SC09	RFP
BGY50	SC14	WBM
BGY51	SC14	WBM
BGY52	SC14	WBM
BGY53	SC14	WBM
BGY54	SC14	WBM
BGY55	SC14	WBM
BGY56	SC14	WBM
BGY57	SC14	WBM
BGY58	SC14	WBM
BGY58A	SC14	WBM
BGY59	SC14	WBM
BGY60	SC14	WBM
BGY61	SC14	WBM
BGY65	SC14	WBM
BGY67	SC14	WBM
BGY67A	SC14	WBM
BGY70	SC14	WBM
BGY71	SC14	WBM
BGY74	SC14	WBM
BGY75	SC14	WBM
BGY78	SC14	WBM
BGY80	SC14	WBM
BGY81	SC14	WBM
BGY82	SC14	WBM
BGY83	SC14	WBM
BGY84	SC14	WBM
BGY84A	SC14	WBM
BGY85	SC14	WBM
BGY85A	SC14	WBM
BGY85H	SC14	WBM
BGY85H/01	SC14	WBM
BGY86	SC14	WBM
BGY87	SC14	WBM
BGY87B	SC14	WBM
BGY88	SC14	WBM
BGY90A	SC09	RFP

TYPE NUMBER	BOOK	SECTION
BGY90B	SC09	RFP
BGY91A	SC09	RFP
BGY91B	SC09	RFP
BGY93A	SC09	RFP
BGY93B	SC09	RFP
BGY93C	SC09	RFP
BGY94A	SC09	RFP
BGY94B	SC09	RFP
BGY94C	SC09	RFP
BGY95A	SC09	RFP
BGY95B	SC09	RFP
BGY96A	SC09	RFP
BGY96B	SC09	RFP
BGY110A	SC09	RFP
BGY110B	SC09	RFP
BGY580	SC14	WBM
BGY581	SC14	WBM
BGY582	SC14	WBM
BGY583	SC14	WBM
BGY584	SC14	WBM
BGY584A	SC14	WBM
BGY585	SC14	WBM
BGY585A	SC14	WBM
BGY586	SC14	WBM
BGY587	SC14	WBM
BGY587B	SC14	WBM
BGY588	SC14	WBM
BLF145	SC08b	RFP/FET
BLF147	SC08b	RFP/FET
BLF175	SC08b	RFP/FET
BLF177	SC08b	RFP/FET
BLF221	SC08b	RFP/FET
BLF225	SC08b	RFP/FET
BLF241	SC08b	RFP/FET
BLF242	SC08b	RFP/FET
BLF244	SC08b	RFP/FET
BLF245	SC08b	RFP/FET
BLF245B	SC08b	RFP/FET
BLF246	SC08b	RFP/FET
BLF246B	SC08b	RFP/FET

TYPE NUMBER	BOOK	SECTION
BLF277	SC08b	RFP/FET
BLF278	SC08b	RFP/FET
BLF346	SC08b	RFP/FET
BLF348	SC08b	RFP/FET
BLF368	SC08b	RFP/FET
BLF378	SC08b	RFP/FET
BLF521	SC08b	RFP/FET
BLF522	SC08b	RFP/FET
BLF543	SC08b	RFP/FET
BLF544	SC08b	RFP/FET
BLF544B	SC08b	RFP/FET
BLF545	SC08b	RFP/FET
BLF546	SC08b	RFP/FET
BLF548	SC08b	RFP/FET
BLT50	SC08a	RFP
BLT80	SC08a	RFP
BLT90/SL	SC08a	RFP
BLT91/SL	SC08a	RFP
BLT92/SL	SC08a	RFP
BLT93/SL	SC08a	RFP
BLU11/SL	SC08a	RFP
BLU15/12	SC08a	RFP
BLU20/12	SC08a	RFP
BLU30/12	SC08a	RFP
BLU30/28	SC08a	RFP
BLU45/12	SC08a	RFP
BLU50	SC08a	RFP
BLU51	SC08a	RFP
BLU52	SC08a	RFP
BLU53	SC08a	RFP
BLU56	SC08a	RFP
BLU60/12	SC08a	RFP
BLU60/28	SC08a	RFP
BLU86	SC08a	RFP
BLU97	SC08a	RFP
BLU98	SC08a	RFP
BLU99	SC08a	RFP
BLV10	SC08a	RFP
BLV11	SC08a	RFP
BLV12	SC08a	RFP

TYPE NUMBER	BOOK	SECTION
BLV20	SC08a	RFP
BLV21	SC08a	RFP
BLV25	SC08a	RFP
BLV30	SC08a	RFP
BLV31	SC08a	RFP
BLV32F	SC08a	RFP
BLV33	SC08a	RFP
BLV33F	SC08a	RFP
BLV36	SC08a	RFP
BLV37	SC08a	RFP
BLV38	SC08a	RFP
BLV45/12	SC08a	RFP
BLV57	SC08a	RFP
BLV59	SC08a	RFP
BLV75/12	SC08a	RFP
BLV80/28	SC08a	RFP
BLV90	SC08a	RFP
BLV90/SL	SC08a	RFP
BLV91	SC08a	RFP
BLV91/SL	SC08a	RFP
BLV92	SC08a	RFP
BLV93	SC08a	RFP
BLV94	SC08a	RFP
BLV95	SC08a	RFP
BLV97	SC08a	RFP
BLV97CE	SC08a	RFP
BLV98	SC08a	RFP
BLV98CE	SC08a	RFP
BLV99	SC08a	RFP
BLV100	SC08a	RFP
BLV101A	SC08a	RFP
BLV101B	SC08a	RFP
BLW29	SC08a	RFP
BLW30	SC08a	RFP
BLW31	SC08a	RFP
BLW32	SC08a	RFP
BLW33	SC08a	RFP
BLW34	SC08a	RFP
BLW50F	SC08a	RFP
BLW60	SC08a	RFP

TYPE NUMBER	BOOK	SECTION
BLW60C	SC08a	RFP
BLW76	SC08a	RFP
BLW77	SC08a	RFP
BLW78	SC08a	RFP
BLW79	SC08a	RFP
BLW80	SC08a	RFP
BLW81	SC08a	RFP
BLW83	SC08a	RFP
BLW84	SC08a	RFP
BLW85	SC08a	RFP
BLW86	SC08a	RFP
BLW87	SC08a	RFP
BLW89	SC08a	RFP
BLW90	SC08a	RFP
BLW91	SC08a	RFP
BLW95	SC08a	RFP
BLW96	SC08a	RFP
BLW97	SC08a	RFP
BLW98	SC08a	RFP
BLW99	SC08a	RFP
BLX13	SC08a	RFP
BLX13C	SC08a	RFP
BLX14	SC08a	RFP
BLX15	SC08a	RFP
BLX39	SC08a	RFP
BLX65	SC08a	RFP
BLX65E	SC08a	RFP
BLX65ES	SC08a	RFP
BLX67	SC08a	RFP
BLX68	SC08a	RFP
BLX69A	SC08a	RFP
BLX91A	SC08a	RFP
BLX91CB	SC08a	RFP
BLX92A	SC08a	RFP
BLX93A	SC08a	RFP
BLX94A	SC08a	RFP
BLX94C	SC08a	RFP
BLX95	SC08a	RFP
BLX96	SC08a	RFP
BLX97	SC08a	RFP

TYPE NUMBER	BOOK	SECTION
BLX98	SC08a	RFP
BLY87A	SC08a	RFP
BLY87C	SC08a	RFP
BLY87C/01	SC08a	RFP
BLY88A	SC08a	RFP
BLY88C	SC08a	RFP
BLY88C/01	SC08a	RFP
BLY89A	SC08a	RFP
BLY89C	SC08a	RFP
BLY90	SC08a	RFP
BLY91A	SC08a	RFP
BLY91C	SC08a	RFP
BLY92A	SC08a	RFP
BLY92C	SC08a	RFP
BLY93A	SC08a	RFP
BLY93C	SC08a	RFP
BLY94	SC08a	RFP
BR100/03	SC03	Th
BR101	SC04	Sm
BR210*	SC02	R
BR211*	SC02	R
BR213*	SC02	R
BR216*	SC02	R
BR220*	SC02	R
BRY39	SC04	Sm
BRY56	SC04	Sm
BRY61	SC10	Mm
BRY62	SC10	Mm
BS107	SC07	FET
BS107A	SC07	FET
BS170	SC07	FET
BS208	SC07	FET
BS250	SC07	FET
BSD12	SC07	FET
BSD22	SC07/10	FET/M
BSD212	SC07	FET
BSD213	SC07	FET
BSD214	SC07	FET
BSD215	SC07	FET
BSN204	SC07	FET

TYPE NUMBER	BOOK	SECTION
BSN204A	SC07	FET
BSN205	SC07	FET
BSN205A	SC07	FET
BSN254	SC07	FET
BSN254A	SC07	FET
BSN274	SC07	FET
BSN274A	SC07	FET
BSP15	SC10	Mm
BSP16	SC10	Mm
BSP19	SC10	Mm
BSP20	SC10	Mm
BSP30	SC10	Mm
BSP31	SC10	Mm
BSP32	SC10	Mm
BSP33	SC10	Mm
BSP40	SC10	Mm
BSP41	SC10	Mm
BSP42	SC10	Mm
BSP43	SC10	Mm
BSP50	SC10	Mm
BSP51	SC10	Mm
BSP52	SC10	Mm
BSP60	SC10	Mm
BSP61	SC10	Mm
BSP62	SC10	Mm
BSP103	SC07/10	FET/Mm
BSP105	SC07/10	FET/Mm
BSP106	SC07/10	FET/Mm
BSP107	SC07/10	FET/Mm
BSP108	SC07/10	FET/Mm
BSP109	SC07/10	FET/Mm
BSP110	SC07/10	FET/Mm
BSP120	SC07/10	FET/Mm
BSP121	SC07/10	FET/Mm
BSP126	SC07/10	FET/Mm
BSP204	SC07	FET
BSP204A	SC07	FET
BSP205	SC07/10	FET/Mm
BSP206	SC07/10	FET/Mm
BSP220	SC07	FET

TYPE NUMBER	BOOK	SECTION
BSP225	SC07/10	FET/Mm
BSP254	SC07	FET
BSP254A	SC07	FET
BSR12	SC10	Mm
BSR12R	SC10	Mm
BSR13	SC10	Mm
BSR13R	SC10	Mm
BSR14	SC10	Mm
BSR14R	SC10	Mm
BSR15	SC10	Mm
BSR15R	SC10	Mm
BSR16	SC10	Mm
BSR16R	SC10	Mm
BSR17	SC10	Mm
BSR17R	SC10	Mm
BSR17A	SC10	Mm
BSR17AR	SC10	Mm
BSR18	SC10	Mm
BSR18R	SC10	Mm
BSR18A	SC10	Mm
BSR18AR	SC10	Mm
BSR19	SC10	Mm
BSR19A	SC10	Mm
BSR20	SC10	Mm
BSR20A	SC10	Mm
BSR30	SC10	Mm
BSR31	SC10	Mm
BSR32	SC10	Mm
BSR33	SC10	Mm
BSR40	SC10	Mm
BSR41	SC10	Mm
BSR42	SC10	Mm
BSR43	SC10	Mm
BSR50	SC04	Sm
BSR51	SC04	Sm
BSR52	SC04	Sm
BSR56	SC07/10	FET/Mm
BSR57	SC07/10	FET/Mm
BSR58	SC07/10	FET/Mm
BSR60	SC04	Sm

TYPE NUMBER	BOOK	SECTION
BSR61	SC04	Sm
BSR62	SC04	Sm
BSS38	SC04	Sm
BSS50	SC04	Sm
BSS51	SC04	Sm
BSS52	SC04	Sm
BSS60	SC04	Sm
BSS61	SC04	Sm
BSS62	SC04	Sm
BSS63	SC10	Mm
BSS63R	SC10	Mm
BSS64	SC10	Mm
BSS64R	SC10	Mm
BSS68	SC04	Sm
BSS83	SC07/10	FET/Mm
BSS84	SC07/10	FET/Mm
BSS87	SC07/10	FET/Mm
BSS89	SC07	FET
BSS91	SC07	FET
BSS92	SC07	FET
BSS100	SC07	FET
BSS123	SC07	FET
BSS131	SC07	FET
BSS138	SC07	FET
BSS192	SC07/10	FET/Mm
BST15	SC10	Mm
BST16	SC10	Mm
BST39	SC10	Mm
BST40	SC10	Mm
BST50	SC10	Mm
BST51	SC10	Mm
BST52	SC10	Mm
BST60	SC10	Mm
BST61	SC10	Mm
BST62	SC10	Mm
BST70A	SC07	FET
BST72A	SC07	FET
BST74A	SC07	FET
BST76A	SC07	FET
BST78	SC07	FET

TYPE NUMBER	BOOK	SECTION
BST80	SC07/10	FET/Mm
BST82	SC07/10	FET/Mm
BST84	SC07/10	FET/Mm
BST86	SC07/10	FET/Mm
BST95	SC07	FET
BST97	SC07	FET
BST100	SC07	FET
BST110	SC07	FET
BST120	SC07/10	FET/Mm
BST122	SC07/10	FET/Mm
BSV15	SC04	Sm
BSV16	SC04	Sm
BSV17	SC04	Sm
BSV52	SC10	Mm
BSV52R	SC10	Mm
BSV64	SC04	Sm
BSV78	SC07	FET
BSV79	SC07	FET
BSV80	SC07	FET
BSV81	SC07	FET
BSW66A	SC04	Sm
BSW67A	SC04	Sm
BSW68A	SC04	Sm
BSX19	SC04	Sm
BSX20	SC04	Sm
BSX32	SC04	Sm
BSX45	SC04	Sm
BSX46	SC04	Sm
BSX47	SC04	Sm
BSX59	SC04	Sm
BSX60	SC04	Sm
BSX61	SC04	Sm
BSX62	SC04	Sm
BSX63	SC04	Sm
BSY95A	SC04	Sm
BT134*	SC03	Tri
BT134W*	SC03	Tri
BT136*	SC03	Tri
BT136F*	SC03	Tri
BT137*	SC03	Tri

TYPE NUMBER	BOOK	SECTION
BT137F*	SC03	Tri
BT138*	SC03	Tri
BT138F*	SC03	Tri
BT139*	SC03	Tri
BT139F*	SC03	Tri
BT145*	SC03	Tri
BT148*	SC03	Th
BT149*	SC03	Th
BT150	SC03	Th
BT151*	SC03	Th
BT151F*	SC03	Th
BT152*	SC03	Th
BT153	SC03	Th
BT169*	SC03	Th
BT169W*	SC03	Th
BTA140*	SC03	Tri
BTR59*	SC03	Tri
BTS59*	SC03	Tri
BTV58*	SC03	Th
BTW38*	SC03	Th
BTW40*	SC03	Th
BTW42*	SC03	Th
BTW43*	SC03	Tri
BTW45*	SC03	Th
BTW58*	SC03	Th
BTY79*	SC03	Th
BTY91*	SC03	Th
BU306	SC06	SP
BU306F	SC06	SP
BU505	SC06	SP
BU506	SC06	SP
BU506D	SC06	SP
BU508A	SC06	SP
BU508D	SC06	SP
BU705	SC06	SP
BU706	SC06	SP
BU706D	SC06	SP
BU806	SC06	SP
BU807	SC06	SP
BU808	SC06	SP

TYPE NUMBER	BOOK	SECTION
BU824	SC06	SP
BU826	SC06	SP
BUP22*	SC06	SP
BUP23*	SC06	SP
BUS11	SC06	SP
BUS11A	SC06	SP
BUS12	SC06	SP
BUS12A	SC06	SP
BUS13	SC06	SP
BUS13A	SC06	SP
BUS14	SC06	SP
BUS14A	SC06	SP
BUS21*	SC06	SP
BUS22*	SC06	SP
BUS23*	SC06	SP
BUS24*	SC06	SP
BUS131*	SC06	SP
BUS132*	SC06	SP
BUS133*	SC06	SP
BUT11	SC06	SP
BUT11A	SC06	SP
BUT11F	SC06	SP
BUT11AF	SC06	SP
BUT12	SC06	SP
BUT12A	SC06	SP
BUT12F	SC06	SP
BUT12AF	SC06	SP
BUT18	SC06	SP
BUT18A	SC06	SP
BUT18F	SC06	SP
BUT18AF	SC06	SP
BUT21B	SC06	SP
BUT21C	SC06	SP
BUT21BF	SC06	SP
BUT21CF	SC06	SP
BUT22B	SC06	SP
BUT22C	SC06	SP
BUT22BF	SC06	SP
BUT22CF	SC06	SP
BUT131	SC06	SP

TYPE NUMBER	BOOK	SECTION
BUV26	SC06	SP
BUV26A	SC06	SP
BUV26F	SC06	SP
BUV26AF	SC06	SP
BUV27	SC06	SP
BUV27A	SC06	SP
BUV27F	SC06	SP
BUV27AF	SC06	SP
BUV28	SC06	SP
BUV28A	SC06	SP
BUV28F	SC06	SP
BUV28AF	SC06	SP
BUV47	SC06	SP
BUV47A	SC06	SP
BUV48	SC06	SP
BUV48A	SC06	SP
BUV82	SC06	SP
BUV83	SC06	SP
BUV89	SC06	SP
BUV90	SC06	SP
BUV90F	SC06	SP
BUV98(V)	SC06	SP
BUV98A	SC06	SP
BUV298(V)	SC06	SP
BUV298A	SC06	SP
BUW11	SC06	SP
BUW11A	SC06	SP
BUW12	SC06	SP
BUW12A	SC06	SP
BUW12F	SC06	SP
BUW12AF	SC06	SP
BUW13	SC06	SP
BUW13A	SC06	SP
BUW13F	SC06	SP
BUW13AF	SC06	SP
BUW84	SC06	SP
BUW85	SC06	SP
BUW86	SC06	SP
BUW87	SC06	SP
BUW87A	SC06	SP

TYPE NUMBER	BOOK	SECTION
BUW131*	SC06	SP
BUW132*	SC06	SP
BUW133*	SC06	SP
BUX46	SC06	SP
BUX46A	SC06	SP
BUX47	SC06	SP
BUX47A	SC06	SP
BUX48	SC06	SP
BUX48A	SC06	SP
BUX84	SC06	SP
BUX84F	SC06	SP
BUX85	SC06	SP
BUX85F	SC06	SP
BUX86	SC06	SP
BUX87	SC06	SP
BUX88	SC06	SP
BUX98	SC06	SP
BUX98A	SC06	SP
BUX99	SC06	SP
BUY89	SC06	SP
BUK416-100AE/BE	SC13	PM
BUK416-200AE/BE	SC13	PM
BUK416-1000AE/BE	SC13	PM
BUK417-500AE/BE	SC13	PM
BUK426-60A/B	SC13	PM
BUK426-100A/B	SC13	PM
BUK426-200A/B	SC13	PM
BUK426-800A/B	SC13	PM
BUK426-1000A/B	SC13	PM
BUK427-400A/B	SC13	PM
BUK427-500A/B	SC13	PM
BUK427-600A/B	SC13	PM
BUK428-500A/B	SC13	PM
BUK428-800A/B	SC13	PM
BUK428-1000A/B	SC13	PM
BUK436-60A/B	SC13	PM
BUK436-100A/B	SC13	PM
BUK436-200A/B	SC13	PM
BUK436-800A/B	SC13	PM
BUK436-1000A/B	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUK437-400A/B	SC13	PM
BUK437-500A/B	SC13	PM
BUK437-600A/B	SC13	PM
BUK438-500A/B	SC13	PM
BUK438-800A/B	SC13	PM
BUK438-1000A/B	SC13	PM
BUK439-60A	SC13	PM
BUK441-60A/B	SC13	PM
BUK441-100A/B	SC13	PM
BUK442-60A/B	SC13	PM
BUK442-100A/B	SC13	PM
BUK443-60A/B	SC13	PM
BUK443-100A/B	SC13	PM
BUK444-200A/B	SC13	PM
BUK444-400A/B	SC13	PM
BUK444-500A/B	SC13	PM
BUK444-600A/B	SC13	PM
BUK444-800A/B	SC13	PM
BUK445-60A/B	SC13	PM
BUK445-100A/B	SC13	PM
BUK445-200A/B	SC13	PM
BUK445-400A/B	SC13	PM
BUK445-500A/B	SC13	PM
BUK445-600A/B	SC13	PM
BUK446-800A/B	SC13	PM
BUK446-1000A/B	SC13	PM
BUK451-60A/B	SC13	PM
BUK451-100A/B	SC13	PM
BUK452-60A/B	SC13	PM
BUK452-100A/B	SC13	PM
BUK453-60A	SC13	PM
BUK453-60B	SC13	PM
BUK453-100A	SC13	PM
BUK453-100B	SC13	PM
BUK453-500A	SC13	PM
BUK453-500B	SC13	PM
BUK454-200A	SC13	PM
BUK454-200B	SC13	PM
BUK454-400A	SC13	PM
BUK454-400B	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUK454-500A	SC13	PM
BUK454-500B	SC13	PM
BUK454-600A	SC13	PM
BUK454-600B	SC13	PM
BUK454-800A	SC13	PM
BUK454-800B	SC13	PM
BUK455-60A	SC13	PM
BUK455-60B	SC13	PM
BUK455-100A	SC13	PM
BUK455-100B	SC13	PM
BUK455-200A	SC13	PM
BUK455-200B	SC13	PM
BUK455-400A	SC13	PM
BUK455-400B	SC13	PM
BUK455-500A	SC13	PM
BUK455-500B	SC13	PM
BUK455-600A	SC13	PM
BUK455-600B	SC13	PM
BUK456-60A	SC13	PM
BUK456-60B	SC13	PM
BUK456-100A	SC13	PM
BUK456-100B	SC13	PM
BUK456-200A	SC13	PM
BUK456-200B	SC13	PM
BUK456-800A	SC13	PM
BUK456-800B	SC13	PM
BUK456-1000A	SC13	PM
BUK456-1000B	SC13	PM
BUK457-400A	SC13	PM
BUK457-400B	SC13	PM
BUK457-500A	SC13	PM
BUK457-500B	SC13	PM
BUK457-600B	SC13	PM
BUK471-60A*	SC13	PM
BUK471-60B*	SC13	PM
BUK471-100A*	SC13	PM
BUK471-100B*	SC13	PM
BUK472-60A*	SC13	PM
BUK472-60B*	SC13	PM
BUK472-100A*	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUK472-100B*	SC13	PM
BUK473-60A*	SC13	PM
BUK473-60B*	SC13	PM
BUK473-100A*	SC13	PM
BUK473-100B*	SC13	PM
BUK474-200A*	SC13	PM
BUK474-200B*	SC13	PM
BUK474-400A*	SC13	PM
BUK474-400B*	SC13	PM
BUK474-500A*	SC13	PM
BUK474-500B*	SC13	PM
BUK474-600A*	SC13	PM
BUK474-600B*	SC13	PM
BUK474-800A*	SC13	PM
BUK474-800B*	SC13	PM
BUK475-60A*	SC13	PM
BUK475-60B*	SC13	PM
BUK475-100A*	SC13	PM
BUK475-100B*	SC13	PM
BUK475-200A*	SC13	PM
BUK475-200B*	SC13	PM
BUK475-400A*	SC13	PM
BUK475-400B*	SC13	PM
BUK475-500A*	SC13	PM
BUK475-500B*	SC13	PM
BUK475-600A*	SC13	PM
BUK475-600B*	SC13	PM
BUK476-800A*	SC13	PM
BUK476-800B*	SC13	PM
BUK476-1000A*	SC13	PM
BUK476-1000B*	SC13	PM
BUK539-60A*	SC13	PM
BUK541-60A*	SC13	PM
BUK541-60B*	SC13	PM
BUK541-100A	SC13	PM
BUK541-100B	SC13	PM
BUK542-60A	SC13	PM
BUK542-60B	SC13	PM
BUK542-100A	SC13	PM
BUK542-100B	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUK543-60A	SC13	PM
BUK543-60B	SC13	PM
BUK543-100A	SC13	PM
BUK543-100B	SC13	PM
BUK545-60A	SC13	PM
BUK545-60B	SC13	PM
BUK545-100A	SC13	PM
BUK545-100B	SC13	PM
BUK545-200A	SC13	PM
BUK545-200B	SC13	PM
BUK551-60A*	SC13	PM
BUK551-60B*	SC13	PM
BUK551-100A	SC13	PM
BUK551-100B	SC13	PM
BUK552-60A	SC13	PM
BUK552-60B	SC13	PM
BUK552-100A	SC13	PM
BUK552-100B	SC13	PM
BUK553-60A	SC13	PM
BUK553-60B	SC13	PM
BUK553-100A	SC13	PM
BUK553-100B	SC13	PM
BUK554-200A	SC13	PM
BUK554-200B	SC13	PM
BUK555-60A	SC13	PM
BUK555-60B	SC13	PM
BUK555-100A	SC13	PM
BUK555-100B	SC13	PM
BUK555-200A	SC13	PM
BUK555-200B	SC13	PM
BUK556-60A*	SC13	PM
BUK571-60A*	SC13	PM
BUK571-60A*	SC13	PM
BUK571-60B*	SC13	PM
BUK571-100A*	SC13	PM
BUK571-100B*	SC13	PM
BUK572-60A*	SC13	PM
BUK572-60B*	SC13	PM
BUK572-100A*	SC13	PM
BUK572-100B*	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUK573-60A*	SC13	PM
BUK573-60B*	SC13	PM
BUK573-100A*	SC13	PM
BUK573-100B*	SC13	PM
BUK575-60A*	SC13	PM
BUK575-60B*	SC13	PM
BUK575-100A*	SC13	PM
BUK575-100B*	SC13	PM
BUK575-200A*	SC13	PM
BUK575-200B*	SC13	PM
BUK617-500AE	SC13	PM
BUK617-500BE	SC13	PM
BUK627-500A	SC13	PM
BUK627-500B	SC13	PM
BUK637-400A	SC13	PM
BUK637-400B	SC13	PM
BUK637-500A	SC13	PM
BUK637-500B	SC13	PM
BUK638-500A	SC13	PM
BUK638-500B	SC13	PM
BUK638-800A*	SC13	PM
BUK638-800B*	SC13	PM
BUK638-1000A*	SC13	PM
BUK638-1000B*	SC13	PM
BUK655-500A	SC13	PM
BUK655-500B	SC13	PM
BUK657-400A	SC13	PM
BUK657-400B	SC13	PM
BUK657-500A	SC13	PM
BUK657-500B	SC13	PM
BUK793-60A*	SC13	PM
BUK795-60A*	SC13	PM
BUK993-60A*	SC13	PM
BUK995-60A*	SC13	PM
BUZ308	SC13	PM
BUZ310	SC13	PM
BUZ311	SC13	PM
BUZ326	SC13	PM
BUZ330	SC13	PM
BUZ331	SC13	PM

TYPE NUMBER	BOOK	SECTION
BUZ347	SC13	PM
BUZ348	SC13	PM
BUZ349	SC13	PM
BUZ350	SC13	PM
BUZ351	SC13	PM
BUZ355	SC13	PM
BUZ356	SC13	PM
BUZ357	SC13	PM
BUZ358	SC13	PM
BUZ384	SC13	PM
BUZ385	SC13	PM
BY228	SC01	R
BY229*	SC02	R
BY229F*	SC02	R
BY249*	SC02	R
BY249F*	SC02	R
BY260*	SC02	R
BY328	SC01	SD
BY329*	SC02	R
BY359*	SC02	R
BY359F	SC02	R
BY438	SC01	R
BY448	SC01	R
BY458	SC01	R
BY505	SC01	R
BY509	SC01	R
BY527	SC01	R
BY584	SC01	R
BY588	SC01	R
BY609	SC01	R
BY610	SC01	R
BY614	SC01	R
BY619	SC01	R
BY620	SC01	R
BY627	SC01	R
BY705	SC01	R
BY706	SC01	R
BY707	SC01	R
BY708	SC01	R
BY709	SC01	R

TYPE NUMBER	BOOK	SECTION
BY710	SC01	R
BY711	SC01	R
BY712	SC01	R
BY713	SC01	R
BY714	SC01	R
BY715	SC01	R
BY716	SC01	R
BY717	SC01	R
BY718	SC01	R
BY719	SC01	R
BY720	SC01	R
BY721	SC01	R
BY722	SC01	R
BY723	SC01	R
BY724	SC01	R
BYD11*	SC01	R
BYD13*	SC01	R
BYD14*	SC01	R
BYD17*	SC01/10	R/Mm
BYD31*	SC01	R
BYD33*	SC01	R
BYD34*	SC01	R
BYD37*	SC01/10	R/Mm
BYD73*	SC01	R
BYD74*	SC01	R
BYD77*	SC01	R
BYM26*	SC01	R
BYM36*	SC01	R
BYM56*	SC01	R
BYP20*	SC02	R
BYP21*	SC02	R
BYP22*	SC02	R
BYQ27*	SC01	R
BYQ28*	SC02	R
BYQ28F*	SC02	R
BYR28*	SC02	R
BYR29*	SC02	R
BYR29F*	SC02	R
BYR30*	SC02	R
BYR34*	SC02	R

TYPE NUMBER	BOOK	SECTION
BYR79*	SC02	R
BYT28*	SC02	R
BYT79*	SC02	R
BYT23OPIV	SC02	R
BYV10*	SC01	R
BYV24*	SC02	R
BYV26*	SC01	R
BYV27*	SC01	R
BYV28*	SC01	R
BYV29*	SC02	R
BYV29F*	SC02	R
BYV30*	SC02	R
BYV31*	SC02	R
BYV32*	SC02	R
BYV32F*	SC02	R
BYV34*	SC02	R
BYV36*	SC01	R
BYV42*	SC02	R
BYV44*	SC02	R
BYV54V	SC02	R
BYV72*	SC02	R
BYV72F*	SC02	R
BYV74*	SC02	R
BYV74F*	SC02	R
BYV79*	SC02	R
BYV92*	SC02	R
BYV95A	SC01	R
BYV95B	SC01	R
BYV95C	SC01	R
BYV96D	SC01	R
BYV96E	SC01	R
BYV118*	SC02	R
BYV118F*	SC02	R
BYV120*	SC02	R
BYV121*	SC02	R
BYV133*	SC02	R
BYV133F*	SC02	R
BYV143*	SC02	R
BYV143F*	SC02	R
BYW25*	SC02	R

TYPE NUMBER	BOOK	SECTION
BYW29*	SC02	R
BYW29F*	SC02	R
BYW30*	SC02	R
BYW31*	SC02	R
BYW54	SC01	R
BYW55	SC01	R
BYW56	SC01	R
BYW92*	SC02	R
BYW93*	SC02	R
BYW95A	SC01	R
BYW95B	SC01	R
BYW95C	SC01	R
BYW96D	SC01	R
BYW96E	SC01	R
BYX10G	SC01	R
BYX25*	SC02	R
BYX30*	SC02	R
BYX38*	SC02	R
BYX39*	SC02	R
BYX42*	SC02	R
BYX46*	SC02	R
BYX52*	SC02	R
BYX56*	SC02	R
BYX90G	SC01	R
BYX96*	SC02	R
BYX97*	SC02	R
BYX98*	SC02	R
BYX99*	SC02	R
BZD23	SC01	Vrg
BZD27	SC01/10	Vrg/Mm
BZT03	SC01	Vrg
BZV10	SC01	Vrf
BZV11	SC01	Vrf
BZV12	SC01	Vrf
BZV13	SC01	Vrf
BZV14	SC01	Vrf
BZV37	SC01	Vrf
BZV49*	SC01/10	Vrg/Mm
BZV55*	SC10	Mm
BZV60	SC01	Vrg

TYPE NUMBER	BOOK	SECTION
BZV80	SC01/10	Vrf/Mm
BZV81	SC01/10	Vrf/Mm
BZV84	SC01/10	Vrf/Mm
BZV85*	SC01	Vrg
BZV86	SC01	SD
BZV87	SC01/10	Vrg/Mm
BZW03*	SC01	Vrg
BZW14	SC01	Vrg
BZW86*	SC02	TS
BZX55*	SC01	Vrg
BZX70*	SC02	Vrg
BZX75*	SC01	Vrg
BZX79*	SC01	Vrg
BZX84*	SC01/10	Vrg/Mm
BZY91*	SC02	Vrg
BZY93*	SC02	Vrg
CNG35	SC12	PhC
CNG36	SC12	PhC
CNG40	SC12	PhC
CNG82	SC12	PhC
CNG83	SC12	PhC
CNR36	SC12	PhC
CNS35	SC12	PhC
CNW82	SC12	PhC
CNW83	SC12	PhC
CNX21	SC12	PhC
CNX35	SC12	PhC
CNX35U	SC12	PhC
CNX36	SC12	PhC
CNX36U	SC12	PhC
CNX38	SC12	PhC
CNX38U	SC12	PhC
CNX39	SC12	PhC
CNX39U	SC12	PhC
CNX48	SC12	PhC
CNX48U	SC12	PhC
CNX62	SC12	PhC
CNX62A	SC12	PhC
CNX71	SC12	PhC
CNX72A	SC12	PhC

TYPE NUMBER	BOOK	SECTION
CNX82A	SC12	PhC
CNX83A	SC12	PhC
CNY17-1	SC12	PhC
CNY17-2	SC12	PhC
CNY17-3	SC12	PhC
CNY17-4	SC12	PhC
CQW58A	S8a	I
CQW89A	S8a	I
CQW89B	S8a	I
CQY58A	S8a	I
CQY89A	S8a	I
CQY89F	S8a	I
ESM3045A(V)	SC06	SP
ESM3045D(V)	SC06	SP
ESM4045A(V)	SC06	SP
ESM4045D(V)	SC06	SP
ESM5045D(V)	SC06	SP
ESM6045A(V)	SC06	SP
ESM6045D(V)	SC06	SP
Fresnel-lens	SC12	A
H11A1	SC12	PhC
H11A2	SC12	PhC
H11A3	SC12	PhC
H11A4	SC12	PhC
H11A5	SC12	PhC
H11B1	SC12	PhC
H11B2	SC12	PhC
H11B3	SC12	PhC
H11B255	SC12	PhC
J108	SC07	FET
J109	SC07	FET
J110	SC07	FET
J111	SC07	FET
J112	SC07	FET
J113	SC07	FET
J174	SC07	FET
J175	SC07	FET
J176	SC07	FET
J177	SC07	FET
JA100	SC04	Sm

TYPE NUMBER	BOOK	SECTION
JA101	SC04	Sm
JC327	SC04	Sm
JC327A	SC04	Sm
JC328	SC04	Sm
JC337	SC04	Sm
JC337A	SC04	Sm
JC338	SC04	Sm
JC500	SC04	Sm
JC501	SC04	Sm
JC546	SC04	Sm
JC547	SC04	Sm
JC550	SC04	Sm
JC556	SC04	Sm
JC557	SC04	Sm
JC558	SC04	Sm
JC559	SC04	Sm
JC560	SC04	Sm
JF494	SC04	Sm
KGZ10	SC17	SEN
KGZ20	SC17	SEN
KGZ21	SC17	SEN
KMZ10A	SC17	SEN
KMZ10A1	SC17	SEN
KMZ10B	SC17	SEN
KMZ10C	SC17	SEN
KP100A	SC17	SEN
KP100A1	SC17	SEN
KP101A	SC17	SEN
KP130AE	SC17	SEN
KP131AE	SC17	SEN
KPZ20G	SC17	SEN
KPZ21G	SC17	SEN
KPZ21GE	SC17	SEN
KRX10	SC17	SEN
KRX11	SC17	SEN
KTY81-100*	SC17	SEN
KTY81-200*	SC17	SEN
KTY83-100*	SC17	SEN
KTY84-100*	SC17	SEN
KTY85-100*	SC10/17	SEN

TYPE NUMBER	BOOK	SECTION
KTY86-205	SC17	SEN
KTY87-205	SC17	SEN
LAE4001R	SC15	M
LAE4002S	SC15	M
LAE6000Q	SC15	M
LBE2003S	SC15	M
LBE2009S	SC15	M
LCE2003S	SC15	M
LCE2009S	SC15	M
LJE42002T	SC15	M
LKE21004R	SC15	M
LKE21015T	SC15	M
LKE21050T	SC15	M
LTE21009R	SC15	M
LTE21015R	SC15	M
LTE21025R	SC15	M
LTE4002S	SC15	M
LTE42005S	SC15	M
LTE42008R	SC15	M
LTE42012R	SC15	M
LUE2003S	SC15	M
LUE2009S	SC15	M
LV172E50R	SC15	M
LV2024E45R	SC15	M
LV2327E40R	SC15	M
LV2931E50S	SC15	M
LVE21050R	SC15	M
LWE2015R	SC15	M
LWE2025R	SC15	M
LZ1418E100R	SC15	M
LZE18100R	SC15	M
MCA230	SC12	PhC
MCA231	SC12	PhC
MCA255	SC12	PhC
MCT2	SC12	PhC
MCT26	SC12	PhC
MJE13004	SC06	SP
MJE13005	SC06	SP
MJE13006	SC06	SP
MJE13007	SC06	SP

TYPE NUMBER	BOOK	SECTION
MJE13008	SC06	SP
MJE13009	SC06	SP
MPS3702	SC04	Sm
MPS3703	SC04	Sm
MPS3704	SC04	Sm
MPS3705	SC04	Sm
MPS3706	SC04	Sm
MPS3904	SC04	Sm
MPS3906	SC04	Sm
MPS6513	SC04	Sm
MPS6514	SC04	Sm
MPS6515	SC04	Sm
MPS6517	SC04	Sm
MPS6518	SC04	Sm
MPS6519	SC04	Sm
MPS6520	SC04	Sm
MPS6521	SC04	Sm
MPS6522	SC04	Sm
MPS6523	SC04	Sm
MPS6531	SC04	Sm
MPS6532	SC04	Sm
MPS6534	SC04	Sm
MPS6535	SC04	Sm
MPSA05	SC04	Sm
MPSA06	SC04	Sm
MPSA13	SC04	Sm
MPSA14	SC04	Sm
MPSA25	SC04	Sm
MPSA26	SC04	Sm
MPSA27	SC04	Sm
MPSA42	SC04	Sm
MPSA43	SC04	Sm
MPSA55	SC04	Sm
MPSA56	SC04	Sm
MPSA63	SC04	Sm
MPSA64	SC04	Sm
MPSA75	SC04	Sm
MPSA76	SC04	Sm
MPSA77	SC04	Sm
MPSA92	SC04	Sm

TYPE NUMBER	BOOK	SECTION
MPSA93	SC04	Sm
MRB11175Y	SC15	M
MRB11350Y	SC15	M
MSB11900Y	SC15	M
MX0912B250Y	SC15	M
MX0912B350Y	SC15	M
MZ0912B50Y	SC15	M
MZ0912B100Y	SC15	M
OM200/S2	SC17	SEN
OM286	SC17	SEN
OM286M	SC17	SEN
OM287	SC17	SEN
OM287M	SC17	SEN
OM320	SC14	WBM
OM321	SC14	WBM
OM322	SC14	WBM
OM323	SC14	WBM
OM323A	SC14	WBM
OM335	SC14	WBM
OM336	SC14	WBM
OM337	SC14	WBM
OM337A	SC14	WBM
OM339	SC14	WBM
OM345	SC14	WBM
OM350	SC14	WBM
OM360	SC14	WBM
OM361	SC14	WBM
OM370	SC14	WBM
OM386B	SC17	SEN
OM386M	SC17	SEN
OM387B	SC17	SEN
OM387M	SC17	SEN
OM388B	SC17	SEN
OM389B	SC17	SEN
OM390	SC17	SEN
OM391	SC17	SEN
OM931	SC05	P
OM961	SC05	P
OM2860	SC17	SEN
OM2870	SC17	SEN

TYPE NUMBER	BOOK	SECTION
OSB/M/S9115*	SC02	St
OSB/M/S9215*	SC02	St
OSB/M/S9415*	SC02	St
OSM9510-12	SC02	St
PBYR635/40/45CT	SC02	R
PBYR735/40/45	SC02	R
PBYR735/40/45F	SC02	R
PBYR1035/40/45	SC02	R
PBYR1035/40/45F	SC02	R
PBYR1535/40/45CT	SC02	R
PBYR1535/40/45CTF	SC02	R
PBYR1635/40/45	SC02	R
PBYR1635/40/45F	SC02	R
PBYR2035/40/45CT	SC02	R
PBYR2035/40/45CTF	SC02	R
PBYR2535/40/45CT	SC02	R
PBYR2535/40/45CTF	SC02	R
PBYR3035/40/45PT	SC02	R
PBYR12035/40/45TV	SC02	R
PBYR16035/40/45TV	SC02	R
PBYR30035/40/45CT	SC02	R
PBYR40035/40/45CT	SC02	R
PH2222/A	SC04	Sm
PH2369	SC04	Sm
PH2907	SC04	Sm
PH2907A	SC04	Sm
PH5415	SC04	Sm
PH5416	SC04	Sm
PH6659	SC07	FET
PH6660	SC07	FET
PH6661	SC07	FET
PH13002	SC06	SP
PH13003	SC06	SP
PKB12005U	SC15	M
PKB20010U	SC15	M
PMBD914	SC01/10	SD/Mm
PMBD2835	SC01	SD
PMBD2836	SC01	SD
PMBD2837	SC01	SD
PMBD2838	SC01	SD

TYPE NUMBER	BOOK	SECTION
PMBD6050	SC01/10	SD/Mm
PMBD6100	SC01	SD
PMBD7000	SC01/10	SD/Mm
PMBF107	SC07	FET
PMBF170	SC07/10	FET/Mm
PMBF4391	SC07/10	FET/Mm
PMBF4392	SC07/10	FET/Mm
PMBF4393	SC07/10	FET/Mm
PMBFJ108	SC07/10	FET/Mm
PMBFJ109	SC07/10	FET/Mm
PMBJF110	SC07/10	FET/Mm
PMBFJ111	SC07/10	FET/Mm
PMBFJ112	SC07/10	FET/Mm
PMBJF113	SC07/10	FET/Mm
PMBFJ174	SC07/10	FET/Mm
PMBJF175	SC07/10	FET/Mm
PMBJF176	SC07/10	FET/Mm
PMBJF177	SC07/10	FET/Mm
PMBT2222	SC10	Mm
PMBT2222A	SC10	Mm
PMBT2369	SC10	Mm
PMBT2907	SC10	Mm
PMBT2907A	SC10	Mm
PMBT3904	SC10	Mm
PMBT3906	SC10	Mm
PMBT4401	SC10	Mm
PMBT4403	SC10	Mm
PMBT5088	SC10	Mm
PMBT5401	SC10	Mm
PMBT5550	SC10	Mm
PMBT5551	SC10	Mm
PMBT6428	SC10	Mm
PMBT6429	SC10	Mm
PMBTA05	SC10	Mm
PMBTA06	SC10	Mm
PMBTA13	SC10	Mm
PMBTA14	SC10	Mm
PMBTA42	SC10	Mm
PMBTA43	SC10	Mm
PMBTA55	SC10	Mm

TYPE NUMBER	BOOK	SECTION
PMBTA56	SC10	Mm
PMBTA63	SC10	Mm
PMBTA64	SC10	Mm
PMBTA92	SC10	Mm
PMBTA93	SC10	Mm
PMBZ5226	SC01	SD
PMLL4148	SC01/10	SD/Mm
PMLL4150	SC01/10	SD/Mm
PMLL4151	SC01/10	SD/Mm
PMLL4153	SC01/10	SD/Mm
PMLL4446	SC01/10	SD/Mm
PMLL4448	SC01/10	SD/Mm
PMLL5225B to	SC01/10	SD/Mm
PMLL5267B	SC01/10	SD/Mm
PN2222	SC04	Sm
PN2222A	SC04	Sm
PN2369	SC04	Sm
PN2907	SC04	Sm
PN2907A	SC04	Sm
PN3439	SC04	Sm
PN3440	SC04	Sm
PN4391	SC07	FET
PN4392	SC07	FET
PN4393	SC07	FET
PN5415	SC04	Sm
PN5416	SC04	Sm
PO44	SC12	PhC
PO44A	SC12	PhC
PPC5001T	SC15	M
PQC5001T	SC15	M
PRLL4001	SC01/10	SD/Mm
PRLL4002	SC01/10	SD/Mm
PRLL5817	SC01/10	SD/Mm
PRLL5818	SC01/10	SD/Mm
PRLL5819	SC01/10	SD/Mm
PTB23001X	SC15	M
PTB23003X	SC15	M
PTB23005X	SC15	M
PTB32001X	SC15	M
PTB32003X	SC15	M

TYPE NUMBER	BOOK	SECTION
PTB32005X	SC15	M
PTB42001X	SC15	M
PTB42002X	SC15	M
PTB42003X	SC15	M
PVB42004X	SC15	M
PXB16050U	SC15	M
PXT2222	SC10	Mm
PXT2222A	SC10	Mm
PXT2907	SC10	Mm
PXT2907A	SC10	Mm
PXT3904	SC10	Mm
PXT3906	SC10	Mm
PXT4401	SC10	Mm
PXT4403	SC10	Mm
PXTA14	SC10	Mm
PXTA27	SC10	Mm
PXTA64	SC10	Mm
PXTA77	SC10	Mm
PZ1418B15U	SC15	M
PZ1418B30U	SC15	M
PZ1721B12U	SC15	M
PZ1721B25U	SC15	M
PZ2024B10U	SC15	M
PZ2024B20U	SC15	M
PZ2327B15U	SC15	M
PZB16035U	SC15	M
PZB16040U	SC15	M
PZB27020U	SC15	M
PZFJ108	SC07	FET
PZFJ109	SC07	FET
PZFJ110	SC07	FET
PZT2222	SC10	Mm
PZT2222A	SC10	Mm
PZT2907	SC10	Mm
PZT2907A	SC10	Mm
PZT3904	SC10	Mm
PZT3906	SC10	Mm
PZTA05	SC10	Mm
PZTA06	SC10	Mm
PZTA13	SC10	Mm

TYPE NUMBER	BOOK	SECTION
PZTA14	SC10	Mm
PZTA42	SC10	Mm
PZTA43	SC10	Mm
PZTA55	SC10	Mm
PZTA56	SC10	Mm
PZTA63	SC10	Mm
PZTA64	SC10	Mm
PZTA92	SC10	Mm
PZTA93	SC10	Mm
RPW100	SC17	SEN
RPW101	SC17	SEN
RPW102	SC17	SEN
RPY98A	SC17	SEN
RPY98C	SC17	SEN
RPY98F	SC17	SEN
RPY98G	SC17	SEN
RPY98S	SC17	SEN
RPY99A	SC17	SEN
RPY99C	SC17	SEN
RPY99D	SC17	SEN
RPY99F	SC17	SEN
RPY99G	SC17	SEN
RPY99S	SC17	SEN
RPY99P/P5206	SC17	SEN
RPY100	SC17	SEN
RPY102	SC17	SEN
RPY104A	SC17	SEN
RPY104C	SC17	SEN
RPY104D	SC17	SEN
RPY104F	SC17	SEN
RPY104G	SC17	SEN
RPY104S	SC17	SEN
RPY105P/P5206	SC17	SEN
RPY107	SC17	SEN
RPY108P/P5211	SC17	SEN
RPY109	SC17	SEN
RPY109B/P2105	SC17	SEN
RPY222	SC17	SEN
RV3135B5X	SC15	M
RX1011B350Y	SC15	M

TYPE NUMBER	BOOK	SECTION
RX1214B150Y	SC15	M
RX1214B300Y	SC15	M
RX2731B90W	SC15	M
RX3034B70W	SC15	M
RXB12350Y	SC15	M
RZ1214B35Y	SC15	M
RZ1214B65Y	SC15	M
RZ2731B16W	SC15	M
RZ2731B32W	SC15	M
RZ2731B48W	SC15	M
RZ2731B60W	SC15	M
RZ3135B14W	SC15	M
RZ3135B28W	SC15	M
RZ3135B42W	SC15	M
RZ3135B50W	SC15	M
RZB12050Y	SC15	M
RZB12100Y	SC15	M
RZB12250Y	SC15	M
SL5500	SC12	PhC
SL5501	SC12	PhC
SL5504	SC12	PhC
SL5505S	SC12	PhC
SL5511	SC12	PhC
TIP29*	SC05	P
TIP30*	SC05	P
TIP31*	SC05	P
TIP32*	SC05	P
TIP33*	SC05	P
TIP34*	SC05	P
TIP41*	SC05	P
TIP42*	SC05	P
TIP47	SC06	P
TIP48	SC06	P
TIP49	SC06	P
TIP50	SC06	P
TIP110	SC05	P
TIP111	SC05	P
TIP112	SC05	P
TIP115	SC05	P
TIP116	SC05	P

TYPE NUMBER	BOOK	SECTION
TIP117	SC05	P
TIP120	SC05	P
TIP121	SC05	P
TIP122	SC05	P
TIP125	SC05	P
TIP126	SC05	P
TIP127	SC05	P
TIP130	SC05	P
TIP131	SC05	P
TIP132	SC05	P
TIP135	SC05	P
TIP136	SC05	P
TIP137	SC05	P
TIP140	SC05	P
TIP141	SC05	P
TIP142	SC05	P
TIP145	SC05	P
TIP146	SC05	P
TIP147	SC05	P
TIP2955	SC05	P
TIP2955T	SC05	P
TIP3055	SC05	P
TIP3055T	SC05	P
VN2406L	SC07	FET
VN2410L	SC07	FET
1N821	SC01	Vrf
1N821A	SC01	Vrf
1N823	SC01	Vrf
1N823A	SC01	Vrf
1N825	SC01	Vrf
1N825A	SC01	Vrf
1N827	SC01	Vrf
1N827A	SC01	Vrf
1N829	SC01	Vrf
1N829A	SC01	Vrf
1N914	SC01	SD
1N916	SC01	SD
1N4001D	SC01	R
1N4002D	SC01	R
1N4003D	SC01	R

TYPE NUMBER	BOOK	SECTION
1N4004D	SC01	R
1N4005D	SC01	R
1N4006D	SC01	R
1N4007D	SC01	R
1N4001G	SC01	R
1N4002G	SC01	R
1N4003G	SC01	R
1N4004G	SC01	R
1N4005G	SC01	R
1N4006G	SC01	R
1N4007G	SC01	R
1N4148	SC01	SD
1N4150	SC01	SD
1N4151	SC01	SD
1N4153	SC01	SD
1N4446	SC01	SD
1N4448	SC01	SD
1N4531	SC01	SD
1N4532	SC01	SD
1N4933	SC01	R
1N5059	SC01	R
1N5060	SC01	R
1N5061	SC01	R
1N5062	SC01	R
1N5225 to	SC01	R
1N5267B	SC01	R
2N918	SC14	WBT
2N930	SC04	Sm
2N1613	SC04	Sm
2N1711	SC04	Sm
2N1893	SC04	Sm
2N2219	SC04	Sm
2N2219A	SC04	Sm
2N2222	SC04	Sm
2N2222A	SC04	Sm
2N2297	SC04	Sm
2N2369	SC04	Sm
2N2369A	SC04	Sm
2N2483	SC04	Sm
2N2484	SC04	Sm

TYPE NUMBER	BOOK	SECTION
2N2646	SC04	Sm
2N2894A	SC04	Sm
2N2904	SC04	Sm
2N2904A	SC04	Sm
2N2905	SC04	Sm
2N2905A	SC04	Sm
2N2906	SC04	Sm
2N2906A	SC04	Sm
2N2907	SC04	Sm
2N2907A	SC04	Sm
2N3019	SC04	Sm
2N3020	SC04	Sm
2N3053	SC04	Sm
2N3375	SC08a	RFP
2N3439	SC04	Sm
2N3440	SC04	Sm
2N3553	SC08a	RFP
2N3632	SC08a	RFP
2N3819	SC07	FET
2N3820	SC07	FET
2N3822	SC07	FET
2N3823	SC07	FET
2N3866	SC08a	RFP
2N3904	SC04	Sm
2N3905	SC04	Sm
2N3906	SC04	Sm
2N3924	SC08a	RFP
2N3926	SC08a	RFP
2N3927	SC08a	RFP
2N3966	SC07	FET
2N4030	SC04	Sm
2N4031	SC04	Sm
2N4032	SC04	Sm
2N4033	SC04	Sm
2N4036	SC04	Sm
2N4091	SC07	FET
2N4092	SC07	FET
2N4093	SC07	FET
2N4123	SC04	Sm
2N4124	SC04	Sm

TYPE NUMBER	BOOK	SECTION
2N4125	SC04	Sm
2N4126	SC04	Sm
2N4220	SC07	FET
2N4220A	SC07	FET
2N4221	SC07	FET
2N4221A	SC07	FET
2N4222	SC07	FET
2N4222A	SC07	FET
2N4340	SC07	FET
2N4391	SC07	FET
2N4392	SC07	FET
2N4393	SC07	FET
2N4400	SC04	Sm
2N4401	SC04	Sm
2N4402	SC04	Sm
2N4403	SC04	Sm
2N4416	SC07	FET
2N4416A	SC07	FET
2N4427	SC08a	RFP
2N4856	SC07	FET
2N4857	SC07	FET
2N4858	SC07	FET
2N4859	SC07	FET
2N4860	SC07	FET
2N4861	SC07	FET
2N5064	SC03	Tri
2N5086	SC04	Sm
2N5087	SC04	Sm
2N5088	SC04	Sm
2N5116	SC07	FET
2N5400	SC04	Sm
2N5401	SC04	Sm
2N5415	SC04	Sm
2N5416	SC04	Sm
2N5460	SC07	FET
2N5461	SC07	FET
2N5462	SC07	FET
2N5484	SC07	FET
2N5485	SC07	FET
2N5486	SC07	FET

TYPE NUMBER	BOOK	SECTION
2N5550	SC04	Sm
2N5551	SC04	Sm
2N5680	SC04	Sm
2N6027	SC04	Sm
2N6028	SC04	Sm
2N6659	SC07	FET
2N6660	SC07	FET
2N6661	SC07	FET
2N7000	SC07	FET
2N7002	SC07	FET
2PA733	SC04	Sm
2PA1015	SC04	Sm
2PA1015L	SC04	Sm
2PC945	SC04	Sm
2PC1815	SC04	Sm
2PC1815L	SC04	Sm
4N25	SC12	PhC
4N25A	SC12	PhC
4N26	SC12	PhC
4N27	SC12	PhC
4N28	SC12	PhC
4N29	SC12	PhC
4N30	SC12	PhC
4N31	SC12	PhC
4N32	SC12	PhC
4N33	SC12	PhC
4N35	SC12	PhC
4N36	SC12	PhC
4N37	SC12	PhC
4N38	SC12	PhC
4N38A	SC12	PhC
4N46	SC12	PhC
6N135	SC12	PhC
6N136	SC12	PhC
56201d	SC06	A
56201j	SC06	A
56245	SC04/14	A
56246	SC04/14	A
56261a	SC06	A
56264	SC03	A

TYPE NUMBER	BOOK	SECTION
56264a	SC02/03	A
56264b	SC02/03	A
56295	SC03	A
56295a	SC02/03	A
56295b	SC02/03	A
56295c	SC02/03	A
56326	SC06	A
56339	SC06	A
56352	SC06	A
56353	SC06/03	A
56354	SC06/03	A
56359b	SC02/03	A
56359c	SC02/03	A
56359d	SC02/03	A
56360a	SC02/03	A
56363	SC02/03	A
56364	SC02/03	A
56367	SC02/03	A
56368b	SC02/03	A
56368c	SC02/03	A
56369	SC02/03	A
56378	SC02/03	A
56379	SC02/03	A
56387a	SC06	A
56387b	SC06	A
56397	SC01	A

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

The contents of each series are listed on pages iii to ix.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom;** Subscriber sets, Cordless Telephones, Mobile/Cellular, Radio Pagers
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; 74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
Supplement to IC07	**Advanced CMOS logic (ACL)**
IC08	**10/100K ECL Logic/Memory/PLD**
IC09	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Programmable Logic Devices (PLD)**
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom;** ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**
IC20	**8051-based 8-bit microcontrollers**
IC23	**Advanced BiCMOS interface logic**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	SC01	**Diodes** High-voltage tripler units
S2a	SC02	**Power diodes**
S2b	SC03	**Thyristors and triacs**
S3	SC04	**Small-signal transistors**
S4a	SC05	**Low-frequency power transistors and hybrid IC power modules**
S4b	SC06	**High-voltage and switching power transistors**
S5	SC07	**Small-signal field-effect transistors**
S6	SC08a*	**RF power bipolar transistors**
	SC08b	**RF power MOS transistors**
	SC09	**RF power modules**
S7	SC10	**Surface mounted semiconductors**
S8b	SC12	**Optocouplers**
S9	SC13*	**PowerMOS transistors**
S10	SC14	**Wideband transistors and wideband hybrid IC modules**
S11	SC15	**Microwave transistors**
S15**	SC16	**Laser diodes**
S13	SC17	**Semiconductor sensors**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

code	handbook title
DC01	**Colour display components** Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	**Monochrome monitor tubes and deflection units**
DC03	**Television tuners, coaxial aerial input assemblies**
DC04	**Loudspeakers**
DC05	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	PA01	**Electrolytic capacitors; solid and non-solid**
C11	PA02	**Varistors, thermistors and sensors**
C12	PA03	**Potentiometers and switches**
C7	PA04	**Variable capacitors**
C22	PA05*	**Film capacitors**
C15	PA06	**Ceramic capacitors**
C9	PA07*	**Piezoelectric quartz devices**
C13	PA08	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T3	PC01	High-power klystrons and accessories
T5	PC02*	Cathode-ray tubes
T6	PC03*	Geiger-Müller tubes
T9	PC04	Photo multipliers
T10	PC05	Plumbicon camera tubes and accessories
T11	PC06	Circulators and Isolators
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09	Dry-reed switches
	PC11	Solid state image sensors and peripherals integrated circuits
T9	PC12*	Electron multipliers

* Not yet issued with the new code in this series of handbooks.

MAGNETIC PRODUCTS

This series of data handbooks comprises:

current code	new code	handbook title
C4, C5	MA01	**Soft Ferrites**
C16	MA02*	**Permanent magnet materials**
C19	MA03*	**Piezoelectric ceramics**

* Not yet issued with the new code in this series of handbooks.

LIQUID CRYSTAL DISPLAYS

current code	new code	handbook title
S14	**LCD01**	**Liquid Crystal Displays and driver ICs for LCDs**

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